

Development of Telescope Readout System based on FELIX for Testbeam Experiments



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Motivation

The ATLAS experiment is planning to build a new all-silicon Inner Tracker (ITk) for the High-Luminosity LHC (HL-LHC). The High Voltage CMOS (HV-CMOS) sensors are extensively investigated for multiple advantages compared to the traditional planar pixel detectors. The FE-I4B Telescope has been built to test HV-CMOS sensor prototypes. The Front-End LInk eXchange (FELIX) is a system to interface the front-end electronics and trigger electronics for several detectors in the ATLAS Phase-I and HL-LHC upgrade. The PCIe based FELIX system has been successfully integrated with the CaRIBOu (Control and Readout Itk BOard) system for HV-CMOS sensors readout in 2016 testbeam at CERN. A new system has been developed for the readout of testbeam telescope sensors as well as the HV-CMOS sensor in the CaRIBOu system with the goal to have the full testbeam readout upgraded to the FELIX system.

Test Setup for Telescope Readout based on FELIX

- FELIX: The interface between the detector front-end electronics and the readout system in the ATLAS upgrade.
- FE-I4B Telescope: It consists of six ATLAS Insertable B-Layer (IBL) doublechip (DC) pixel modules, which is built mainly for the study of the HV-CMOS sensor.
- CaRIBOu: A modular test system for HV-CMOS sensor R&D in the ITk. Its readout chip is the FE-I4B.

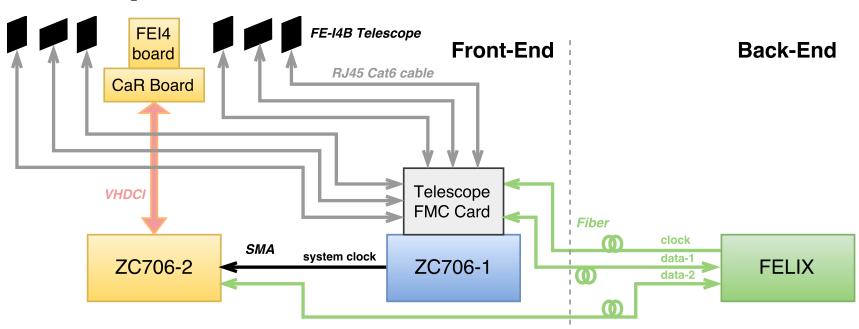


Figure 1. Test Setup of FE-I4B Telescope and CaRIBOu readout based on the FELIX

- FELIX configuration
 - To-host path: GBT mode with 8b10b encoding
 - From-host path: GBT mode without 8b10b encoding
 - 4-bit Elinks are used for both data paths.
 - Low level FELIX software is used.
- Two Xilinx ZC706 boards are used in the front-end.
 - Optimized fixed-latency GBT-FPGA.
 - Both ZC706 boards are 'transparent' for FE-I4B communication.
 - Slow control via the FELIX GBT link
 - Configuration of Si5345 on the Telescope Readout FMC Card
 - Programmable phase with IDELAY configuration for the FE-I4B data
- A Telescope Readout FMC Card is designed as an interface between IBL DC modules and the ZC706 board.
- Three GBT links are used on the FELIX in the back-end: one for clock distribution and the other two for data transmission.

FE-I4B Tuning Test

- Read/write global registers, shift registers and in-pixel registers
- Initial configuration
- Noise scan
- Digital/Analog scan
- Tuning test
- Threshold scan

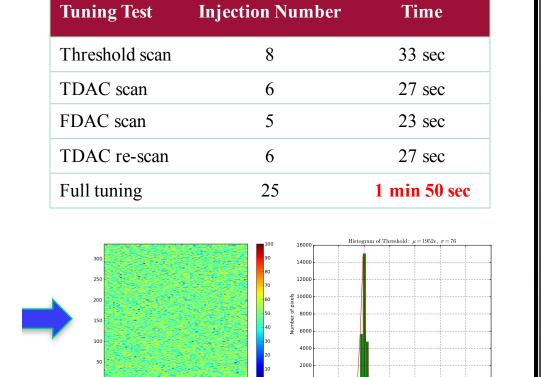


Table 1. Time needed for Tuning Test

Figure 2. Heatmap and Threshold Distribution before and after Tuning Test

Injection Test of H35DEMO Sensor on the CaRIBOu

- FE-I4B configuration
- H35DEMO configuration
 - Slow control bus
- Configuration of injection signals
- Send injection signals to H35DEMO sensor following Trigger commands to the FE-I4B readout chip
- Figure 3. Injection of Analog Matrix

of H35DEMO

Telescope Readout FMC Card

- An adapter between the IBL DC modules and the ZC706 board.
- Provide extra GBT links to FELIX
- Improve recovered clock quality
- Receive two HitOR signals from the FE-I4B Telescope for Trigger generation

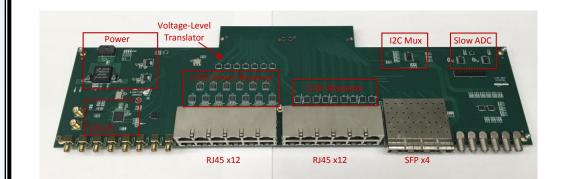
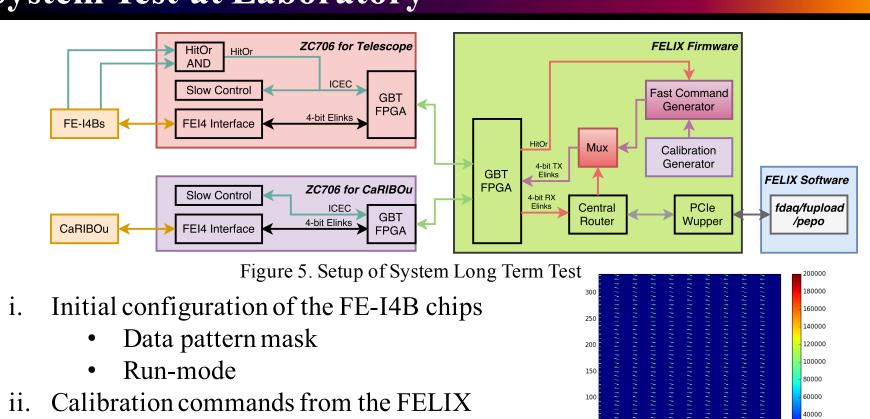


Figure 4. Telescope Readout FMC Card

- FMC connectors
- RJ45 connectors
- SFP connectors
- Voltage level translator Clock chip of Si5345

System Test at Laboratory



iii. Two HitOR signals for Trigger command

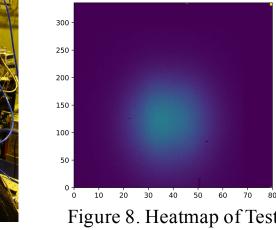
iv. Long term test

Figure 6. System Test Results

Testbeam

- Successful testbeam at CERN in August, 2017
- FE-I4B Telescope & CaRIBOu readout via the FELIX
- HitOR signals of the front and back IBL DC modules are used to generate Trigger command inside the FELIX.
- Stable operation for data taking





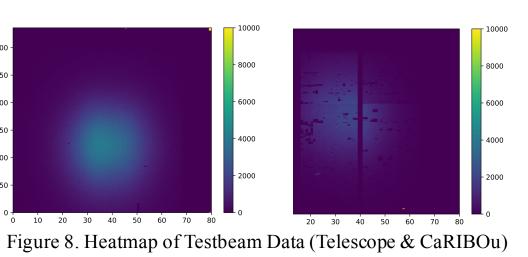


Figure 7. Testbeam Setup

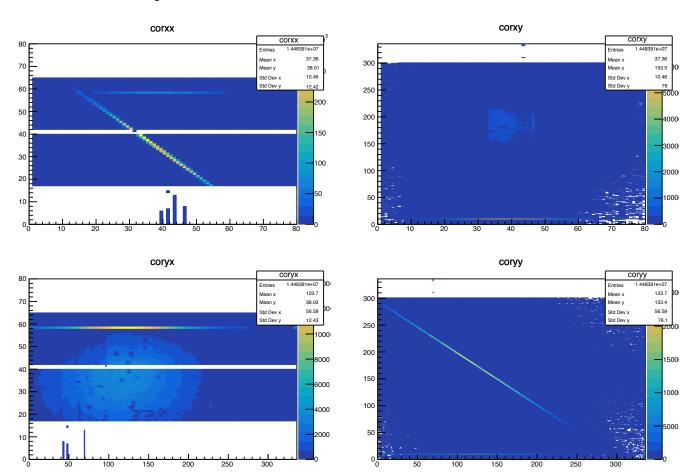


Figure 9. Correlation of Telescope and CaRIBOu Testbeam Data