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## Development of Telescope Readout System Based on FELIX for Testbeam Experiments

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A testbeam telescope, based on the ATLAS IBL silicon pixel modules, has been built to investigate the possibility of using the CMOS technology in the HL-LHC upgrade of ITk. The Front-End LInk eXchange (FELIX) system is a new approach to function as the gateway between different front-ends and the commodity switched network in the ATLAS upgrade. A FELIX based readout system has been developed for the testbeam telescope, including a FMC Telescope Readout Card for data transmission. The test results show that it is capable of high-density pixel sensor calibration and readout effectively, and being deployed in the testbeam experiments.

### Summary

The ATLAS experiment is planning to build a new all-silicon Inner Tracker (ITk) for the High-Luminosity LHC (HL-LHC). The High Voltage CMOS (HV-CMOS) sensors are extensively investigated for multiple advantages compared to the traditional planar pixel detectors. The FE-I4 telescope has been built to test small HV-CMOS prototypes, which consists of six ATLAS Insertable B-Layer (IBL) double-chip (DC) pixel modules. The Front-End LInk eXchange (FELIX) is a system to interface the front-end electronics and trigger electronics for several detectors in the ATLAS Phase-I and HL-LHC upgrade. The PCIe based FELIX has been verified as a good option for HV-CMOS sensors readout. A new system is being developed for the readout of testbeam telescope sensors, with the goal to have the full testbeam readout upgraded to the FELIX system.

This FELIX based readout system includes a Xilinx ZC706, an interface FMC Telescope Readout Card and a FELIX in the back-end. The Xilinx ZC706 is the main FELIX interface in the front-end. It consists several firmware modules, including the FE-I4 interface module, the low-latency GBT-FPGA, and other control parts. The FE-I4 output data is a 160 Mbps 8b/10b encoded serial signal, which is de-serialized, aligned and decoded in the ZC706. Different data types from FE-I4 will also be extracted and buffered. There are two GBT links between ZC706 and FELIX: one is used to distribute the clock signal from FELIX to ZC706, and the other is for data transmission. The FELIX software is responsible for issuing all the control commands and continuously storing all the pixel data from the front-end for off-line analysis.

An interface board, FMC Telescope Readout Card, has been designed, which will be placed between IBL DC modules and the ZC706 board. This board is connected to the ZC706 through FMC connectors, with single external 12-V power supply. There are 12 RJ45 ports connecting to all the IBL DC modules in the testbeam telescope, and 4 SFP connectors for GBT links. A clock chip of Si5345 is implemented on board in order to improve the quality of recovered clock from the GBT link. This clock chip can be configured from FELIX through the GBT link. The hardware design of the FMC Telescope Readout Card has been verified, including the power rails, I2C bus, Si5345, SFP connectors, LVDS repeaters, etc.

The previous version of this FELIX based readout system has been used to readout Device Under Test (DUT) in the testbeam in August, 2016 at CERN. The configuration and tuning of both CCPD sensor and FE-I4 chip can be fulfilled with a good efficiency. During a more than 13-hours of data taking, the testbeam data can be streamed from the FE-I4 to the disk without any loss. With the new FMC Telescope Readout Card, the readout of telescope sensors will also be realized with FELIX system. It is planned to have the full testbeam readout upgraded to the FELIX system by summer 2017.

**Primary author:** WU, Weihao (Brookhaven National Laboratory (US))

**Co-authors:** BENOIT, Mathieu (UNIGE); CHEN, Hucheng (Brookhaven National Laboratory (US)); CHEN, Kai (Brookhaven National Laboratory (US)); IACOBUCCI, Giuseppe (Universite de Geneve (CH)); LANNI, Francesco (Brookhaven National Laboratory (US)); LIU, Hongbin (Brookhaven National Laboratory (US)); XU, Lailin (Brookhaven National Laboratory (US))

**Presenter:** WU, Weihao (Brookhaven National Laboratory (US))

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