TWEPP Poster Session - UCSC, 13th September 2017

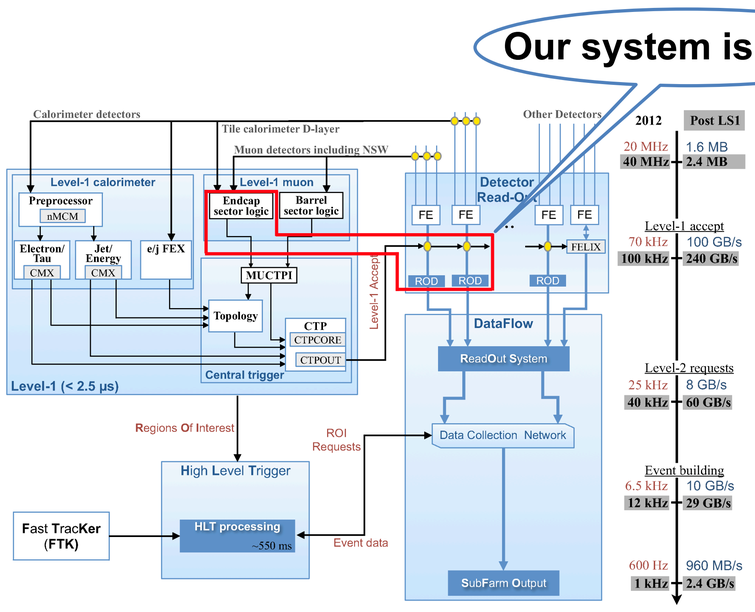
Development of the new Trigger Processor Board for the ATLAS Level-1 Endcap Muon Trigger for Run-3

ATLAS Muon Trigger System

With the current system, the trigger rate above a p_T threshold of 20 GeV would be an unacceptable rate (~28 kHz) of the Level-1 system at an instantaneous luminosity of 3×10^{34} cm^{-2}s^{-1}.

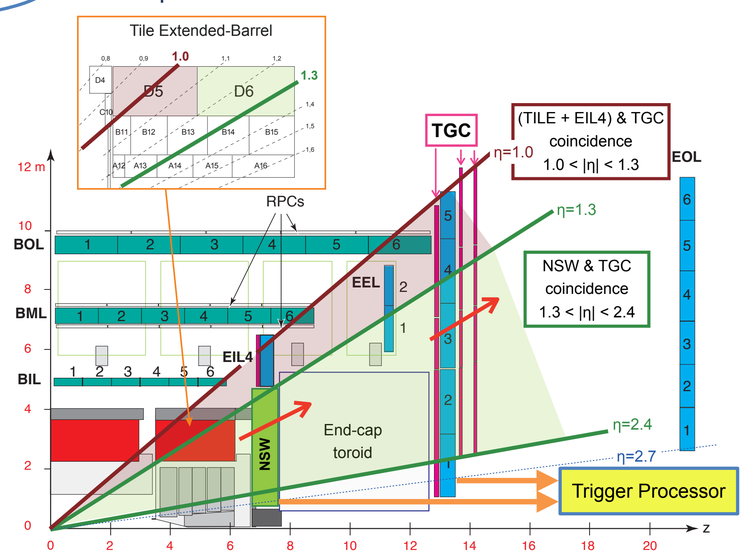
→ **Introduce the new trigger**

[Trigger and Data Acquisition System]



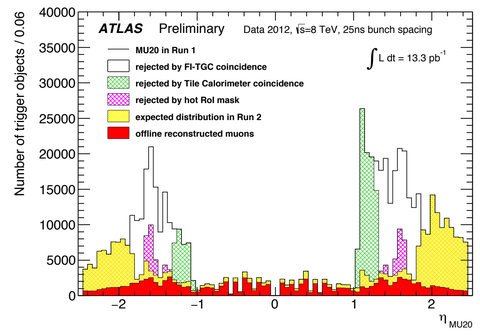
Timing, Trigger and Control (TTC) signals which contain the event ID, trigger, and control signals are provided from CTP to sub-detectors. Each detector can be synchronized using the TTC signals.

New Small Wheel (NSW) consists of small-strip TGC and MicroMegas detectors with high-rate tolerance and improved resolution.

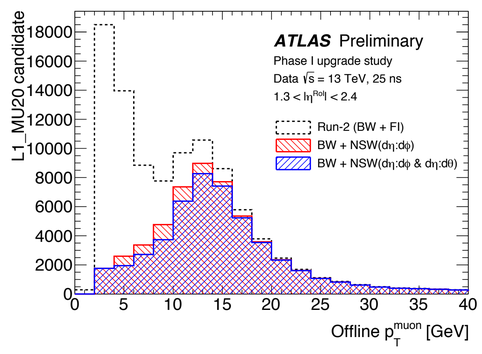


The level-1 endcap muon trigger will improve the rejection power of fake triggers by incorporating track vector information from NSW.

Expected performance



Introducing NSW, which **covers a wider range** (1.3 < |η| < 2.7) than old Small Wheel (1.0< |η| < 1.9), it is possible to **reduce the trigger rate in high eta regions.**



p_T distributions of offline reconstructed muons matched to a Level-1 triggers for a single muons with p_T above 20 GeV.

Introducing the NSW can **reduce low p_T muons trigger rate.**

→ **28 kHz → 13 kHz.**

Trigger Processor (New Sector Logic)

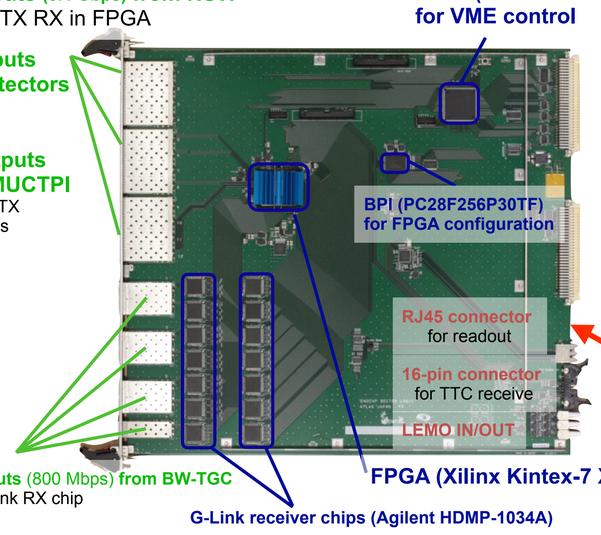
- Calculate the muon p_T for each trigger sector and make trigger decision
- Send p_T and Region of Interest (ROI) information to MUCTPI

6 optical inputs (6.4 Gbps) **from NSW**
SFP+ with GTX RX in FPGA

6 optical inputs for other detectors

2 optical outputs (6.4 Gbps) **to MUCTPI**
SFP+ with GTX TX
10 optical outputs for spares

CPLD (XC2C256-7PQ208C) for VME control

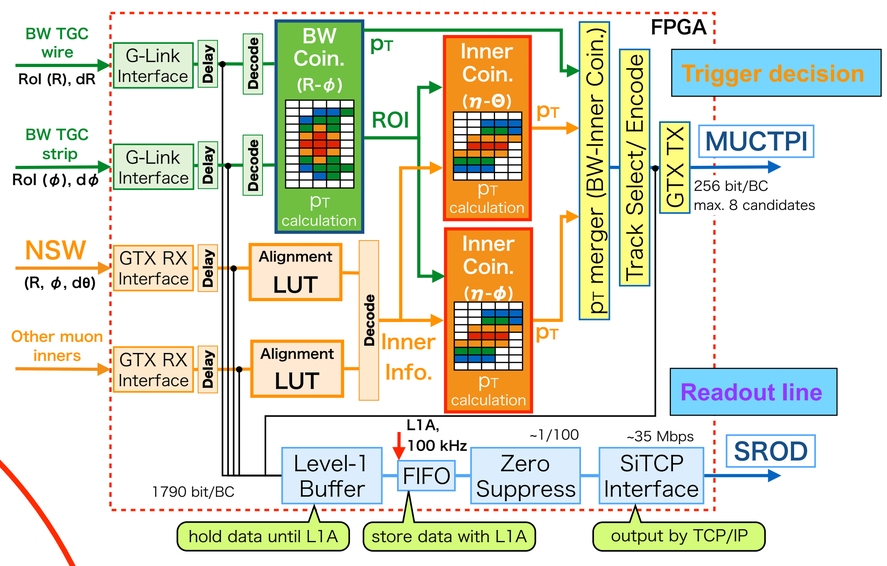


14 optical inputs (800 Mbps) **from BW-TGC**
SFP RX + G-Link RX chip

FPGA (Xilinx Kintex-7 XCK325T)

G-Link receiver chips (Agilent HDMP-1034A)

New Sector Logic firmware diagram



Trigger Decision

1. BW d*R*-dφ coincidence
   - input data from BW-TGC wires and strips respectively
   - calculate p_T by taking *R* and φ coincidence
2. BW-NSW coincidence
   - add R, φ and dθ from NSW
   - take dη-dφ coincidence and calculate p_T

Readout Line

- Level-1 Buffer stores the received data and trigger decision information until trigger coming
- FIFO stores the data with trigger
- Zero-Suppress
- The readout data are sent to SROD by TCP/IP (SiTCP)
- SiTCP is the technology which connects to Xilinx FPGA to the Ethernet

TTC FAN-OUT BOARD

- Propagate TTC signals to each NSL
- Readout TTC signals at maximum rate of 100 kHz
- Busy control

optical input, output
Maximum rate : 6.4 Gbps
SFP+ with GTP TX and RX

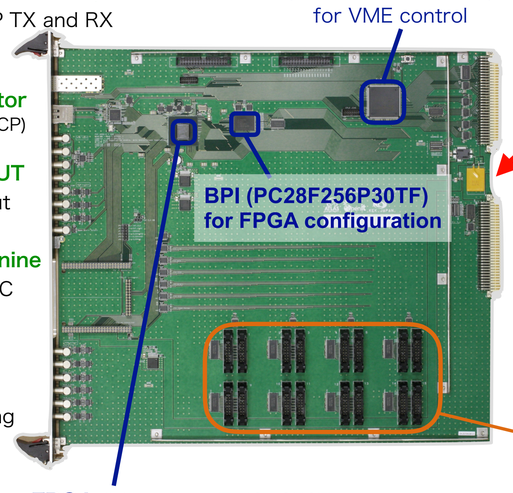
CPLD (XC2C256-7PQ208C) for VME control

RJ45 connector for readout (SiTCP)

LEMO IN/OUT Busy output

TTCrq mezzanine receives TTC signals

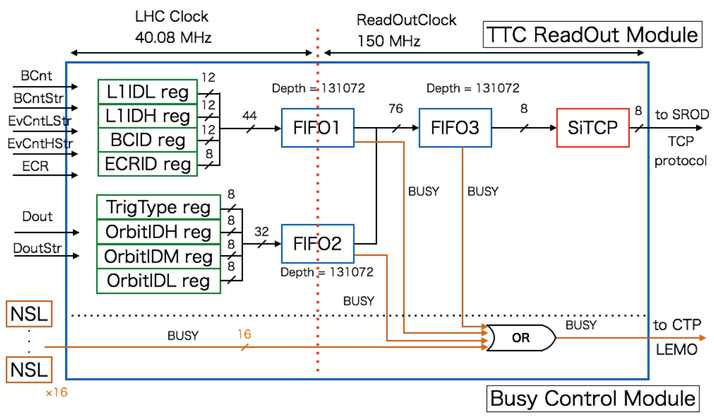
LEMO OUT for monitoring TTC signals



FPGA (Xilinx Artix-7 XCA676T)

Flat Cable connectors to propagate TTC signals to each SL board
Busy signals from SL boards

TTC FAN-OUT BOARD firmware diagram



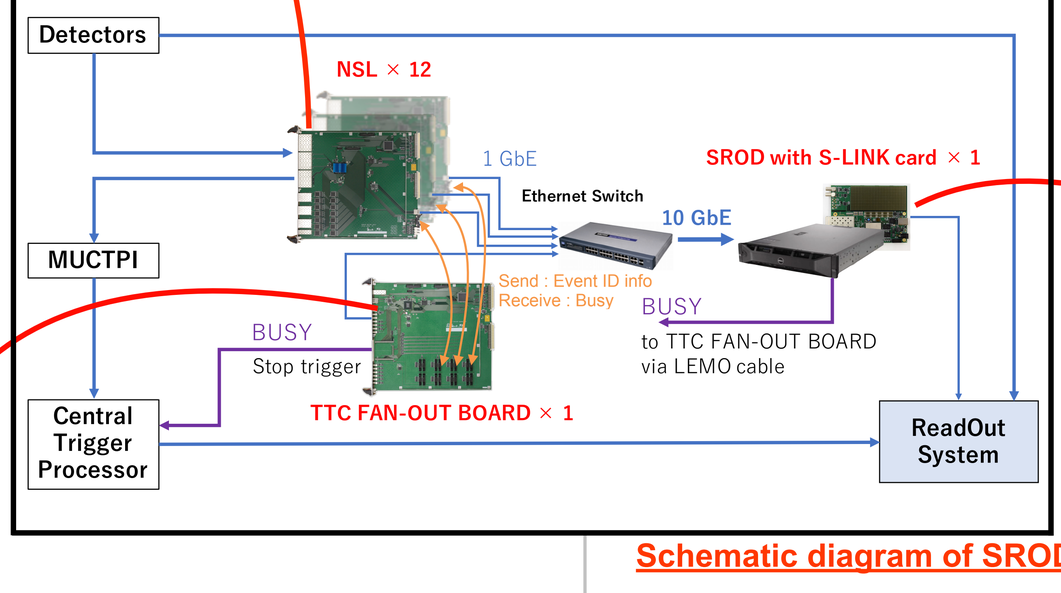
TTC ReadOutModule

- Receive the data from TTCrq and readout by each event
- Data formatting to send to SROD
- output by TCP/IP (SiTCP)

Busy Control Module

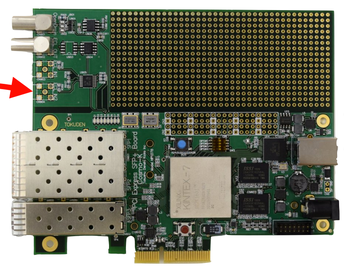
- Implemented in the TTC ReadOutModule
- Take “OR” from NSLs, SROD and own FIFO
- Send to CTP by LEMO to stop trigger

Brief diagram for the new read-out scheme



Software-based ReadOut Driver (SROD)

- SROD is implemented by multi process on PC
- Event Building
- Data Formatting
- Error Handling

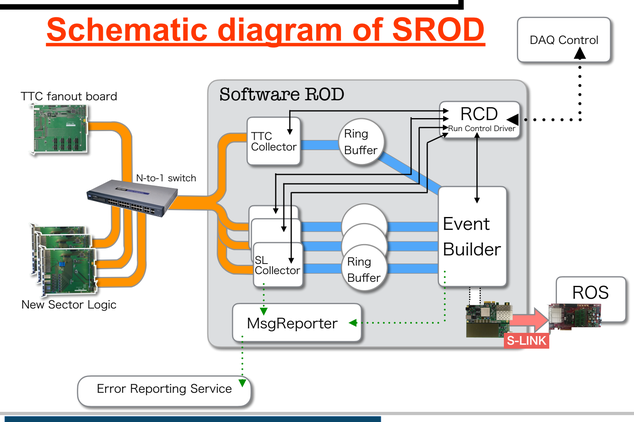


PCIe S-LINK card

- Send data to ReadOut System
- Send SROD Busy to TTC FAN-OUT BOARD

- S-LINK is a CERN specification for FIFO-like data-link which can be used to connect front-end to read-out at any stage in a data flow environment

Schematic diagram of SROD



SL/TTC Collector

- Reads data from NSL (TTC FAN-OUT) board
- One process per board

Ring Buffer

- Absorbs the timing variation in receipt of data

Event Builder

- Reads data from the ring buffer and builds the ROD event fragments

Run Control Driver (RCD)

- Synchronizes each process state with the ATLAS detectors

Message (Msg) Reporter

- Sends message to Error Reporting Service

Current Achievement

- Prototype of NSL and TTC FAN-OUT BOARD were made and its design was verified
- A beam test was done using CERN SPS Beam Facility and checked whole phase-1 system (NSL, TTC FAN-OUT BOARD and SROD) is working

Future Plan

- Test for actual setup which uses 12 NSL, 1 TTC FAN-OUT BOARD and 1 SROD will be performed.
- Connection test with MUCTPI will be performed
- Mass-production of NSL and TTC FAN-OUT BOARD in 2018

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