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Development of the New Trigger Processor Board for the ATLAS Level-1 Endcap Muon Trigger for Run-3

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The ATLAS first-level Endcap Muon trigger in LHC Run-3 will
identify muons by combining data from the Thin-Gap chamber detector (TGC) and a new detector, called the New-Small-Wheel (NSW). In order to handle data from both TGC and NSW, new trigger processor board has been developed. The board has a modern FPGA to make use of Multi-Gigabit transceiver technology. The readout system for trigger data has also been implemented with TCP/IP instead of a dedicated ASIC. This presentation will focus on the electronics and its firmware of the ATLAS first-level Endcap Muon trigger processor board for LHC Run-3.

Summary

The LHC performance for Run-3 is expected to increase its
instantaneous luminosity to $3 \times 10^{3\mathrm{cm}^{-2}\mathrm{s}^{-1}}$ after the 'Phase-1'upgrade, to take place from 2018-2020. In order to cope with this high luminosity, an upgrade of the ATLAS trigger system will be required.
The ATLAS first-level Endcap Muon trigger system identifies muons with high transverse momentum from 40 MHz bunch crossings, using data from fast muon trigger detectors, TGC. The whole system is implemented on a special trigger circuit, which makes the trigger decision latency as short as 2.2 us. In LHC Run-2, the Endcap Muon trigger requires the coincidence between TGC Big-Wheel (BW) at the middle station and the Small-Wheel at the inner station, in order to reduce the fake triggers of beam-induced backgrounds by slow-particles from the endcap toroid or shields.
In the Phase-1 upgrade, a new detector, called New-Small-Wheel (NSW), will be installed at the small wheel region. NSW provides information of finer position and direction of the track, which can be used for the trigger selection by the trigger processor board. Finer track information from the NSW can be used as part of the trigger logic to enhance performance significantly. We aim to keep the trigger
rate for muons with $p_T > 20$ GeV/c, at the same level as it is now.
In order to handle data from both TGC and NSW, some new
electronics, including a 9U VME board known as the trigger processor, are being developed. The trigger processor board has a modern FPGA to make use of Multi-Gigabit transceiver technology, which will be used to receive data from the NSW. The firmware implemented in a FPGA on the trigger processor board consists of two major parts, trigger and readout. The trigger part does to receive data, to calculate the muon momentum with a fixed latency, and to output the trigger decision to the central trigger system. The readout system for trigger data has also been re-designed, with data transmission implemented with TCP/IP instead of by a dedicated ASIC, by using SiTCP technology. This makes
it possible to minimize the use of custom readout electronics and instead use some commercial PCs and network switches to collect, format, and send the data.
This presentation will describe the aforementioned upgrades of the first-level Endcap Muon trigger system. Particular emphasis will be placed on the new Sector Logic electronics and the firmware. The performance of software readout system, and the latest results of the trigger performance study for LHC Run-3 will be also discussed.

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