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Simulations of Busy Probabilities in the ALPIDE Chip and the Upgraded ALICE ITS Detector

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For the LS2 upgrade of the ITS detector in the ALICE experiment at the LHC, a novel pixel detector chip, the ALPIDE chip, has been developed. In the event of busy ALPIDE chips in the ITS detector, the readout electronics may need to take appropriate action to minimize loss of data. A lightweight, statistical simulation model for the ALPIDE/ITS has been designed using the SystemC framework.

With the simulations we have been able to quantify the probability of busy situations under various conditions, which is crucial knowledge for the further design and development of the readout electronics.

Summary

For the upgrade of the Inner Tracking System (ITS) in the ALICE experiment at the LHC, a novel pixel detector chip called ALPIDE has been developed.
The upgraded ITS will consist of over 24,000 ALPIDE chips spread out over 192 detector staves in 7 layers. Each stave is connected to its own Readout Unit (RU), and 8 RUs are connected to a dedicated Common Readout Unit (CRU). The readout electronics is currently under development, and investigations are ongoing to decide if a dedicated system for monitoring and handling busy situations in the ALPIDE chips is required.

Due to the random and unpredictable nature of the collisions at LHC, there will be situations where some of the ALPIDE chips will have their Multi Event Buffer (MEB) slices filled faster than the events can be read out. In this situation, the chips will send busy messages so that the RUs can take appropriate measures.
Reducing the trigger rate may be one such measure. Forwarding the information to components later in the chain so that the busy decision is taken on larger parts of the detector may be another.

It will be crucial to have a busy monitoring system. If this system should also take active actions is not clear yet, and this can only be decided once the probability of busy chips is known with a high statistical certainty. None of the existing simulation models have been suitable for this task, as they were either extremely accurate, and comparably slow; did not scale for the whole detector; or they did not model the right parts of the ALPIDE chip required for these simulations. Additionally, no simulation has so far been done of the whole readout chain, including ALPIDE, RU and potentially the CRU.

A simplified simulation model of the ALPIDE has been developed using the SystemC framework. In this simulation model a purely statistical approach to event generation has been used. The events are created with random inter-event times, event multiplicities, and hit coordinates, all following well known statistical distributions that are representable for an LHC experiment. Only the necessary parts of logic in the ALPIDE chip were implemented, using a high level of abstraction in order to reduce simulation time.

The simulation model can easily be adapted for a variety of detector configurations, and currently a model of the RU is being included into the model. The simulations so far have proven to be in line with the expected results from earlier simulations (readout efficiency of up to 99.86% in 100kHz Pb-Pb, triggered mode).

Other possible applications of the simulation model include being used as an accurate ALPIDE data generator. This is useful for RU design or input to other simulations. Additionally, other research projects will be using

the ALPIDE chip, to which the simulation model can easily be adapted.

Primary author: NESBO, Simon Voigt (Western Norway University of Applied Sciences (NO))

Co-authors: ALME, Johan (University of Bergen (NO)); ROHRICH, Dieter (Department of Physics & Technology-University of Bergen); HELSTRUP, Haavard (Western Norway University of Applied Sciences (NO)); GIUBILATO, Piero (Universita e INFN, Padova (IT)); AGLIERI RINELLA, Gianluca (CERN); SHAHOYAN, Ruben (CERN); ULLALAND, Kjetil (University of Bergen (NO)); HRISTOZKOV, Svetlomir; SCHAMBACH, Joachim (University of Texas (US))

Presenter: NESBO, Simon Voigt (Western Norway University of Applied Sciences (NO))

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