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Functionality and Performance of the ALFA_CTPIN Module

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During first long stoppage (LS1) of the LHC, the Central Trigger Processor (CTP) of the ATLAS experiment has been upgraded. In addition to enriched functionality, it resulted in increasing the CTP input-output latency by 75 ns (3 cycles@40 MHz). The ALFA triggers were no longer early enough to contribute to the global ATLAS triggering. A dedicated input board, speeding up the ALFA signal processing and providing advanced monitoring of the ALFA trigger signals, has been therefore required.
The ALFA_CTPIN module has been designed to deliver requested functionality. In this text, we will give description of it and present achieved performance.

Summary

The ALFA_CTPIN module has been designed in VME standard. To its inputs it receives the LHC clock and orbit synchronising signals from the CTP (40 MHZ and 11 kHz, respectively) and up to 16 trigger signals from ALFA detector stations. From its outputs it drives ALFA triggers to the CTP.

The whole functionality of the ALFA_CTPIN has been implemented in two FPGA chips present on the motherboard. The module's logic consists of the following functional blocks: Trigger-Decoder, Trigger-Processing Unit, Rate-Counters Unit, Test-Pattern Generator, Phase-Measurement Unit and VME Interface.

The Trigger-Decoder processes trigger signals coming from ALFA detector stations. Each detector station sends to the ALFA_CTPIN module encoded trigger signals coming either from the Main-Detector (MD) or the Overlap-Detector (OD). The Trigger-Decoder detects the trigger type and produces on its MD or OD outputs unique trigger pulses driven directly to the ATLAS CTP module. The latency of trigger detection is 50 ns (4 cycles@80 MHz) while the introduced dead-time is 75 ns which is still inside 100 ns dead-time of the ALFA detector itself.

The MD and OD triggers are also made available internally to the Trigger-Processing Unit for further processing. The MD and OD outputs from the Trigger-Decoder form four 8-bit wide vectors used for addressing individual Look-Up-Tables (LUTs) which produce 128-bit wide data on their outputs. This output data then passes through a combinatorial stage were bit-masking, AND or OR operations are applied to produce final values of 128 trigger items. Bit-masking contents as well as combinatorial function selection is pre-settable individually to each trigger item via VME. The latency of trigger processing is 25 ns (1 cycle@40 MHz).

Such processed trigger items feed the Scalers Unit to measure their rates. There are two type of scalers: Simple and BC ones. While the Simple scalers measure the aggregate rate, the BC ones measure the rate per specific LHC bunch number (BC). There are 128 Simple scalers and 26 BC ones, both scaler types sum the trigger items' counts over either 1 or 10 seconds.
For commissioning and testing purposes, the Phase-Measurement Unit and Test-Pattern Generator have been implemented in the module's logic.
The Phase-Measurement Unit measures the interval between leading edges of incoming ALFA trigger signals and the main clock of the module, respectively. The resolution of this measurement is 2.5 ns.
The Test-Pattern Generator allows to generate internally any ALFA triggers' patterns which may arrive to all inputs of the module within one orbit signal of the LHC. The patterns can be generated for specific number of cycles or as long as they're enabled.

A dedicated, standalone software has been developed to create and verify the logic for the trigger items. The configuration of the module and access to rates of the trigger items uses ATLAS TDAQ software. The module is configured and controlled by the RCD application. Every 1.3 sec the scalers from the module are readout using the VME interface. The collected data are then published either as raw numbers or in form of histograms.

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