ALICE trigger system for LHC Run 3

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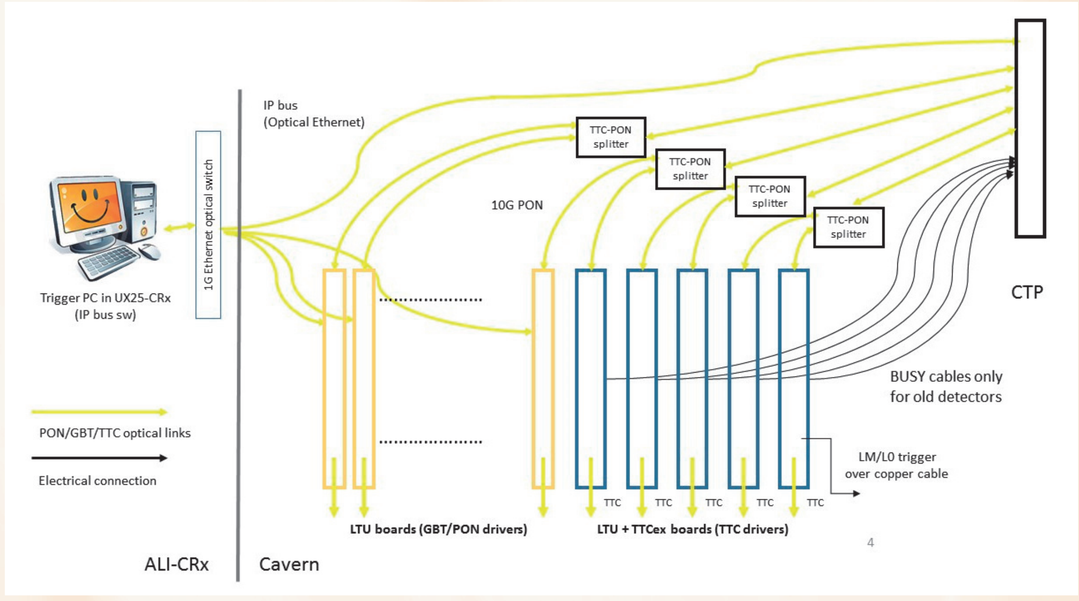
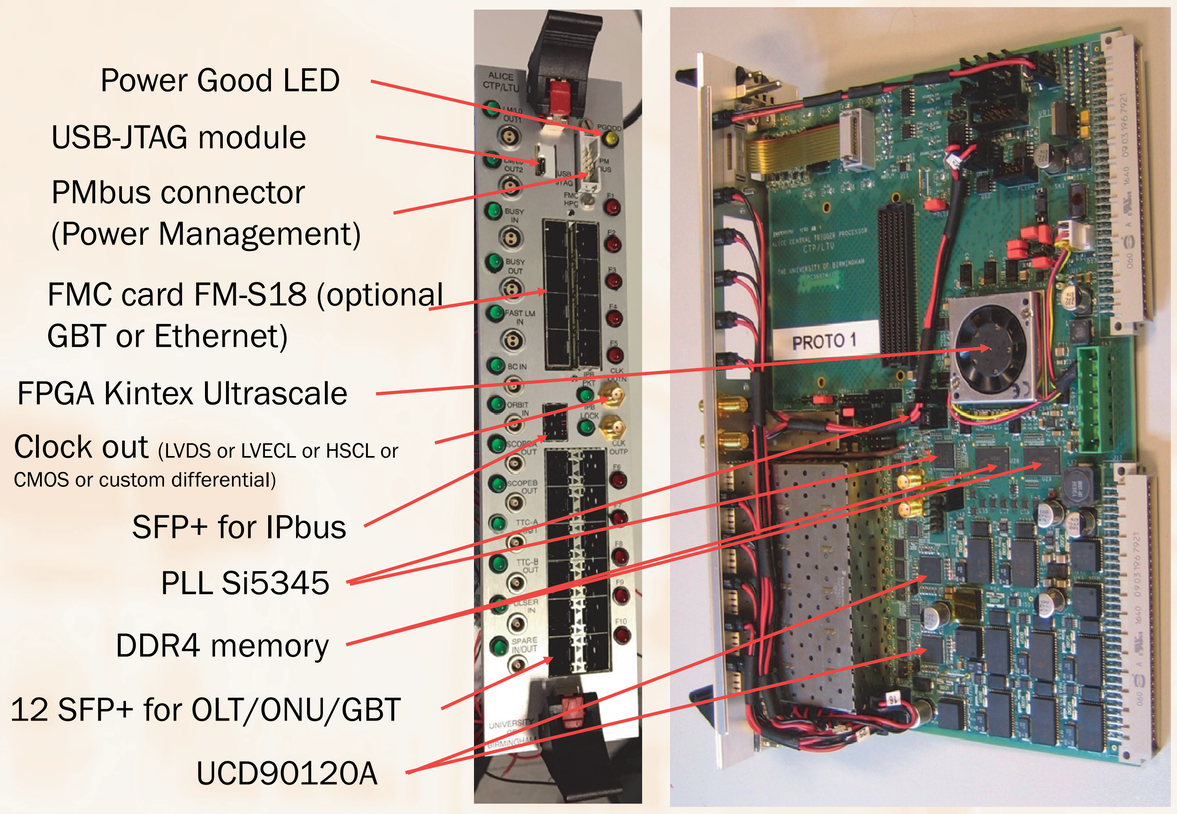
Introduction

In Run 3, the interaction rates at LHC Point 2 will increase to 50 kHz for Pb-Pb, and 200 kHz for p-p and p-A. In addition, where feasible a safety margin of two is applied in the system design. The aim of the ALICE trigger system is to select essentially all of these interactions. The new ALICE Central Trigger Processor (CTP) will be based on three trigger latencies (LM at 650 ns, L0 at 900 ns and L1 at 6.5 μs) with regular “Heartbeat” (HB) triggers for detectors running in continuous mode. The trigger system must also cope with old detectors that still have dead-time during the readout. The ALICE CTP is going to be upgraded for LHC Run 3 with completely new hardware and a new Trigger and Timing Control system based on a Passive Optical Network (TTC-PON) system. Some detectors will get the triggers also via a GBT system directly to their detector electronics in order to have a lower trigger latency. The new trigger system has been designed to be dead time free and able to transmit trigger data at 9.6 Gbps. A new universal trigger board has been designed where, by changing the FMC card, it can function as a CTP or as a LTU.



Schematic layout of new trigger system

The Prototype CTP/LTU Board



Photos of prototype CTP/LTU board

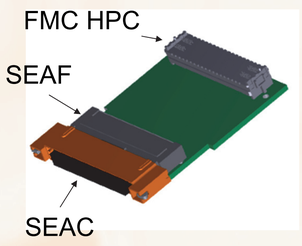
CTP/LTU board is designed as a 6U VME format with a front panel of 12HP width (3 VME slots), but it takes only +5V/10A and ±12V/1A from the VME bus. It is based on the Xilinx Kintex Ultrascale FPGA (XCKU040FFVA1156), 2 x 1GB DDR4 memory, 2 x Si5345 PLL, FMC HPC connector, 2x6 SFP+ cage, a single SFP+ cage, 2 x power controller UCD90120A and several DC-DC converters. CTP/LTU design is compatible also with XCKU060FFVA1156 FPGA. It provides also a high quality clock on two SMA outputs.

Available interfaces on the board are:

- USB-JTAG (JTAG access to FPGA and FMC card)
- IPbus (main control and monitoring for the CTP/LTU board)
- DDR4 (snap-shot memory and trigger data generator)
- TTC-PON (clock and trigger distribution based on Passive Optical Network (PON) system)
- TTC (old Trigger and Timing Control system)
- GBT (LAT-OPT, clock and trigger distribution directly to detector FEE)
- I2C (access to PLL Si5345, SFP plug-in modules : AFBR-709DMZ, LTF7222, LTF7221)
- SPI (access to Flash memory N25Q128)
- Power Management (reading voltages, currents and alerts for different conditions)

FMC CTP card

The FMC CTP card is designed with a Samtec SAEF connector and 70 LVDS repeaters, configurable as input or output in groups of 4. A configuration and serial number of the card will be stored in EEPROM.



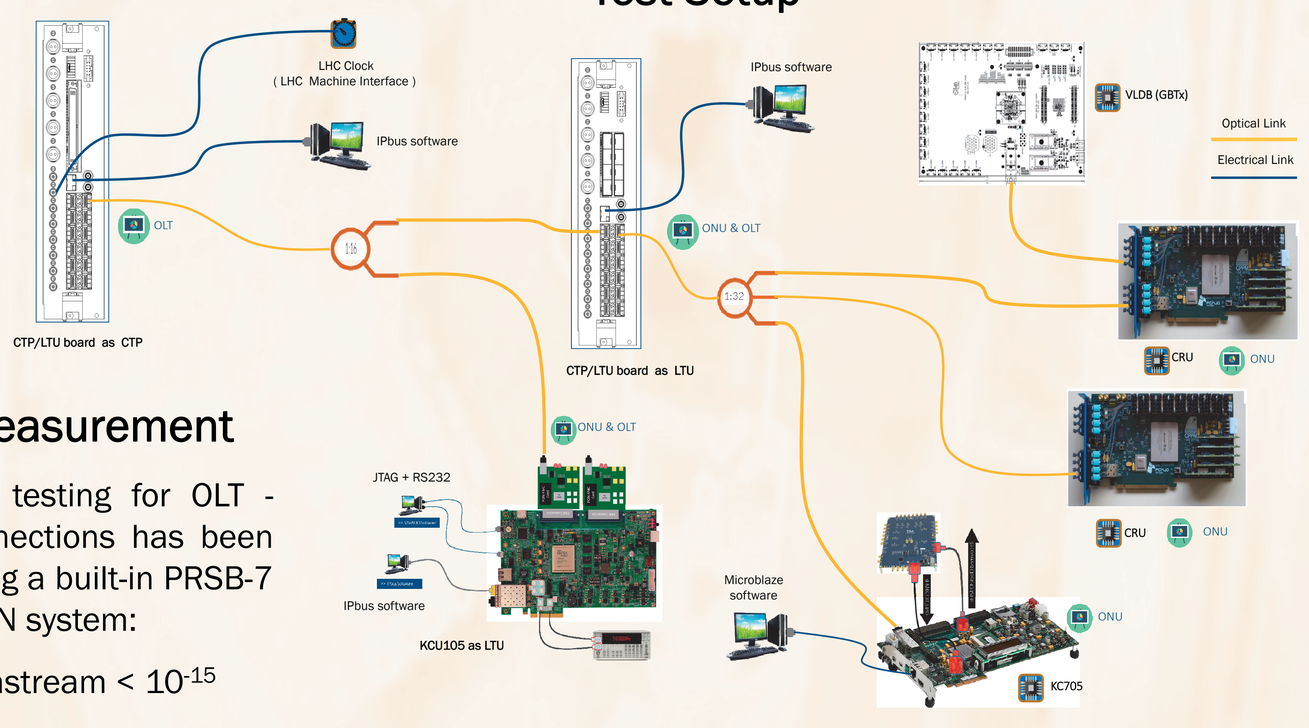
FMC CTP card

Standalone version

The CTP/LTU board will also be produced as a standalone unit, for detector laboratories, based on an ELMA Guardbox 33 case 3 and two AC-DC power supplies +12V/10A and -5V/3A.

ELMA Guardbox for CTP/LTU board

Test Setup



BER measurement

The BER testing for OLT - ONU connections has been done using a built-in PRSB-7 in TTC-PON system:

BER downstream < 10^{-15}

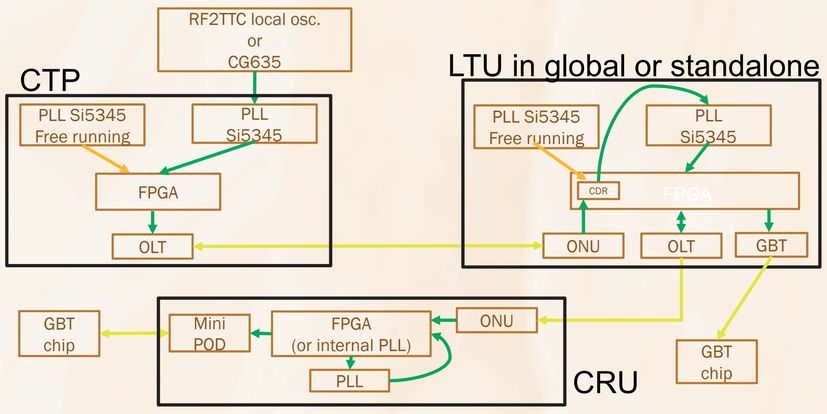
BER upstream < 10^{-14}

Stability of fixed latency measurement

	Tj (BER-12)	Rj	Dj	Pj
RF2TTC local osc.	149.42 ps	2.24 ps	117.54 ps	72.04 ps
CTP Si5345 out	62.14 ps	1.21 ps	44.94 ps	21.88 ps
LTU recovered clk from ONU	438.36 ps	25.88 ps	69.23 ps	137.44 ps
LTU Si5345 out	42.10 ps	1.64 ps	18.78 ps	19.75 ps
CRU Aria10 internal PLL				
GBTx elink0	298.95 ps	13.00 ps	113.53 ps	101.91 ps

	Tj (BER-12)	Rj	Dj	Pj
CG635	110.02 ps	7.72 ps	91 fs	7.40 ps
CTP Si5345 out	17.21 ps	1.20 ps	163 fs	1.93 ps
LTU recovered clk from ONU	340.09 ps	17.62 ps	88.85 ps	134.52 ps
LTU Si5345 out	17.42 ps	1.21 ps	181 fs	2.54 ps
CRU Aria10 internal PLL				
GBTx elink0	144.99 ps	9.21 ps	13.67 ps	31.95 ps

Clock jitter measurement in the full chain



Clock path in the trigger system

Summary

A new trigger system has been developed for the ALICE experiment for Run 3 of the LHC. The system utilises a universal trigger board (CTP/LTU board), based on the Xilinx Kintex Ultrascale FPGA. Testing of the prototype boards has been a successful and first phase of the board production will begin later this month.