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ALICE Trigger System for LHC Run 3

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The ALICE Central Trigger Processor (CTP) is going to be upgraded for LHC Run 3 with completely new hardware and a new Trigger and Timing Control (TTC) system based on a Passive Optical Network (PON) system. The new trigger system has been designed as dead time free and able to transmit trigger data at 9.6 Gbps. A new universal trigger board has been designed, where by changing the FMC card, it can function as a CTP or as a LTU. It is based on the Xilinx Kintex Ultrascale FPGA and upgraded TTC-PON.

Summary

In LHC Run 3 the interaction rates at point 2 will increase to 50 kHz for Pb-Pb, and 200 kHz for p-p and p-A. In addition, where feasible a safety margin of two is applied in the system design. The aim of the ALICE trigger system is to select essentially all of these interactions. The new ALICE CTP will be based on 3 trigger levels (LM at 650 ns, L0 at 900 ns and L1 at 6.5 µs) with regular "Heartbeat" (HB) triggers for detectors running in continuous mode. The trigger system must also cope with detectors that still have dead-time during the readout. It is based on the Xilinx Kintex Ultrascale FPGA and it has several interfaces: upgraded TTC-PON, GBT, IPbus, I2C, SPI and also the original TTC. The board is equipped with 2 DDR4 memories (each 1 GB) and it can be equipped with a maximum of 20 SFP+ modules. A complex power system on the board is controlled by a UCD90120A power sequencer and is monitored via PMbus. The main interface between the LTU and the CRU (Common Readout Unit) will be TTC-PON, but the ITS and MFT detectors will also receive triggers directly at their FEE via GBT (in parallel to CRU via TTC-PON) due to a trigger latency constraints. The interface between the CTP and the LTU is also based on TTC-PON. The LTU will collect all BUSY signals (TTC-PON time multiplexed upstream) from the detectors and forward them to the CTP where an overall BUSY mask will be built. The new trigger system and the prototype of the trigger board will be presented.

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