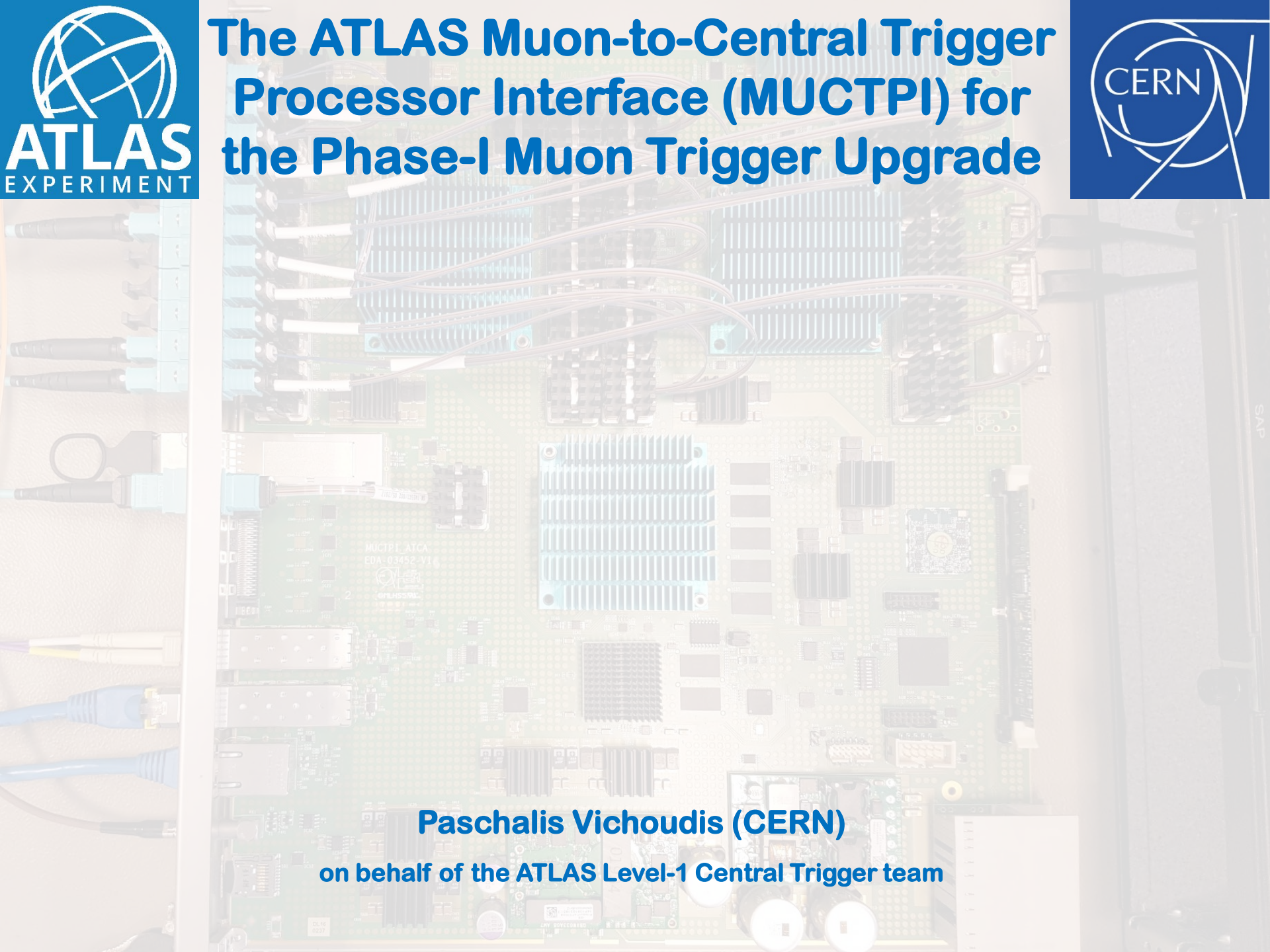
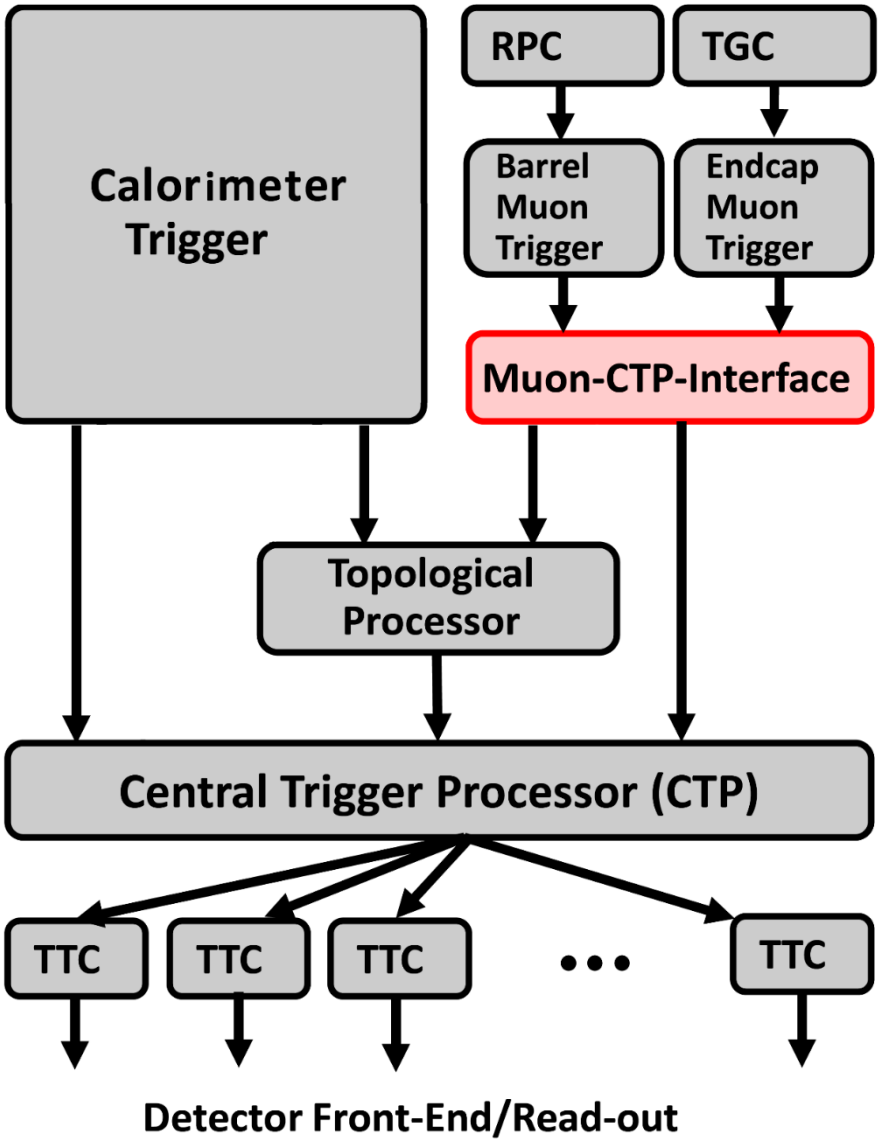
The ATLAS Muon-to-Central Trigger Processor Interface (MUCTPI) for the Phase-I Muon Trigger Upgrade



Paschalis Vichoudis (CERN)

on behalf of the ATLAS Level-1 Central Trigger team

The ATLAS Level-1 Trigger System



* *TTC: Timing, Trigger and Control*

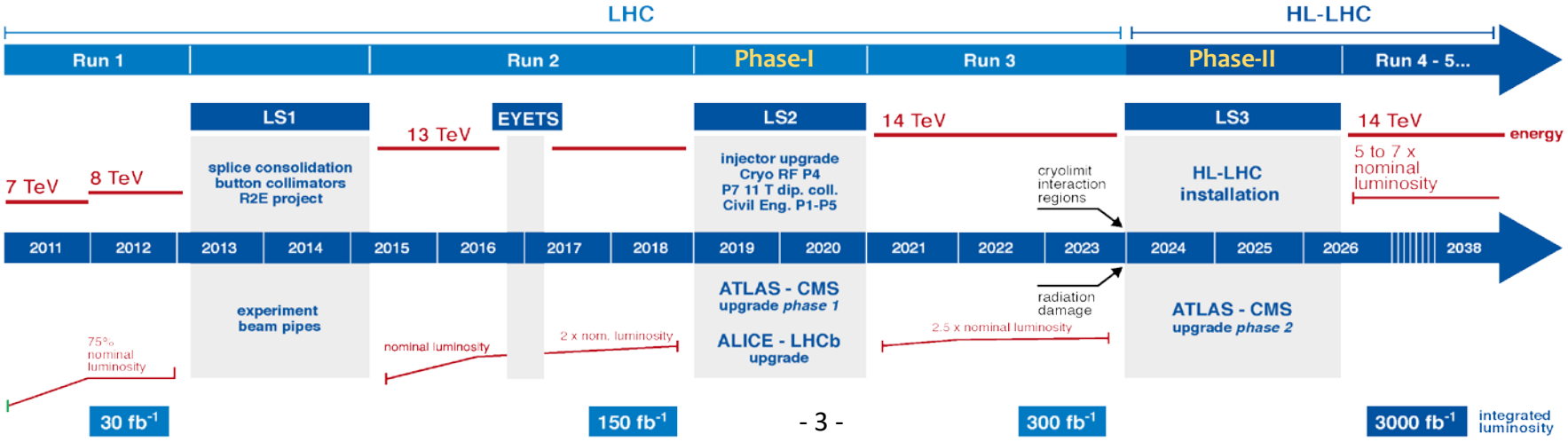
MUCTPI functionality

- Receives muon candidates from each of the 208 muon sectors (64 in the barrel region and 144 in the endcap region) at the bunch crossing rate (40MHz)
- Counts muon candidates for each p_T threshold and sends the number of muons ("multiplicity") to the CTP
- Avoids double counting of single muons that are detected by more than one muon sector due to geometrical overlap of the muon chambers and the trajectory of the muon in the magnetic field ("overlap handling")
- Sends muon candidate information to Topological Processor (L1Topo)

MUCTPI Upgrade

- MUCTPI upgrade is part of the overall trigger upgrade on the road to the HL-LHC
  - Upgrade in line with development of New Small Wheel (NSW) of muon trigger system
  - To be deployed in LS2 (2019-2020)

- Required improvements to MUCTPI
  - Increase the bandwidth by using optical links
    - Allow for new/more information from the sector logic (more candidates, more precise position information etc.)
    - Electrical connections bulky and difficult to maintain
  - Send full-precision information on muon candidates to L1Topo
  - Fit within the same tight latency requirement (8 BC = 200 ns)
  - Designed to be compatible with the Phase-II upgrade



MUCTPI Implementation

Optical input/output

High-density ribbon fiber optical transmitters/receivers:

- Avago MiniPOD: 12-way, up to 14 Gb/s, 18 x 22 mm

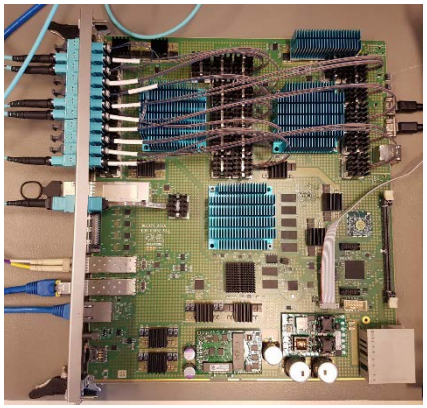
High performance processing

High-end FPGAs with >100 on-chip high-speed serial links:

- Xilinx UltraScale family selected (20 nm)
- Plan to migrate to UltraScale+ (16 nm) for production

ATCA form-factor

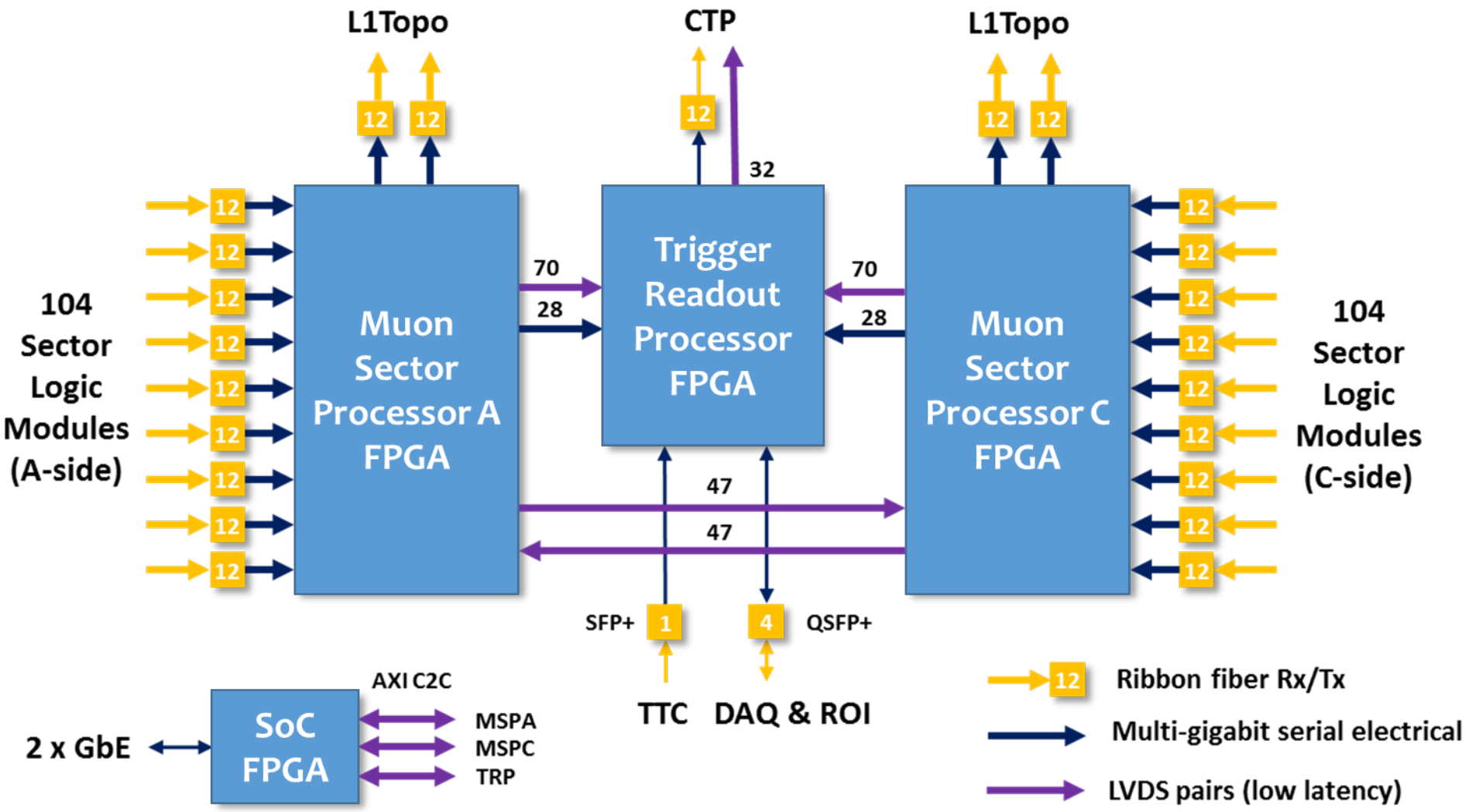
Improved cooling, power supply, board real-estate, hardware platform monitoring



➔ Enables MUCTPI functionality on a single board

Compared to 18 9U VME boards in a crate

MUCTPI Block Diagram



** SoC: System-on-Chip*

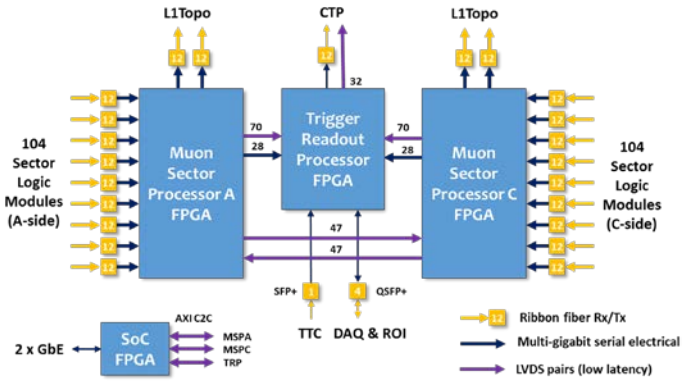
MUCTPI Functionality

2 Muon Sector Processor (MSP) FPGAs (Xilinx Virtex Ultrascale VU160)

- 1 FPGA handles ½ of the muon trigger
- Muon sector logic input: 9 MiniPOD receivers (104 MGT Rx)
- L1Topo output: 2 MiniPOD transmitters (24 MGT Tx)
- Muon sector data reception & timing alignment
- Overlap handling: suppress double counting of single muons
- Muon trigger object output to L1Topo
- Monitoring: rates & per-bunch histograms per sector
- On-chip playback & snapshot memories

Trigger/Readout Processor (TRP) FPGA (Xilinx Kintex Ultrascale KU095)

- Receive and merge information from 2 MSP FPGAs
- Calculate global muon candidate multiplicities
- Implement muon-only topological algorithms
- Send trigger multiplicities and flags to CTP
- DAQ readout, HLT output
- Event monitoring
- TTC reception, decoding and distribution



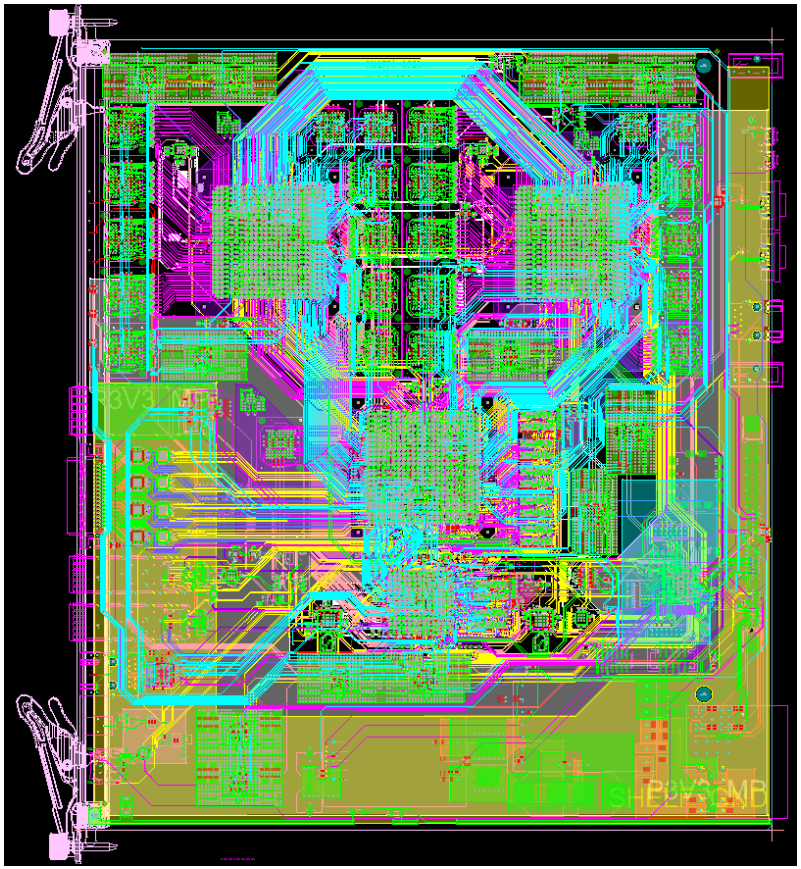
MUCTPI Layout

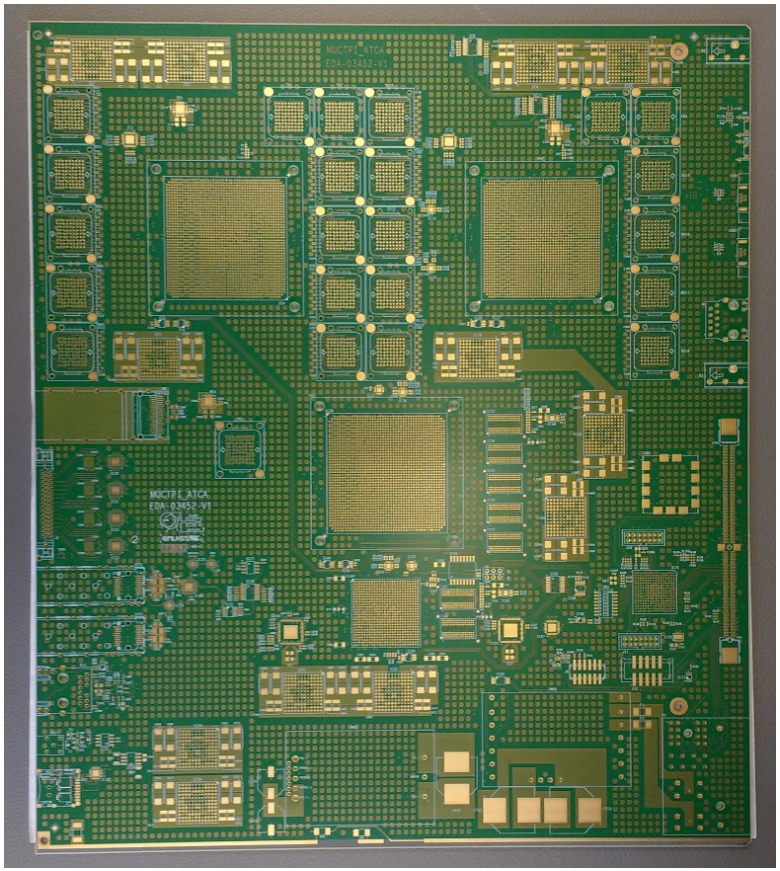
Routing

23 twelve-way miniPODs (18 Rx & 5 Tx)
3 x 2104-pin Ultrascale FPGAs
~330 MGT pairs (6.4 to 12.8 Gb/s)
~240 LVDS pairs (1.28 Gb/s)

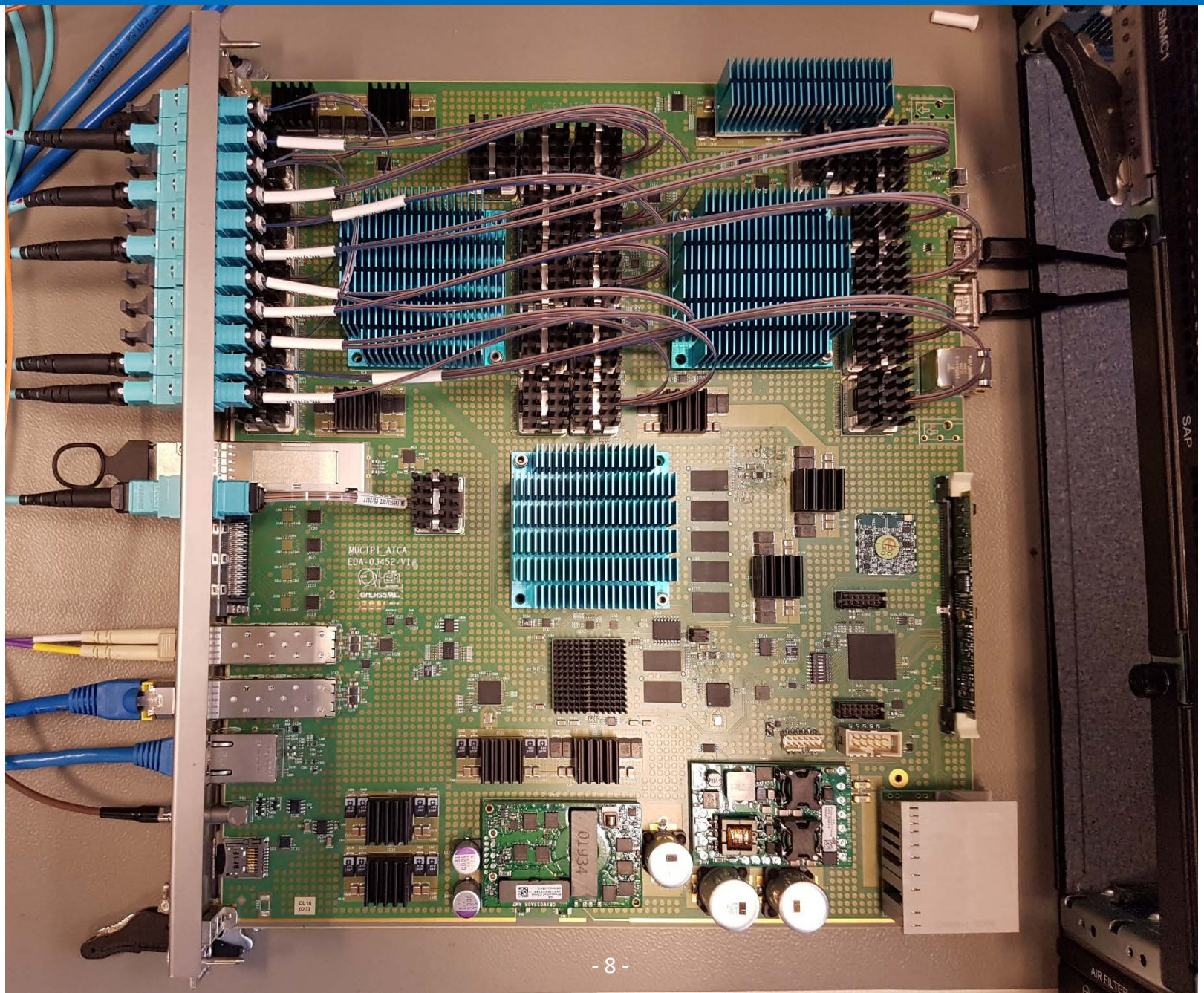
PCB

22-layer PCB
Megtron-6 low-loss dielectric
Blind vias for high-speed track layers





MUCTPI Prototype



MUCTPI Zynq System-on-Chip (SoC)

Zynq is a dual ARM core and FPGA programmable logic in one package

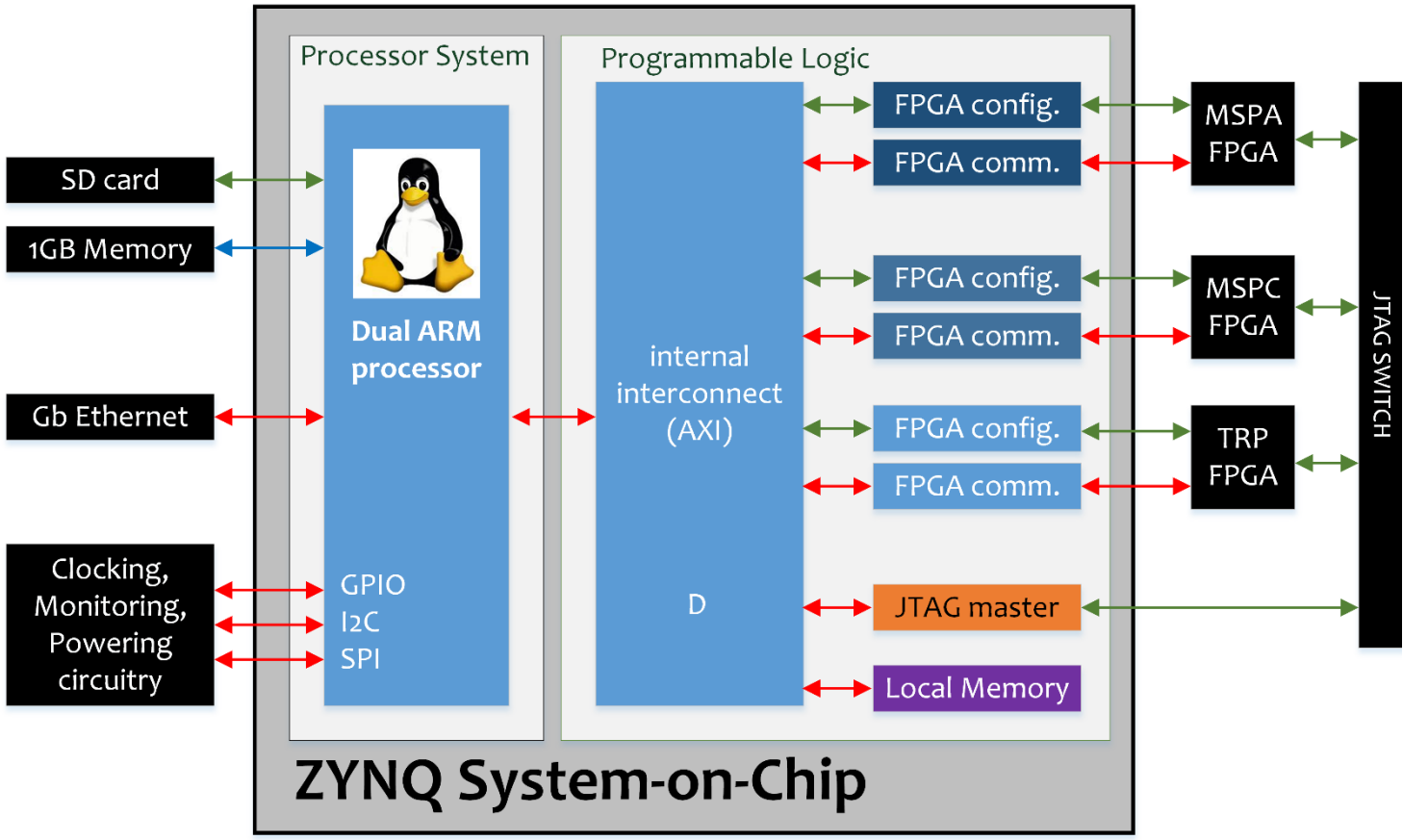
Running embedded Linux

Gigabit Ethernet (GbE) IP connection with a PC

Run Control functionality (i.e. control, configuration and monitoring)

FPGA bitstream download

On-board hardware monitoring (optical links, voltages, currents, temperatures etc.)



MUCTPI Inter-FPGA Communication

AXI Chip-to-Chip (C2C)

- Extension of the on-chip AXI bus outside the SoC
- Point-to-point interconnections, one per FPGA
- Less than 1 GPIO bank per FPGA (~36 I/Os @ 333Mb/s)
- Performance exceeds the GbE bandwidth to PC

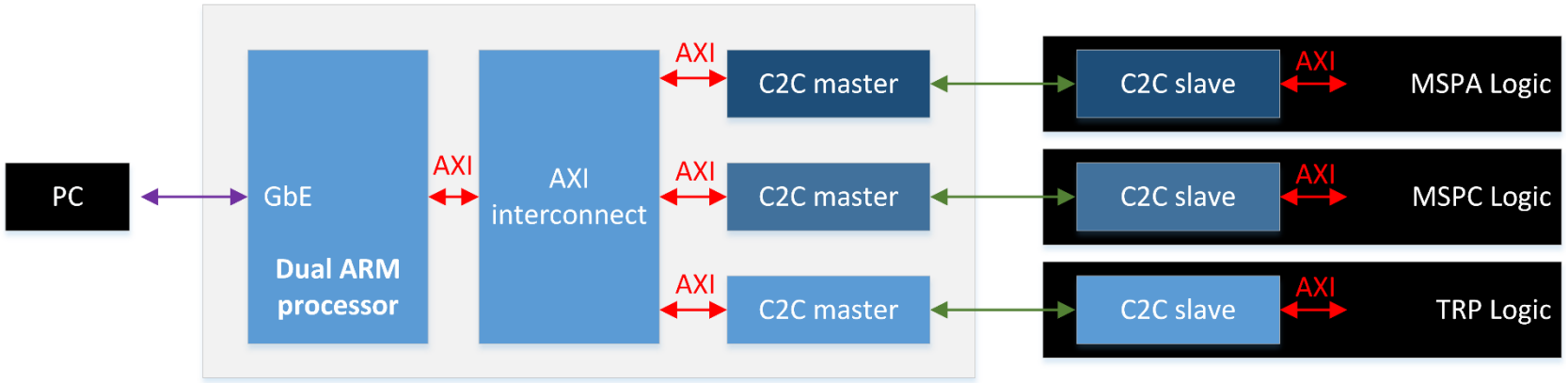
Performance

Block transfers

data size	performance	
block (KB)	local (MB/s)	c2c (MB/s)
1	43	41
2	64	62
4	111	101
8	180	149
16	270	199
32	355	247
64	426	277
128	472	295

Single word access

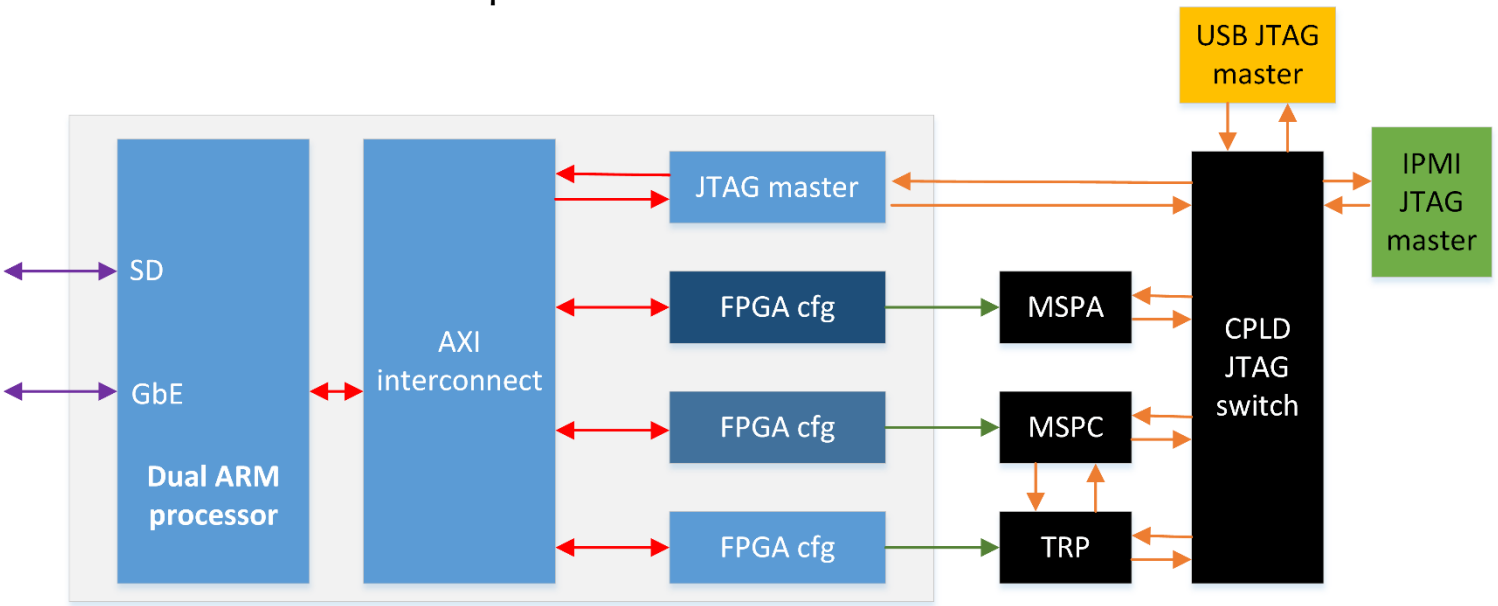
local (MB/s)	c2c (MB/s)
30	6



MUCTPI FPGA Configuration

Configuration scheme

- SoC boots via SD card / QSPI Flash / Ethernet
- No dedicated configuration memories for the Ultrascale FPGAs
- SoC configures the Ultrascale FPGAs via dedicated configuration controllers
  - Ultrascale FPGA bitfiles from SD card or Ethernet (200MB in total)
  - Less than 10 seconds total configuration time (via the Slave Serial protocol)
- USB-JTAG cable for initial debugging
- Virtual JTAG cable via Ethernet implemented in SoC



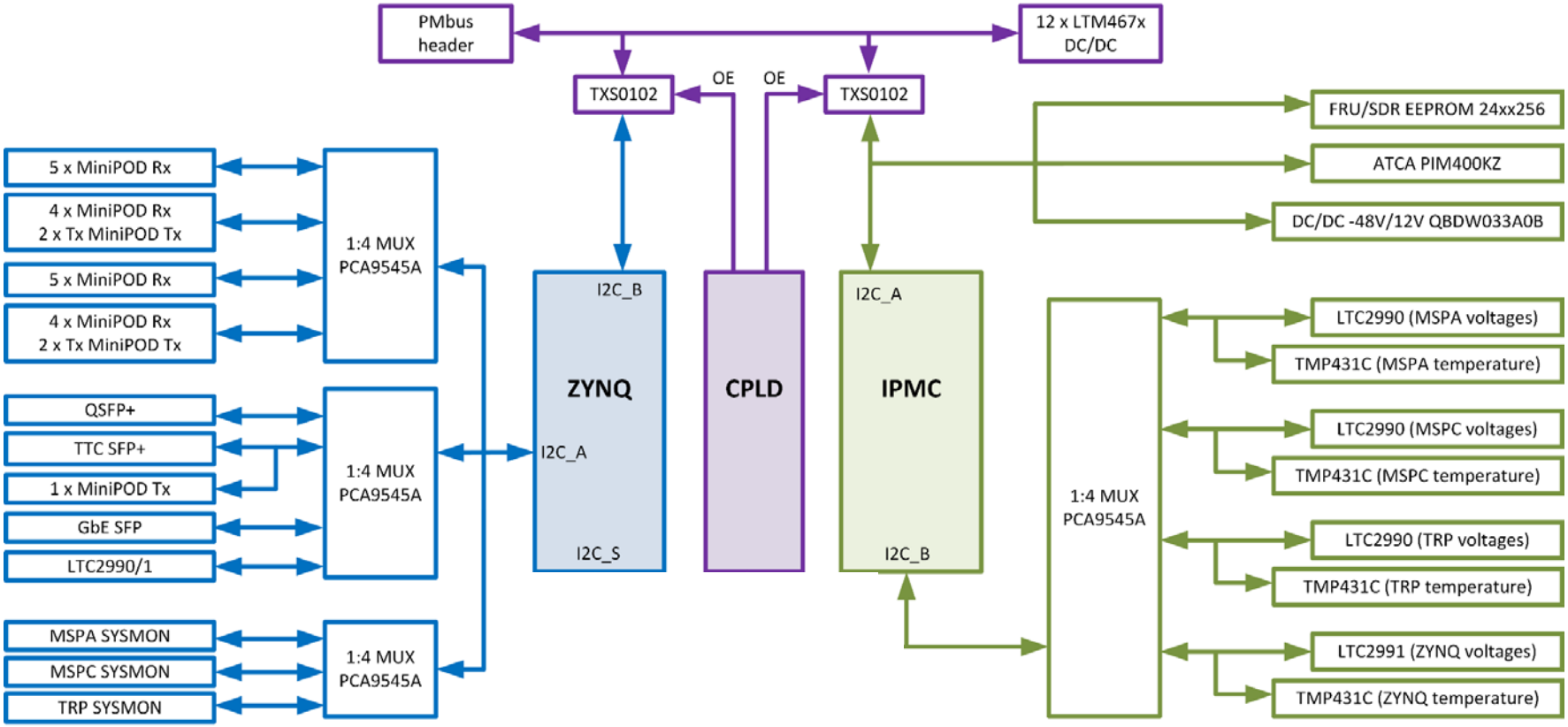
MUCTPI Hardware Monitoring

Hundreds of parameters monitored

- Temperature, Current, Voltages
- Optical receiver power
- Error conditions / alarms
- IC/module identification

Two independent monitoring paths

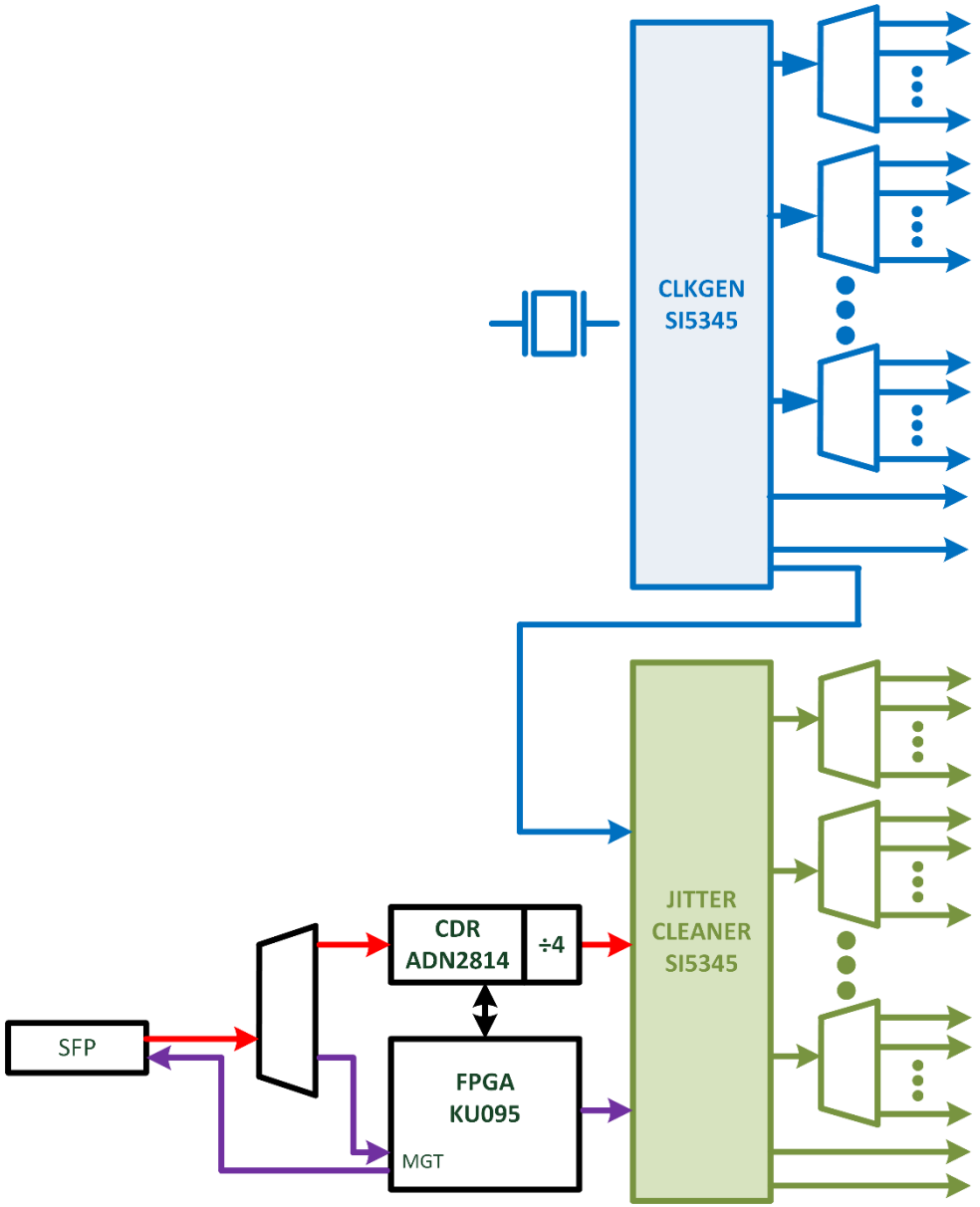
- via the ZYNQ SoC
- via IPMC and ATCA shelf manager using independent i2c sensor devices
- Same parameters monitored (however using different sensor devices)



MUCTPI Clocking

Flexible clock circuitry

- Two programmable 10-output clock chips (SI5345)
  - 1st used as free-running clock generator
  - 2nd used as zero-delay Jitter cleaner/ clock-multiplier synchronized with LHC clock
- Configured by the SoC through SPI
- Options for TTC reception
  - External circuitry based on dedicated CDR chip (ADN2814)
  - MGT Rx and associated firmware in TRP FPGA oversampling and recovering the TTC stream
- Confirmed fixed and deterministic latency for LHC clock
- Designed to be forward compatible with TTC-PON (to be tested)



MUCTPI Serial Links

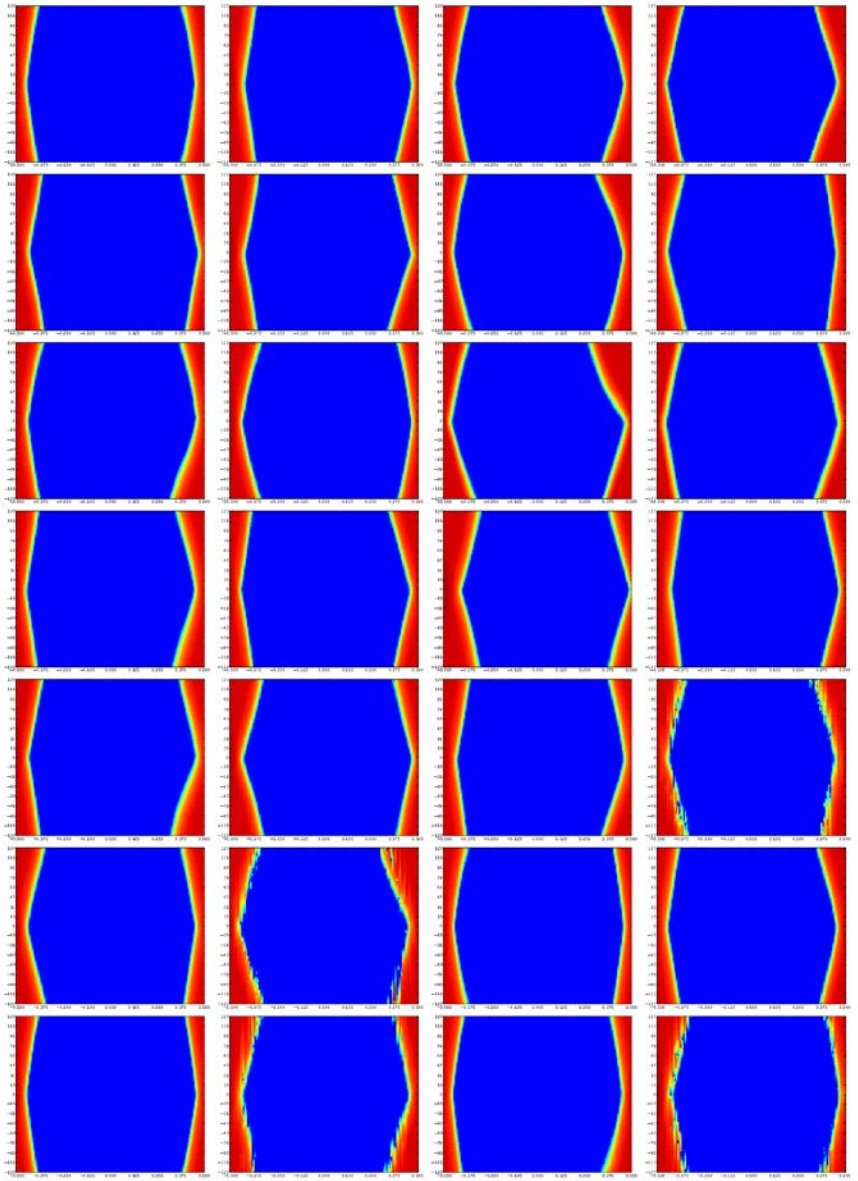
Multi-Gigabit serial links (~330)

- All tested successfully using the Xilinx Bit Error Rate Test tool (IBERT)
- Excellent performance at 6.4Gb/s with very wide eye opening (~75% of the duty cycle)
- Compatibility for future operation at 9.6 & 12.8 Gb/s confirmed
    - error-free operation of 100+ links at 12.8Gb/s for 10 days

Low latency LVDS serial links (~240)

- Error free operation at 1.28Gb/s
- Wide eye opening (avg. 70% of the duty cycle)

Example of eye diagrams at 6.4Gb/s



MUCTPI Power Supply

Input power: -48V DC -> 12V DC -> twelve point-of-load DC/DC converters

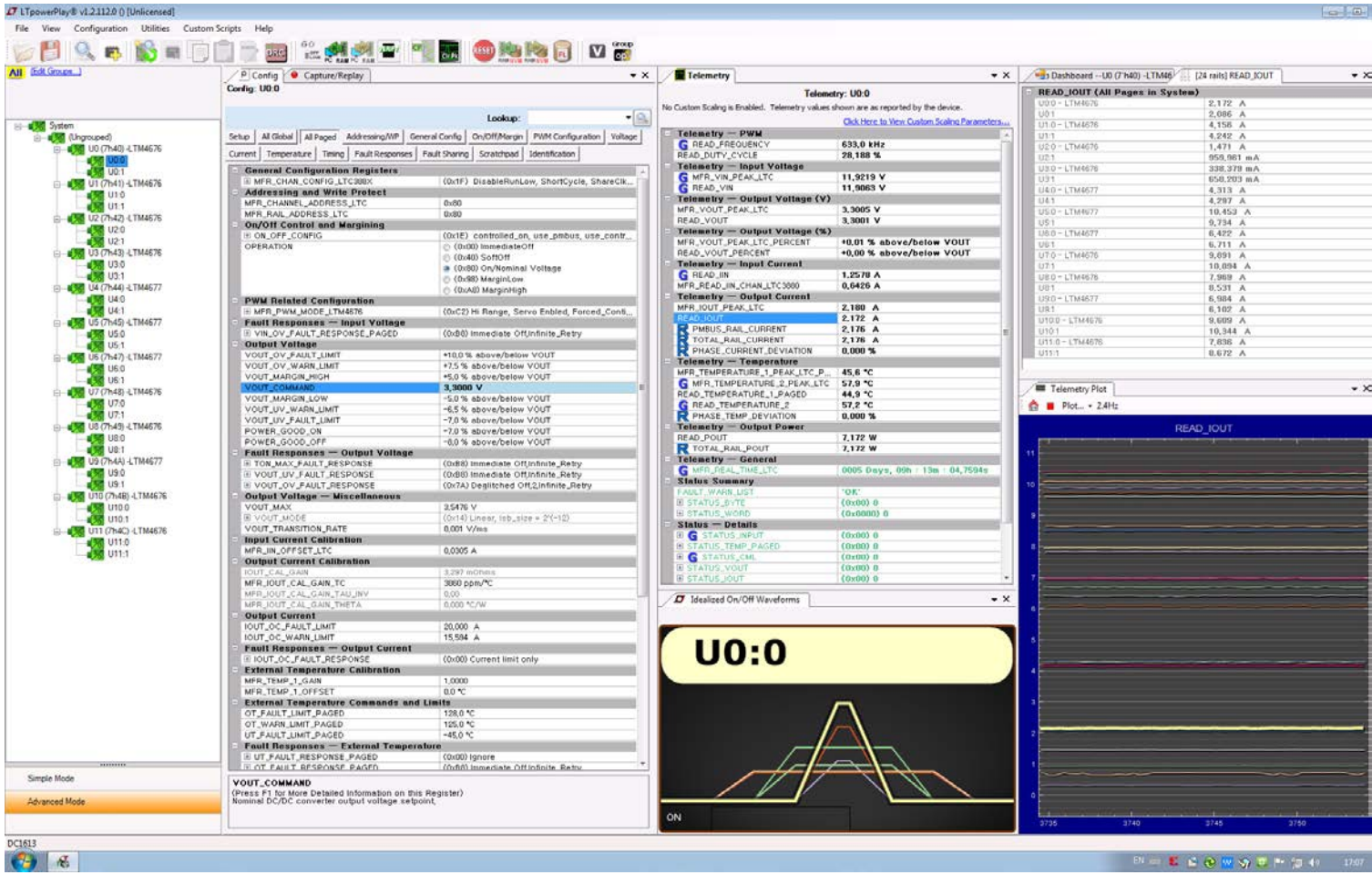
LTM467x family by Linear Technology

Dual DC/DC converters (13A or 18A per channel)

Control/monitoring through PMbus (voltage/current /sequencing etc)

GUI used for initial configuration & monitoring during test and debugging

PMbus accessible via the SOC to read voltage, current, temperature, alarms etc.



MUCTPI Power Consumption

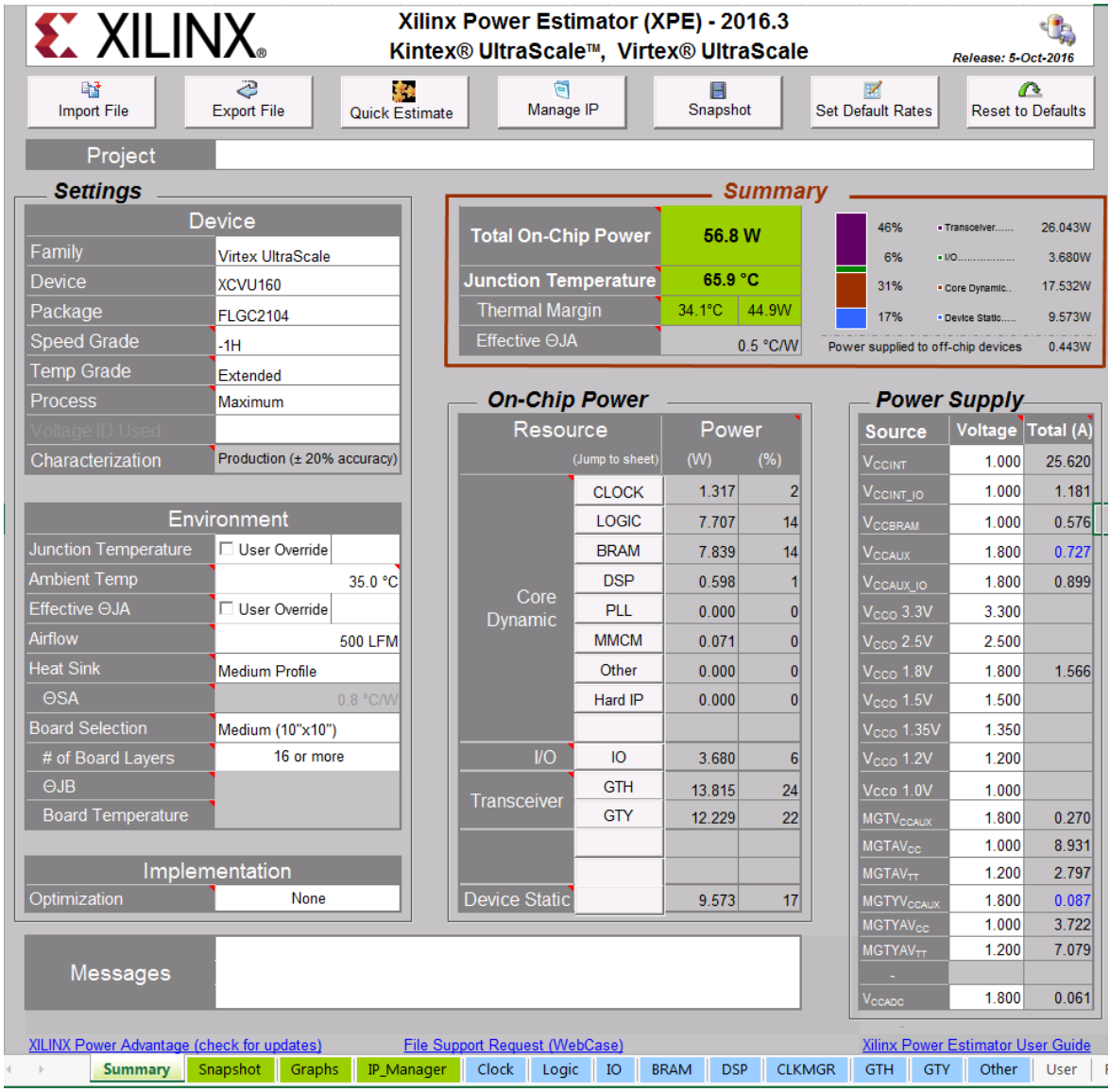
Estimated to be up to 300 Watts max (based on Xilinx Power Estimator)

200W consumption measured with all links running at 12.8Gb/s

ATCA platform supports up to 400W per board

Successful powering and heat dissipation tests using test firmware with all MGT links running and commercial passive heatsinks

Upgrade of some DC/DC converters with pin-compatible devices with higher current capabilities possible



MUCTPI Summary & Outlook

- Conceptual design, schematic entry and layout in 2016
- First fully assembled prototype received in Q2, 2017
- Another two partially assembled prototypes available for software development
- 95% of board features have been successfully tested
  - Only minor fixes required to the board
- Smooth bring-up of Zynq-based SoC thanks to extensive preparatory work with development kits
- Plan to upgrade MSP FPGAs to pin-to-pin compatible Ultrascale+ device (VU9P) for additional memory/logic resources for production modules

Thank you