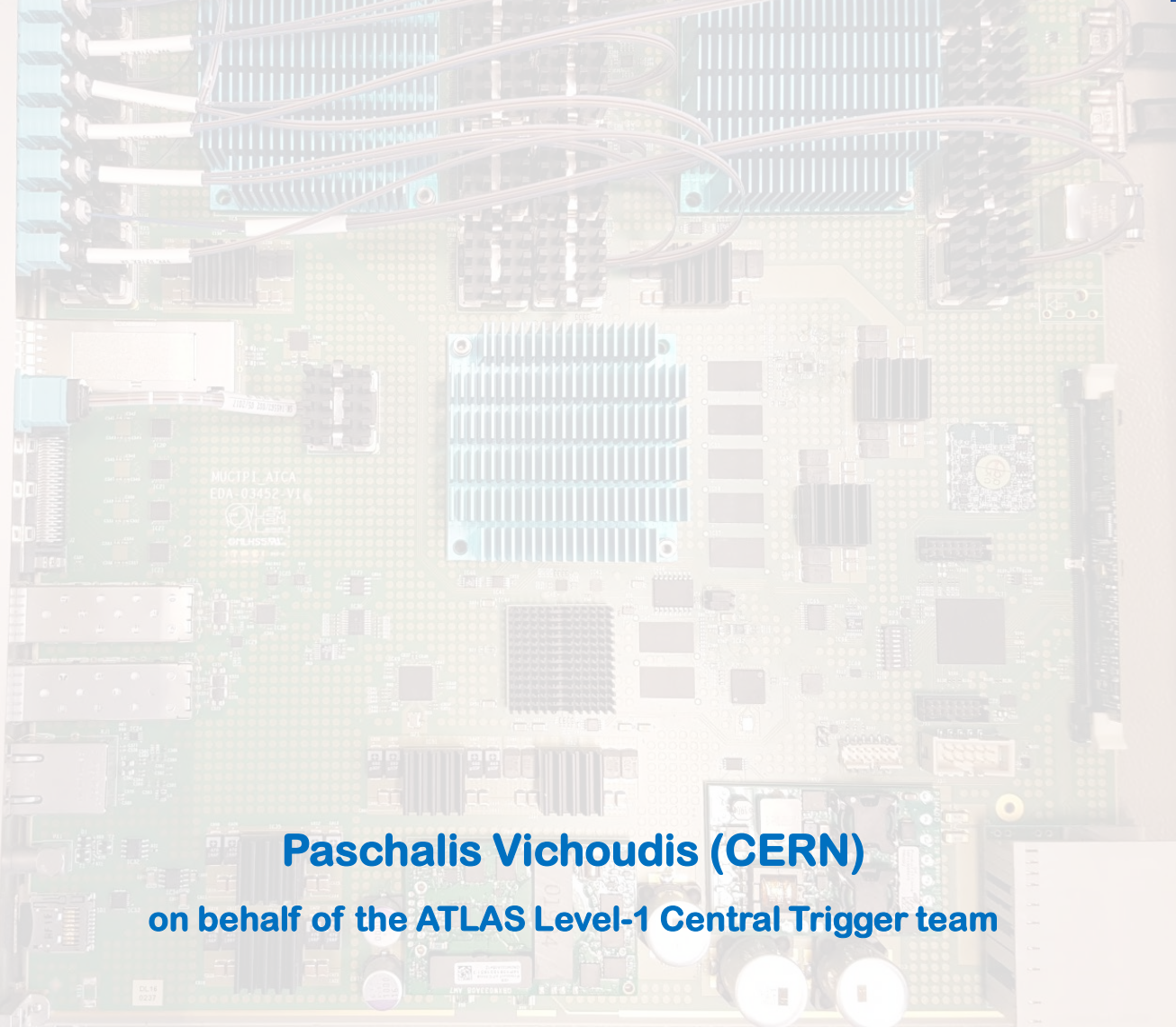


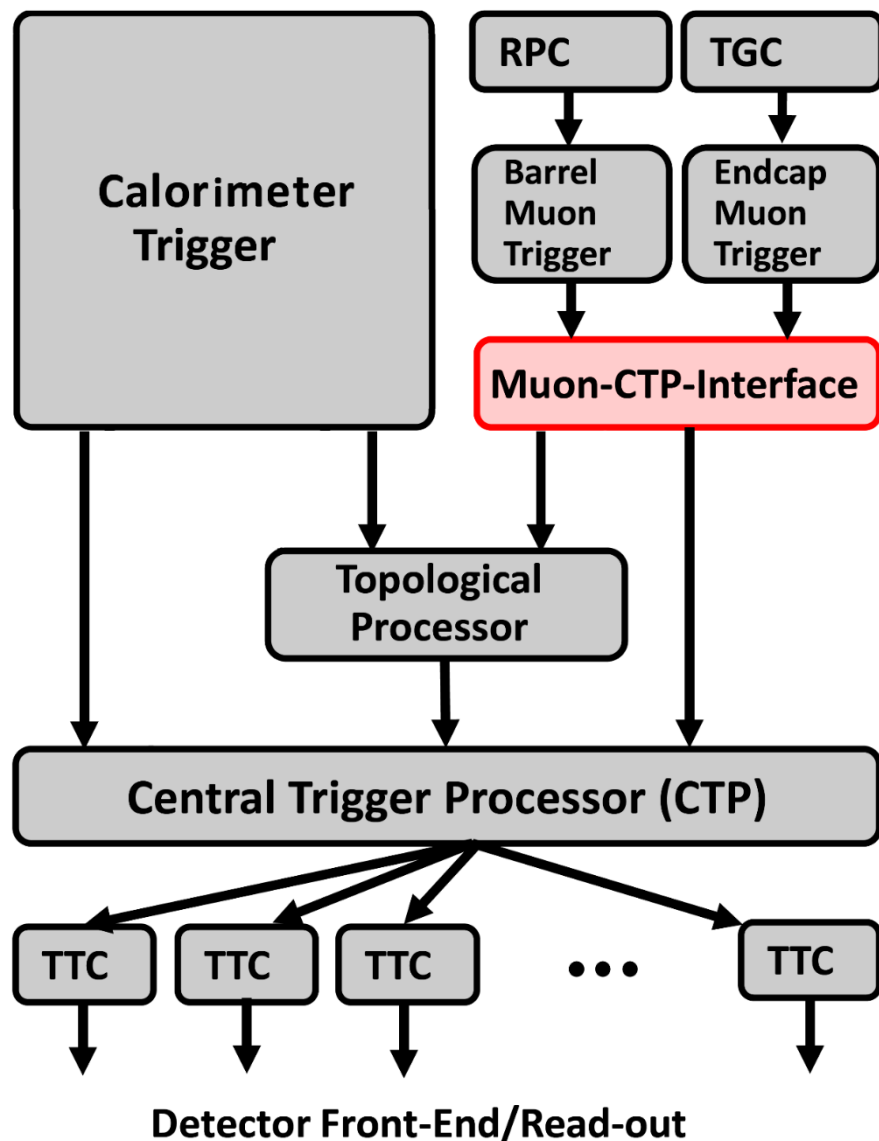
# The ATLAS Muon-to-Central Trigger Processor Interface (MUCTPI) for the Phase-I Muon Trigger Upgrade



**Paschalis Vichoudis (CERN)**

on behalf of the ATLAS Level-1 Central Trigger team

# The ATLAS Level-1 Trigger System



\* TTC: Timing, Trigger and Control

## MUCTPI functionality

- Receives **muon candidates** from each of the 208 muon sectors (64 in the barrel region and 144 in the endcap region) at the bunch crossing rate (40MHz)
- Counts muon candidates for each  **$p_T$  threshold** and sends the number of muons (“**multiplicity**”) to the CTP
- Avoids **double counting** of single muons that are detected by more than one muon sector due to geometrical overlap of the muon chambers and the trajectory of the muon in the magnetic field (“**overlap handling**”)
- Sends muon **candidate information** to Topological Processor (**L1Topo**)

# MUCTPI Upgrade

- MUCTPI upgrade is part of the overall trigger upgrade on the road to the HL-LHC
  - Upgrade in line with development of New Small Wheel (NSW) of muon trigger system
  - To be deployed in LS2 (2019-2020)
- Required improvements to MUCTPI
  - Increase the bandwidth by using optical links
    - Allow for new/more information from the sector logic (more candidates, more precise position information etc.)
    - Electrical connections bulky and difficult to maintain
  - Send full-precision information on muon candidates to L1Topo
  - Fit within the same tight latency requirement (8 BC = 200 ns)
  - Designed to be compatible with the Phase-II upgrade





# MUCTPI Implementation

## Optical input/output

High-density ribbon fiber optical transmitters/receivers:

Avago MiniPOD: 12-way, up to 14 Gb/s, 18 x 22 mm



## High performance processing

High-end FPGAs with >100 on-chip high-speed serial links:

Xilinx UltraScale family selected (20 nm)

Plan to migrate to UltraScale+ (16 nm) for production

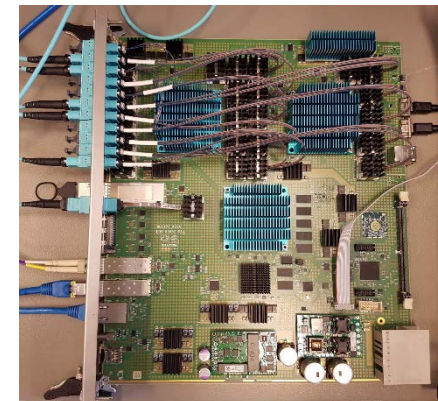


## ATCA form-factor

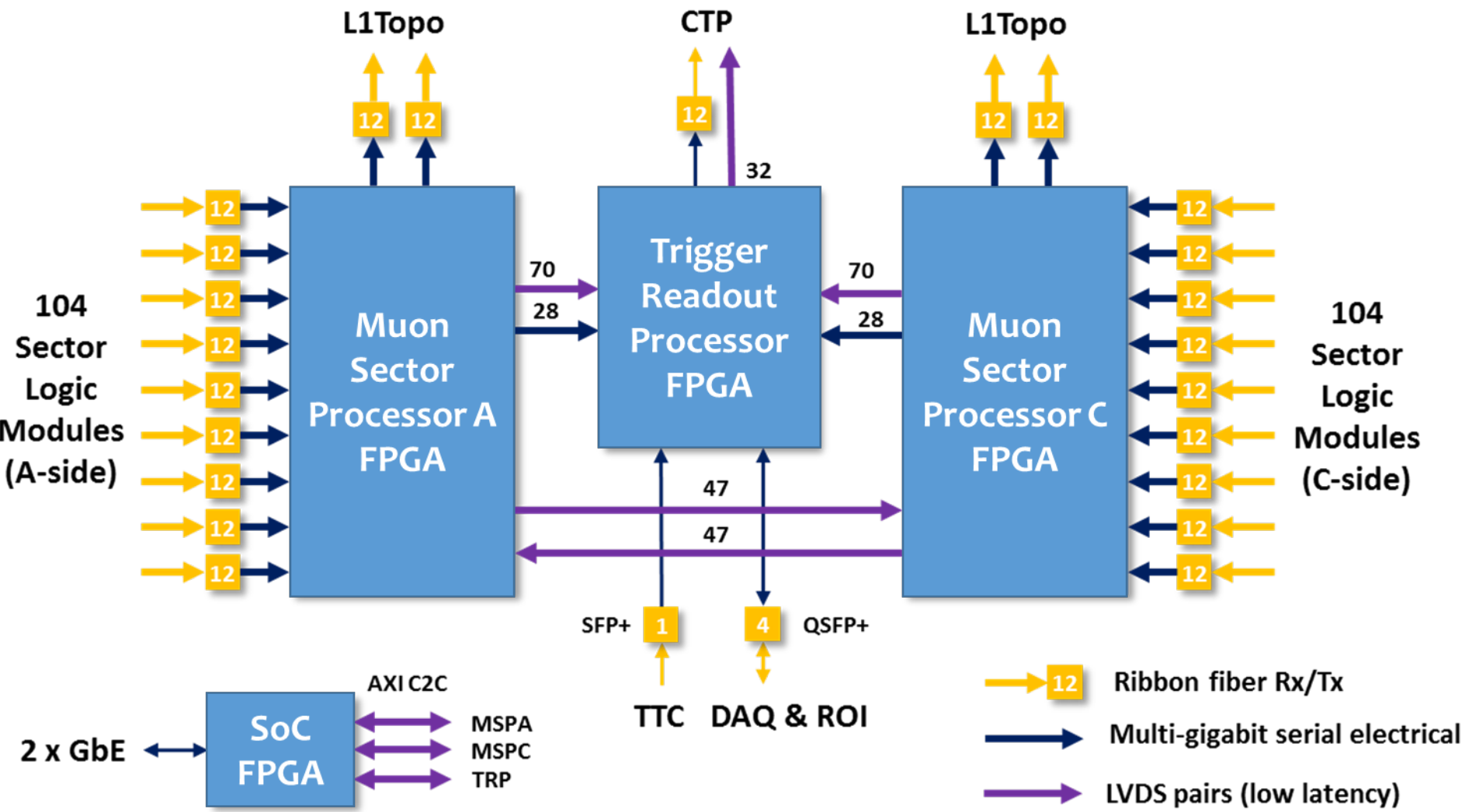
Improved cooling, power supply, board real-estate, hardware platform monitoring

➔ Enables MUCTPI functionality on a single board

Compared to 18 9U VME boards in a crate



# MUCTPI Block Diagram



\* SoC: System-on-Chip

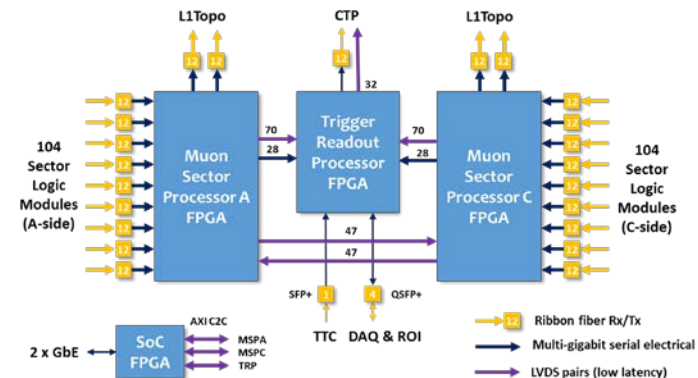
# MUCTPI Functionality

## 2 Muon Sector Processor (MSP) FPGAs (Xilinx Virtex Ultrascale VU160)

- 1 FPGA handles  $\frac{1}{2}$  of the muon trigger
- Muon sector logic input: 9 MiniPOD receivers (104 MGT Rx)
- L1Topo output: 2 MiniPOD transmitters (24 MGT Tx)
- Muon sector data reception & timing alignment
- Overlap handling: suppress double counting of single muons
- Muon trigger object output to L1Topo
- Monitoring: rates & per-bunch histograms per sector
- On-chip playback & snapshot memories

## Trigger/Readout Processor (TRP) FPGA (Xilinx Kintex Ultrascale KU095)

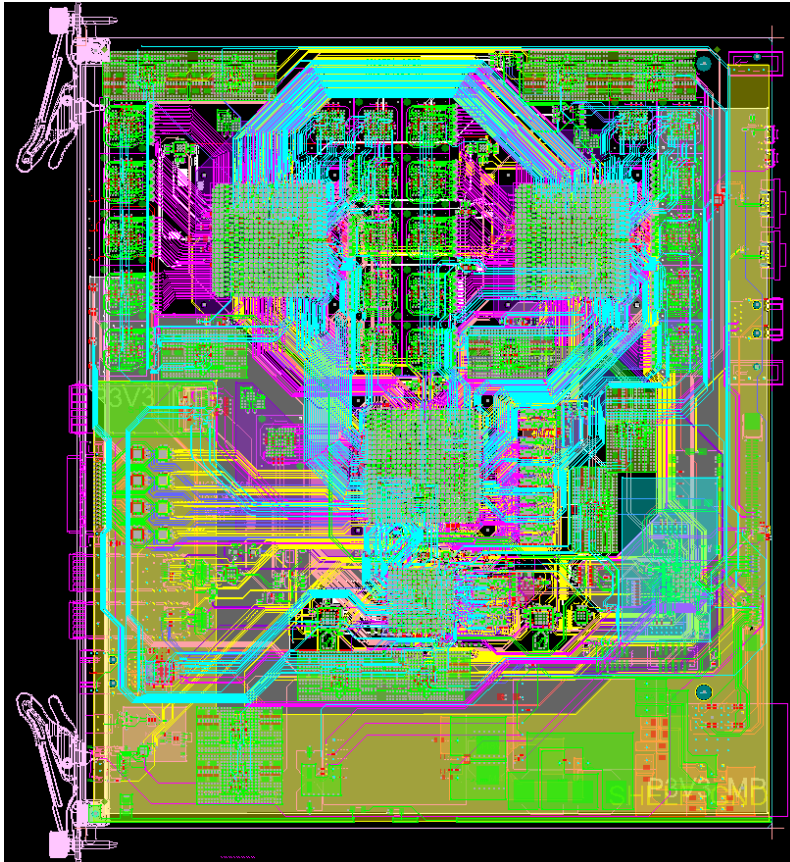
- Receive and merge information from 2 MSP FPGAs
- Calculate global muon candidate multiplicities
- Implement muon-only topological algorithms
- Send trigger multiplicities and flags to CTP
- DAQ readout, HLT output
- Event monitoring
- TTC reception, decoding and distribution



# MUCTPI Layout

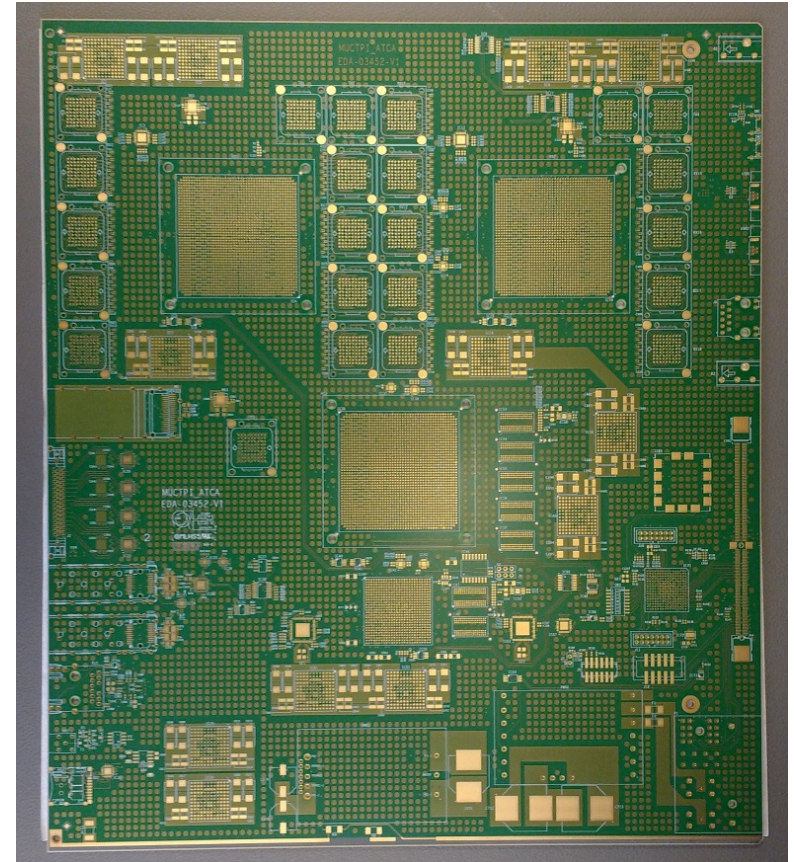
## Routing

- 23 twelve-way miniPODs (18 Rx & 5 Tx)
- 3 x 2104-pin Ultrascale FPGAs
- ~330 MGT pairs (6.4 to 12.8 Gb/s)
- ~240 LVDS pairs (1.28 Gb/s)



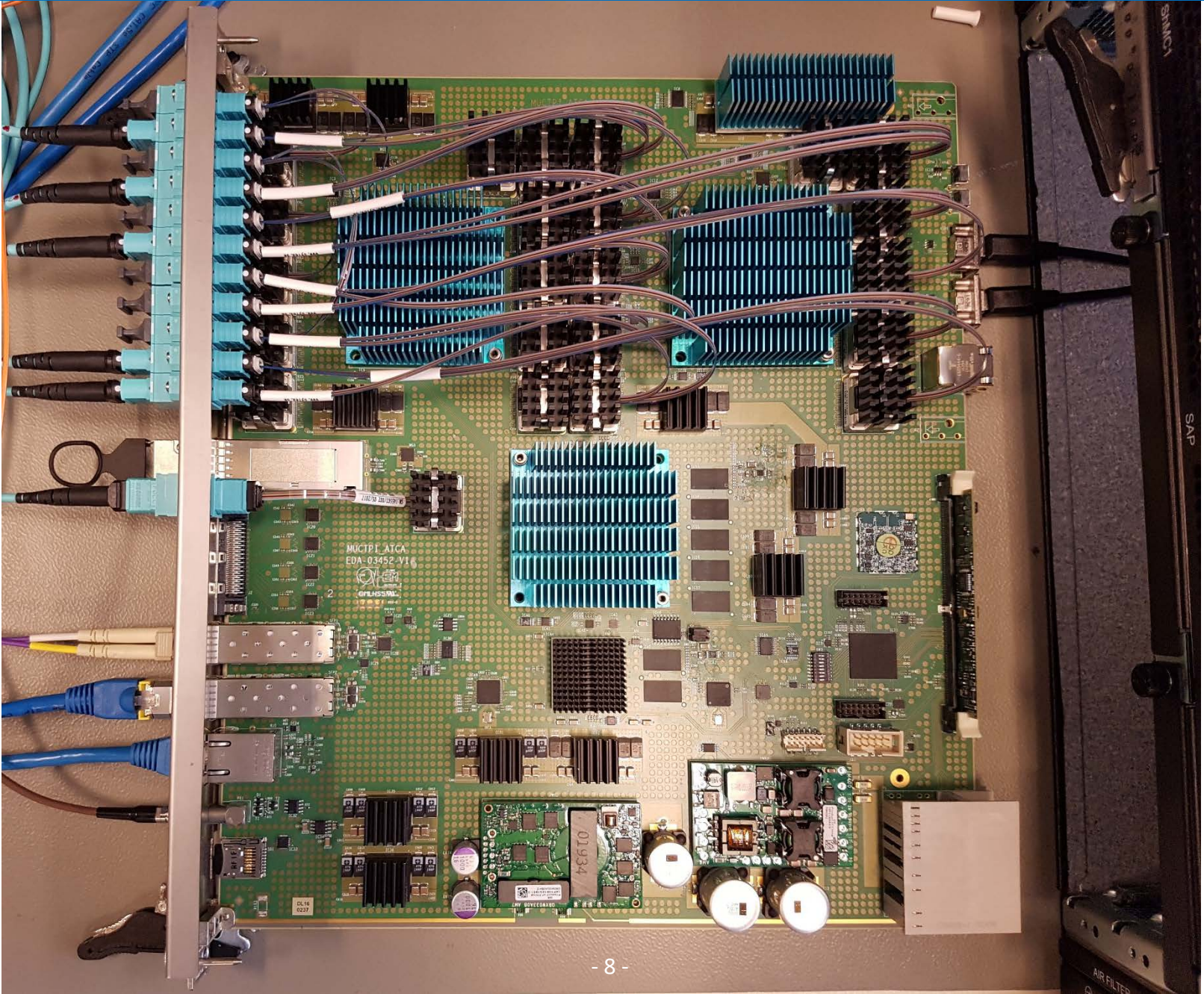
## PCB

- 22-layer PCB
- Megtron-6 low-loss dielectric
- Blind vias for high-speed track layers





# MUCTPI Prototype





# MUCTPI Zynq System-on-Chip (SoC)

Zynq is a dual ARM core and  
FPGA programmable logic in  
one package

Running embedded Linux

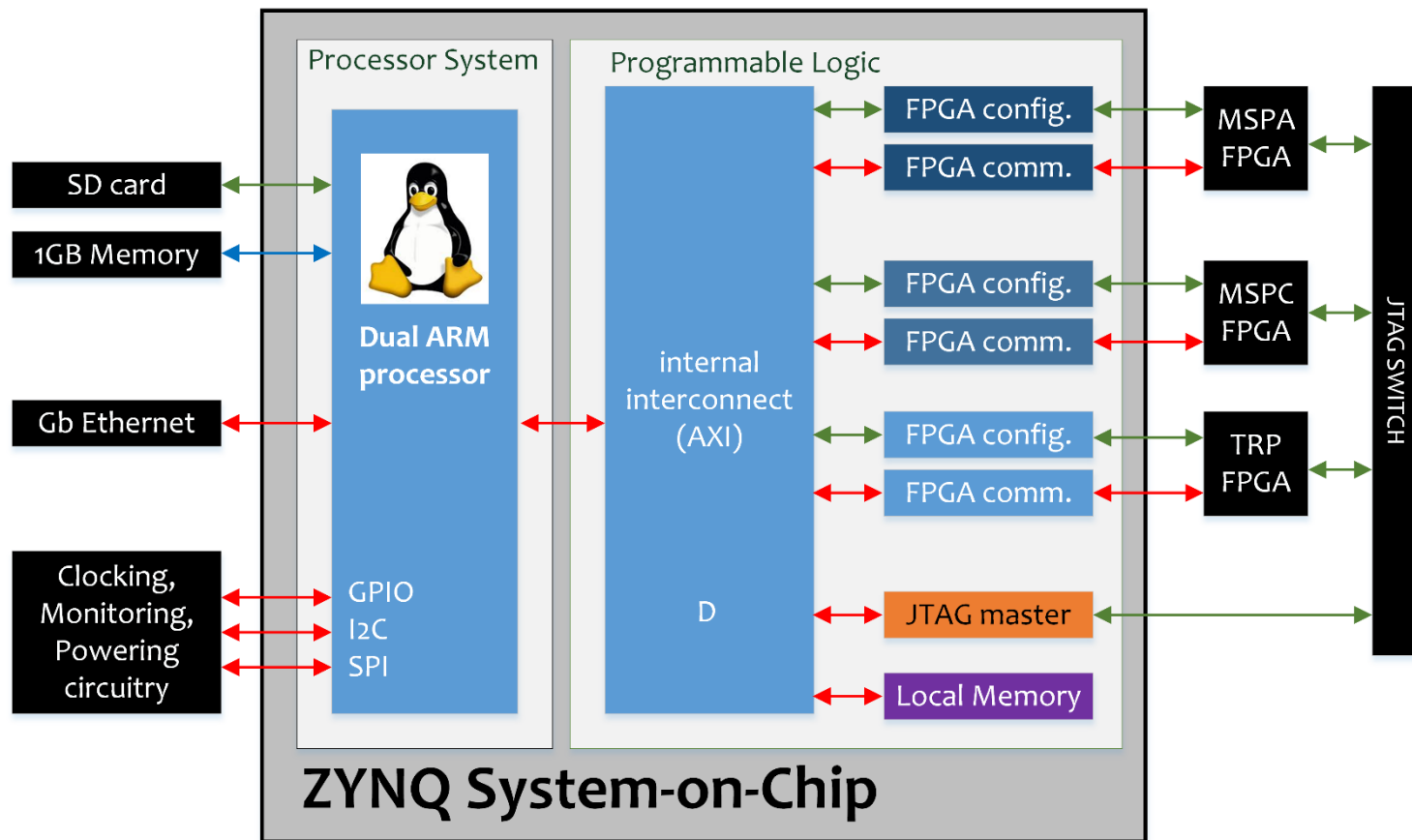
Gigabit Ethernet (GbE)

IP connection with a PC

Run Control functionality  
(i.e. control, configuration  
and monitoring)

FPGA bitstream download

On-board hardware  
monitoring (optical links,  
voltages, currents,  
temperatures etc.)



# MUCTPI Inter-FPGA Communication

## AXI Chip-to-Chip (C2C)

- Extension of the on-chip AXI bus outside the SoC
- Point-to-point interconnections, one per FPGA
- Less than 1 GPIO bank per FPGA (~36 I/Os @ 333Mb/s)
- Performance exceeds the GbE bandwidth to PC

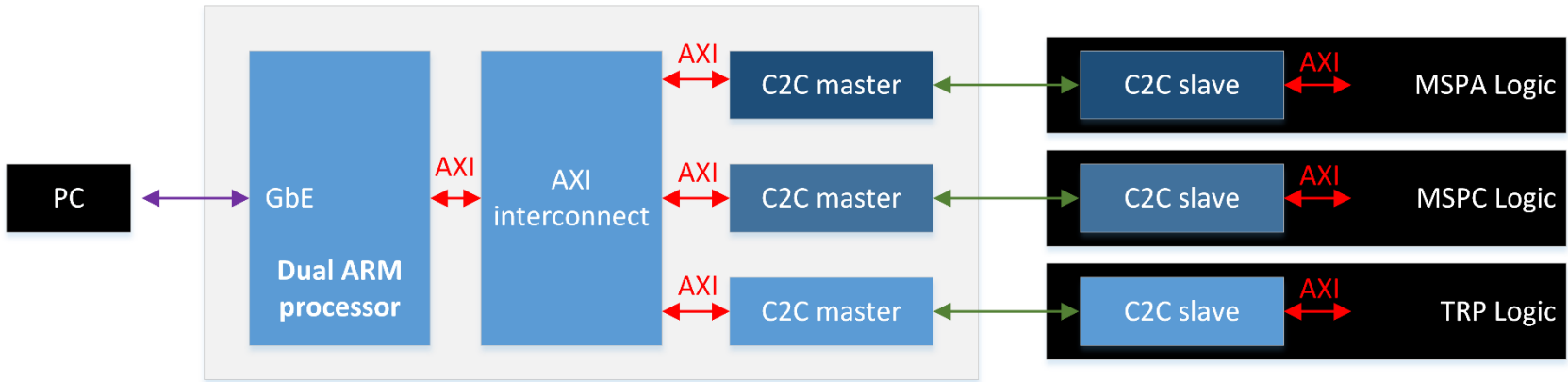
## Performance

### Block transfers

data size	performance	
block (KB)	local (MB/s)	c2c (MB/s)
1	43	41
2	64	62
4	111	101
8	180	149
16	270	199
32	355	247
64	426	277
128	472	295

### Single word access

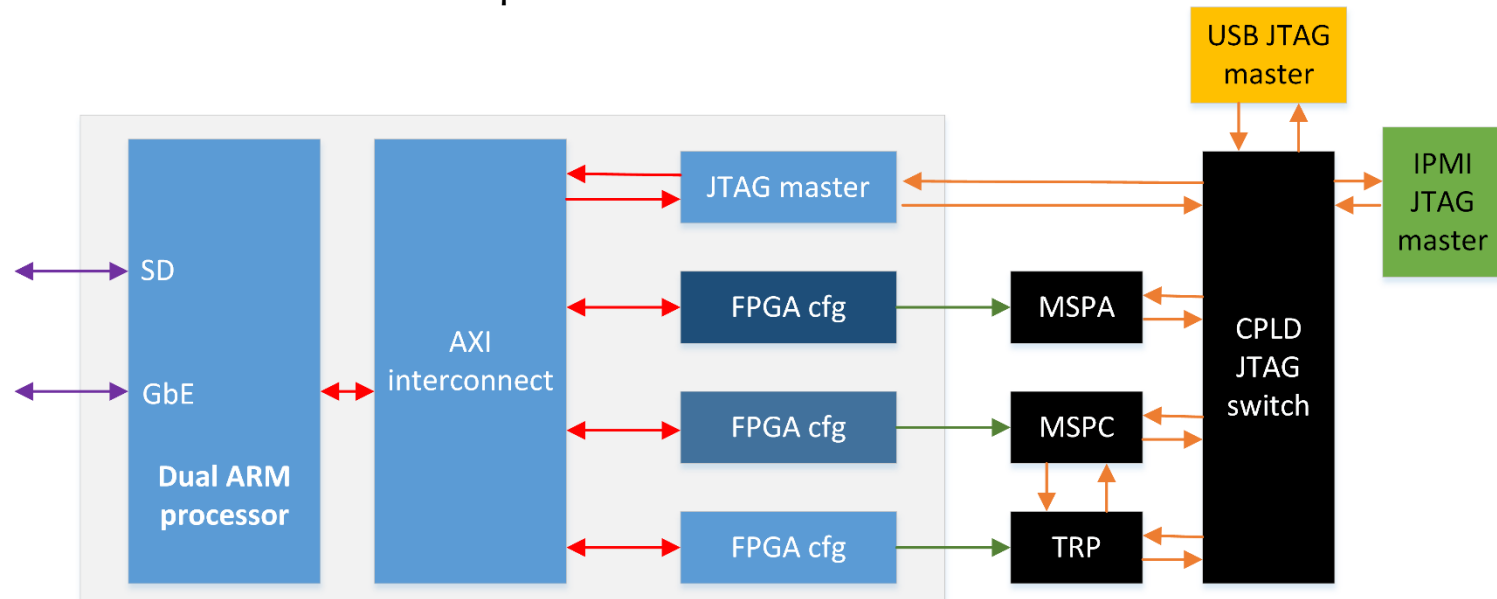
local (MB/s)	c2c (MB/s)
30	6



# MUCTPI FPGA Configuration

## Configuration scheme

- SoC boots via SD card / QSPI Flash / Ethernet
- No dedicated configuration memories for the Ultrascale FPGAs
- SoC configures the Ultrascale FPGAs via dedicated configuration controllers
  - Ultrascale FPGA bitfiles from SD card or Ethernet (200MB in total)
  - Less than 10 seconds total configuration time (via the Slave Serial protocol)
- USB-JTAG cable for initial debugging
- Virtual JTAG cable via Ethernet implemented in SoC





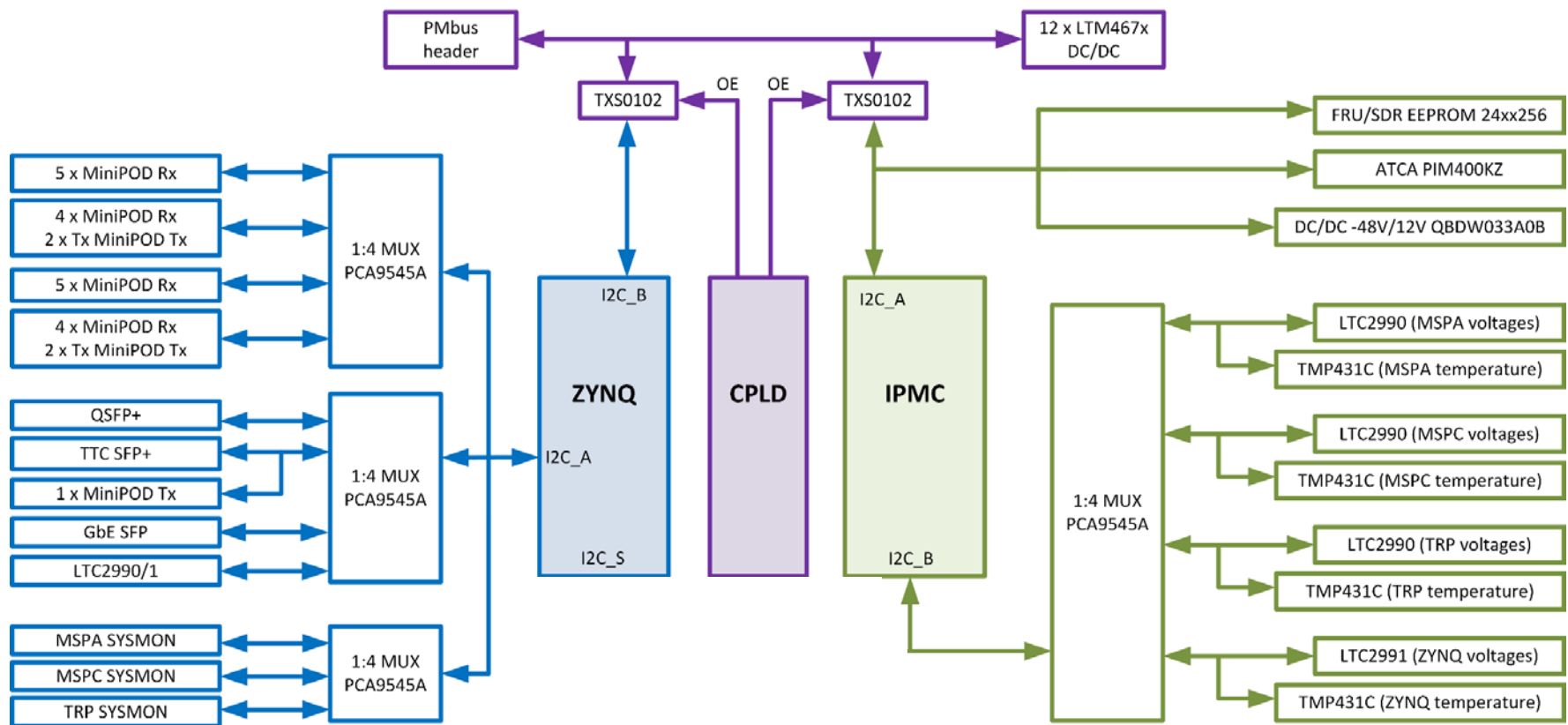
# MUCTPI Hardware Monitoring

## Hundreds of parameters monitored

- Temperature, Current, Voltages
- Optical receiver power
- Error conditions / alarms
- IC/module identification

## Two independent monitoring paths

- via the ZYNQ SoC
- via IPMC and ATCA shelf manager using independent i2c sensor devices
- Same parameters monitored (however using different sensor devices)





# MUCTPI Serial Links

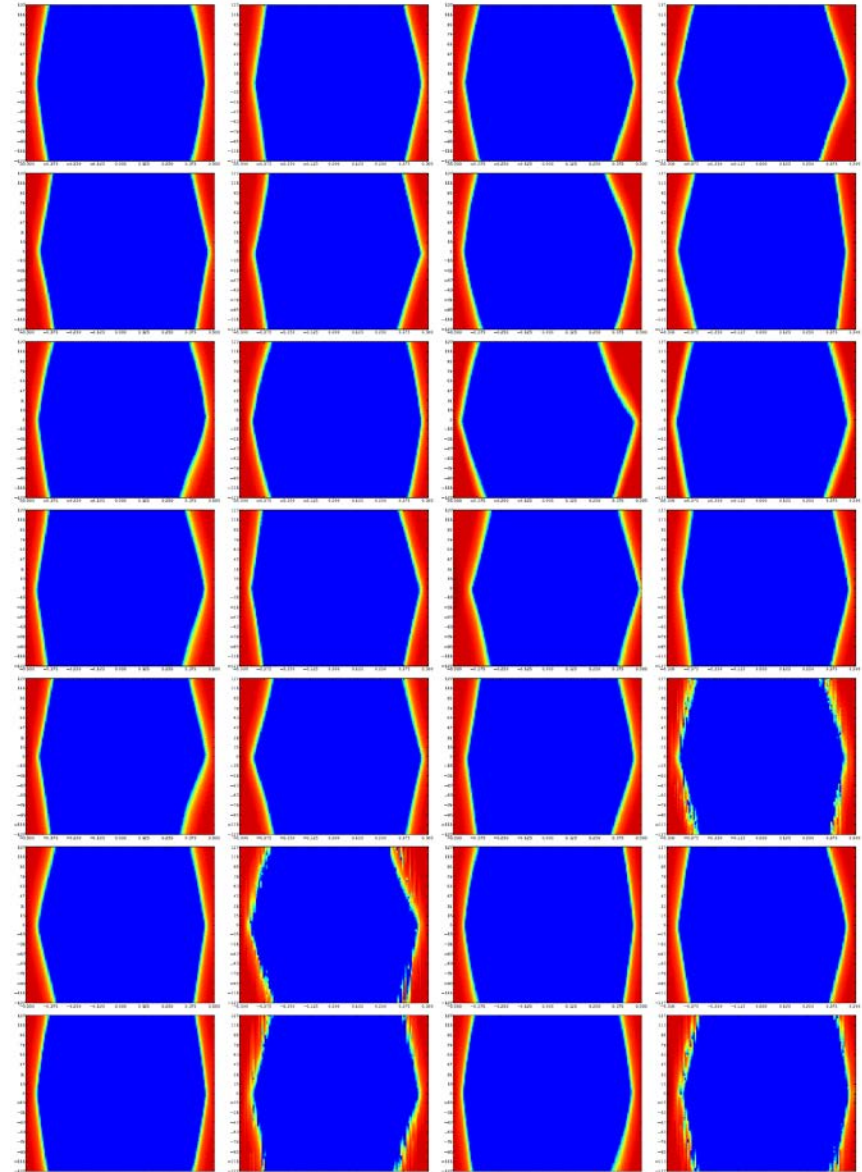
## Multi-Gigabit serial links (~330)

- All tested successfully using the Xilinx Bit Error Rate Test tool (IBERT)
- Excellent performance at 6.4Gb/s with very wide eye opening (~75% of the duty cycle)
- Compatibility for future operation at 9.6 & 12.8 Gb/s confirmed
  - error-free operation of 100+ links at 12.8Gb/s for 10 days

## Low latency LVDS serial links (~240)

- Error free operation at 1.28Gb/s
- Wide eye opening ( avg. 70% of the duty cycle)

Example of eye diagrams at 6.4Gb/s





# MUCTPI Power Supply

Input power: -48V DC -> 12V DC -> twelve point-of-load DC/DC converters

LTM467x family by Linear Technology

Dual DC/DC converters (13A or 18A per channel)

Control/monitoring through PMbus (voltage/current/sequencing etc)

GUI used for initial configuration & monitoring during test and debugging

PMbus accessible via the SOC to read voltage, current, temperature, alarms etc.

The screenshot displays the LTPowerPlay v1.2.112.0 software interface. The main window is divided into several panes:

- System Tree:** Shows a hierarchy of converters labeled U0 through U11, each with a status icon.
- Config U0 0:** A detailed configuration window for a specific converter. It includes sections for:
  - General Configuration Registers:** Settings for address, channel, and on/off control.
  - On/Off Control and Margining:** Parameters for controlled on, soft start, and margining.
  - PWM Related Configuration:** Settings for PWM mode and frequency.
  - Fault Responses - Input Voltage:** Configurable fault responses for input voltage deviations.
  - Output Voltage:** Target output voltage (3.3000 V) and margining parameters.
  - Fault Responses - Output Voltage:** Configurable fault responses for output voltage deviations.
  - Output Voltage - Miscellaneous:** Parameters like VOUT\_MAX and VOUT\_MODE.
  - Input Current Calibration:** MFR\_IN\_OFFSET\_LTC.
  - Output Current Calibration:** IOUT\_CAL\_GAIN and IOUT\_CAL\_GAIN\_TC.
  - Output Current:** IOUT\_OC\_FAULT\_LIMIT and IOUT\_OC\_WARN\_LIMIT.
  - Fault Responses - Output Current:** Configurable fault responses for output current.
  - External Temperature Calibration:** MFR\_TEMP\_1\_GAIN and MFR\_TEMP\_1\_OFFSET.
  - External Temperature Commands and Limits:** OT\_FAULT\_LIMIT\_PAGED and OT\_WARN\_LIMIT\_PAGED.
  - Fault Responses - External Temperature:** Configurable fault responses for external temperature.
  - VOUT\_COMMAND:** A section for issuing commands to the converter.
- Telemetry:** A window showing real-time data for U0:0, including:
  - Input Voltage:** 11.9219 V
  - Output Voltage:** 3.3005 V
  - Input Current:** 1.2578 A
  - Output Current:** 2.180 A
  - Temperature:** 45.6 °C
  - Power:** 7.172 W
- Dashboard - U0 (7/40) - LTM467:** A summary view of the converter's status.
- READ\_IOUT (All Pages in System):** A table listing current values for all converters (U00 to U11).
- Telemetry Plot:** A graph showing the output current (READ\_IOUT) over time, with a 2.4Hz zoom.
- Idealized On/Off Waveforms:** A graph showing the idealized on/off waveforms for U0:0.

# MUCTPI Power Consumption

Estimated to be up to 300 Watts max (based on Xilinx Power Estimator)

200W consumption measured with all links running at 12.8Gb/s

ATCA platform supports up to 400W per board

Successful powering and heat dissipation tests using test firmware with all MGT links running and commercial passive heatsinks

Upgrade of some DC/DC converters with pin-compatible devices with higher current capabilities possible

**XILINX** Xilinx Power Estimator (XPE) - 2016.3  
Kintex® UltraScale™, Virtex® UltraScale  
Release: 5-Oct-2016

Project: [Empty]

**Settings**

Device	
Family	Virtex UltraScale
Device	XCVU160
Package	FLGC2104
Speed Grade	-1H
Temp Grade	Extended
Process	Maximum
Voltage ID Used	
Characterization	Production (± 20% accuracy)

**Environment**

Junction Temperature	<input type="checkbox"/> User Override	
Ambient Temp		35.0 °C
Effective ΘJA	<input type="checkbox"/> User Override	
Airflow		500 LFM
Heat Sink		Medium Profile
ΘSA		0.8 °C/W
Board Selection		Medium (10"x10")
# of Board Layers		16 or more
ΘJB		
Board Temperature		

**Implementation**

Optimization	None
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**Summary**

Total On-Chip Power	56.8 W
Junction Temperature	65.9 °C
Thermal Margin	34.1 °C   44.9 W
Effective ΘJA	0.5 °C/W

**Power Breakdown**

46%	Transceiver.....	26.043W
6%	I/O.....	3.680W
31%	Core Dynamic.....	17.532W
17%	Device Statc.....	9.573W
Power supplied to off-chip devices		0.443W

**On-Chip Power**

Resource	Power (W)	(%)	
Core Dynamic	CLOCK	1.317	2
	LOGIC	7.707	14
	BRAM	7.839	14
	DSP	0.598	1
	PLL	0.000	0
	MMCM	0.071	0
	Other	0.000	0
	Hard IP	0.000	0
I/O	IO	3.680	6
Transceiver	GTH	13.815	24
	GTY	12.229	22
Device Static		9.573	17

**Power Supply**

Source	Voltage	Total (A)
V <sub>CCINT</sub>	1.000	25.620
V <sub>CCINT_IO</sub>	1.000	1.181
V <sub>CCBRAM</sub>	1.000	0.576
V <sub>CCAUX</sub>	1.800	0.727
V <sub>CCAUX_IO</sub>	1.800	0.899
V <sub>CC0 3.3V</sub>	3.300	
V <sub>CC0 2.5V</sub>	2.500	
V <sub>CC0 1.8V</sub>	1.800	1.566
V <sub>CC0 1.5V</sub>	1.500	
V <sub>CC0 1.35V</sub>	1.350	
V <sub>CC0 1.2V</sub>	1.200	
V <sub>CC0 1.0V</sub>	1.000	
MGT <sub>VCCAUX</sub>	1.800	0.270
MGT <sub>VCC</sub>	1.000	8.931
MGT <sub>AVTT</sub>	1.200	2.797
MGT <sub>VCCAUX</sub>	1.800	0.087
MGT <sub>YAVCC</sub>	1.000	3.722
MGT <sub>YAVTT</sub>	1.200	7.079
V <sub>CCADC</sub>	1.800	0.061

**Messages**

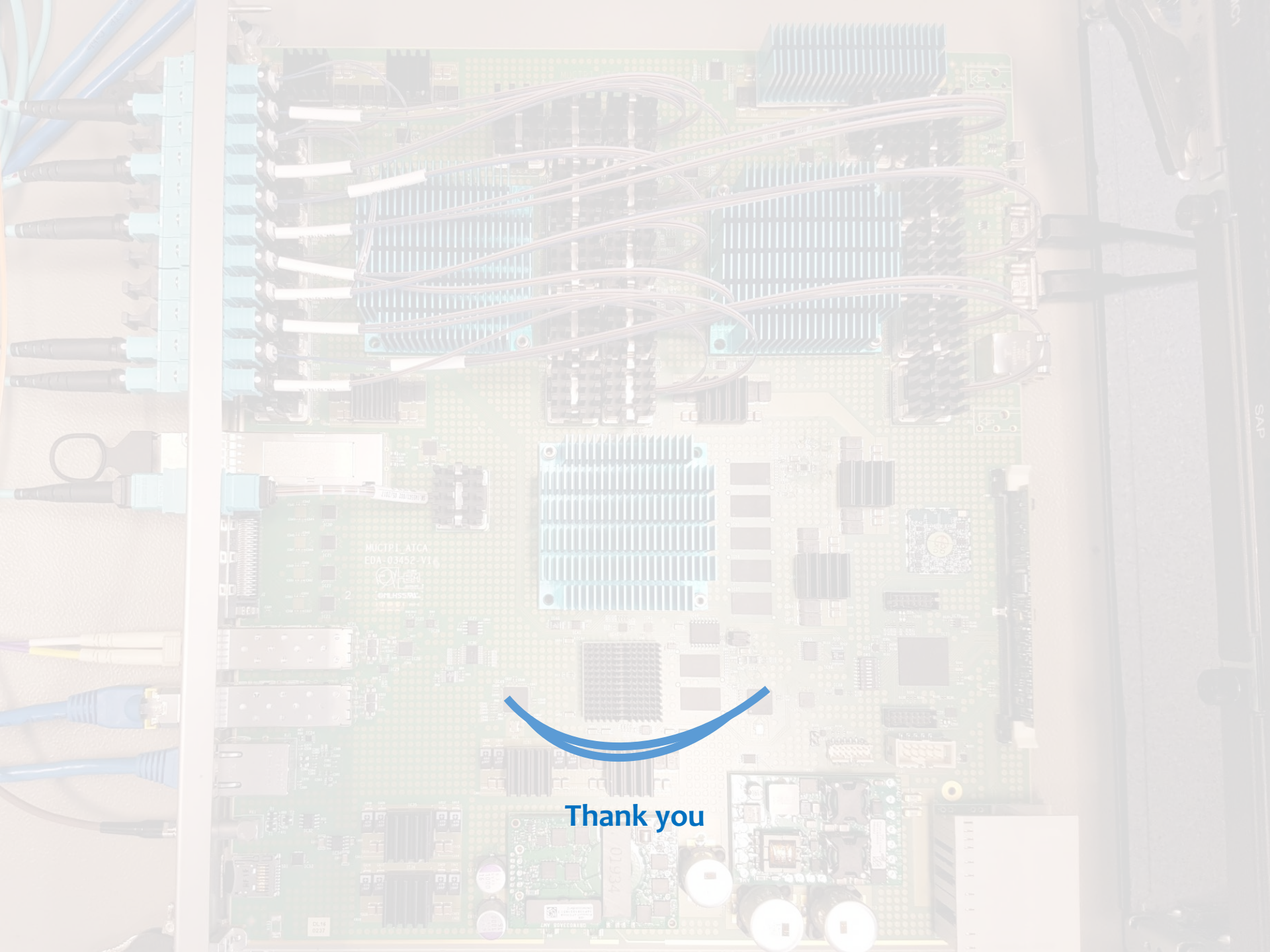
XILINX Power Advantage (check for updates) | File Support Request (WebCase) | Xilinx Power Estimator User Guide

Summary | Snapshot | Graphs | IP\_Manager | Clock | Logic | IO | BRAM | DSP | CLKMGR | GTH | GTY | Other | User

# MUCTPI Summary & Outlook

- Conceptual design, schematic entry and layout in 2016
- First fully assembled prototype received in Q2, 2017
- Another two partially assembled prototypes available for software development
- 95% of board features have been successfully tested
  - Only minor fixes required to the board
- Smooth bring-up of Zynq-based SoC thanks to extensive preparatory work with development kits
- Plan to upgrade MSP FPGAs to pin-to-pin compatible Ultrascale+ device (VU9P) for additional memory/logic resources for production modules





Thank you