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The ATLAS Muon-to-Central Trigger Processor Interface for the Phase-I Muon Trigger Upgrade

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The Muon-to-Central Trigger Processor Interface (MUCTPI) of the ATLAS experiment at CERN will be upgraded for run 3 of the LHC. The current system, a full 9U VME crate, will be replaced by a single AdvancedTCA blade, based on state-of-the-art FPGA technology and high-density ribbon fibre-optic transmitters and receivers. The module uses a System-on-Chip (SoC) with a processor running an embedded Linux operating system to communicate with the experiment run control system. We present the hardware design and implementation of the module, the communication model used in the SoC as well as results from the validation of the first prototype.

Summary

The Muon-to-Central Trigger Processor Interface (MUCTPI) is part of the Level-1 trigger system of the ATLAS experiment at CERN. It receives and combines information on muon candidates from the 208 trigger sector logic modules in the barrel and endcap regions of the detector and calculates the candidate multiplicity, taking into account the possible double counting between trigger sectors due to the geometrical overlap of the muon chambers and the trajectory of the muons in the magnetic field, and sends the result to the Central Trigger Processor (CTP).

The existing MUCTPI will be upgraded for run 3 of the Large Hadron Collider (LHC), in order to interface with the new muon endcap trigger sector logic modules which will be deployed as part of the muon new small wheel upgrade. The upgraded MUCTPI will also be able to send full precision information on the muon candidates identified by the muon trigger processors at the bunch crossing rate to the topological trigger processor (L1Topo) of the Level-1 trigger system, which will allow combined calorimeter/muon topological trigger algorithms to be implemented.

The MUCTPI upgrade requires a complete redesign of the existing VME based system. The design is based on state-of-the-art FPGA technology (Xilinx 20 nm UltraScale devices), featuring a large number of on-chip high-speed serial transceivers, and high-density ribbon fiber optics receiver and transmitter modules. These technologies allow a much higher integration of the new MUCTPI and enable the implementation of all the required functionality on a single AdvancedTCA (ATCA) blade. In comparison, the existing system requires a full 9U VME shelf with 18 boards. The module features over 270 multi-gigabit optical inputs/outputs operating at line rates between 6.4 and 12.8 Gbit/sec, resulting in an aggregate bandwidth of over 2 Tbit/sec.

Two large Virtex UltraScale FPGAs (sector processors), each covering one side of the detector, are used to receive and process the muon trigger data from the 208 sector logic modules. The sector processor FPGAs also send lists of muon candidates with their full precision information to L1Topo through up to 48 serial optical links.

A third FPGA, a Xilinx Kintex UltraScale device, is used to merge the information from the two sides of the detector, to perform the required trigger calculations and to send the resulting object multiplicities and trigger flags to the CTP. For events accepted by the CTP, it also outputs a list of muon candidates to the DAQ system and sends Region-of-Interest (RoI) information to the high-level trigger (HLT) to seed the muon processing.

Finally a Xilinx Zynq System-on-Chip (SoC) FPGA is used to interface the MUCTPI to the ATLAS run control system through a Gigabit Ethernet connection. It is used to configure and control the MUCTPI and to read

state and monitoring information. The SoC device runs an embedded Linux operating system with application-specific software using a remote-procedure-call approach.
We present the hardware design and implementation of the module as well as results from the validation of the first prototype.

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