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Development of the jet Feature EXtractor (jFEX) for the ATLAS Level 1 Calorimeter Trigger upgrade at the LHC

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To cope with the enhanced luminosity delivered by the Large Hadron Collider in 2021, the ATLAS experiment has planned a major upgrade. The first level trigger based on calorimeter data will be upgraded to exploit fine-granularity readout using a new system of Feature Extractors (FEXs), each optimized to trigger on different physics objects. This presentation is focused on the jet FEX.
The main challenges of such a board are the input bandwidth of up to 3 Tb/s, dense routing of high-speed signals and power consumption. We report on design, firmware development and results of integrated tests of a prototype.

Summary

To cope with the increased luminosity after Long Shutdown 2, ATLAS has planned a major upgrade of the sub-detectors. The Level 1 calorimeter trigger system is redesigned taking advantage of the latest technology available to exploit higher granularity data from the calorimeter. It consists of three subsystems, called Feature Extractors (FEXs), each optimized to trigger on different physics objects: eFEX (electromagnetic FEX) identifies electron, gamma and tau signatures; jFEX (jet FEX) identifies jets and large-area taus and calculates energy sums including missing transverse energy; gFEX (global FEX) identifies large-area jets and calculates global variables. This presentation focuses on the jFEX prototype, its design, performance tests and the ongoing firmware development.
The board design is based on the ATCA specifications, consists of 24 layers of MEGTRON6 and it hosts four FPGAs from the Xilinx UltraScale family (XCVU190FLGA2577). The selected FPGA model presents one of the largest number of MGT links available within the Virtex UltraScale family. 7 jFEX modules will be produced covering the whole calorimeter with different granularity depending on the detector region.
The jFEX design presented several challenges: The high input bandwidth of up to 3 Tb/s combined with the on-board data duplication results in a dense routing of over 500 differential high-speed signals. This duplication is required due to a limited optical input capacity. The used PMA loop-back method allows data duplication without any signal splitting or additional devices at the cost of some latency. 20 opto-electrical receivers feed the incoming data from 240 fibers to the FPGAs and four opto-electrical transmitters send the processed data of the algorithms to the next stage in the trigger system, the Topological Processor (L1Topo), via 48 optical fibers. The worst case estimate for the power consumption of the whole board is about 500 W. This required careful planning of the power planes including simulations of current densities and voltage drops and simulations on signal integrity.
An extension mezzanine is used, where the Xilinx Zynq System on Chip manages board control and FPGA communication via IPBus. After production and assembly of the jFEX prototype the board has been tested in Mainz and during integrated tests at CERN. In parallel there is an ongoing firmware development of algorithms and infrastructure.

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