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The Development of the Global Feature eXtractor (gFEX) for the ATLAS Level 1 Calorimeter Trigger at the LHC

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During the ATLAS Phase-I upgrade, the global feature extractor (gFEX) will be designed to maintain the trigger acceptance against the increasing luminosity for the ATLAS Level-1 calorimeter trigger system. The prototypes v1 and v2 have been designed and tested in 2015 and 2016 respectively. With the lessons learned, a pre-production board with three UltraScale+ FPGAs and one ZYNQ UltraScale+, and 35 MiniPODs is implemented in an ATCA module. This board will receive coarse-granularity information from the entire ATLAS calorimeters on up to 300 optical fibers and each FPGA has 24 links to the L1Topo at the speed up to 12.8Gb/s.

Summary

The Large Hadron Collider (LHC) will undergo a series of upgrades to increase both collision energy and luminosity in next ten years, and the ATLAS experiment will follow the same upgrade schedule. During the Phase-I upgrade, a new component - global feature extractor (gFEX) will be designed to maintain the trigger acceptance against the increasing luminosity for the ATLAS Level-1 calorimeter trigger system. The gFEX is designed to identify patterns of energy associated with the hadronic decays of high momentum Higgs, W, & Z bosons, top quarks, and exotic particles in real time at the LHC crossing rate. The prototype v1 and v2 have been designed and fully tested in 2015 and 2016 respectively. The prototype v1 board is designed with one single system-on-chip processor, ZYNQ, and one Xilinx Vertex-7 FPGA for challenge technologies validation and the prototype v2 board is design with three Vertex UltraScale FPGAs and one ZYNQ for the full functionalities and performance test. Both gFEX prototypes have been developed and evaluated successfully. The gFEX prototype v1 has been used in the LArL1Calo link speed test, to determine the baseline link speed of 11.2Gb/s. The prototype v2 has been designed and tested in the lab. High-speed fiber-optic links are stable at 12.8 Gbps, and on-board electrical links are stable at 25.6 Gbps. Parallel buses operate at 1.12 Gb/s with good margin. The integration test with FELIX has been successful, and now the prototype v2 is being used as firmware development platform.

With the lessons learned from these two prototype boards, a pre-production board with three Xilinx UltraScale+ FPGAs and one MPSOC ZYNQ UltraScale+, and 35 MiniPODs is implemented in an ATCA module. This board will receive coarse-granularity information from the entire ATLAS calorimeters on up to 300 optical fibers at the speed up to 12.8 Gb/s synchronized to 40 MHz LHC clock frequency and each FPGA has 24 links to the L1Topo at 12.8 Gb/s. The ZYNQ UltraScale+ will be the only one to communicate with FELIX for the TTC clock recovery and data transfer. It is also used to control and configure all the three processor FPGAs, monitor board health, and interface to Gigabit Ethernet and UART. Now, the routing of the pre-production board is almost done and will be sent out for fabrication in the May. We will bring it up around July and will present the performance on the meeting.

Primary author: STAMEN, Rainer (Ruprecht-Karls-Universitaet Heidelberg (DE))

Presenter: TANG, Shaochun (Brookhaven National Laboratory (US))

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