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2. Electrically Aware Design Flow

- In-design extraction and analysis of parasitics, EM/ IR and LDE parameters
- Resimulation with parasitics and LDE parameters from a layout in-progress (prior to sign-off)
- Using electrical constraints to verify and meet design requirements

Abstract

Advanced nodes have introduced many new design challenges including significantly greater impact of parasitics and other electrical effects, and design iterations are becoming increasingly costly as well. It is no longer possible to push out analyzing the effect of parasitics and checking for reliability issues till the very end of the design cycle i.e. during sign-off. It is now almost imperative to perform electrical analysis, specifically simulating with parasitics and layout dependent device parameters derived from layout, and checking for Electro-migration issues and IR Drops. This presentation covers such an in-design methodology which also helps designers meet design requirements through electrical constraints, and verify that these constraints are being followed in the physical implementation. Once identified, issues such as Electro-migration violations can be fixed easily with guidance and assistance from the tool, and the design can be re-verified quickly while the layout is still in progress, without waiting till sign-off.

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