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Designing CMOS Chips Beyond 65 nm

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Moore's Law has entered a new frontier as device scaling continues to excel in 10nm and beyond. As the physical dimension of devices and interconnect are being shrunk, the design rules and the design flow, for both design community and EDA community, face unprecedented complexity. Conventional design optimization techniques also need to take the novel process technologies, such as multi-gate devices (e.g., FinFET), spacer technology, and self-aligned multiple patterning lithography, into account to achieve the best possible performance, power, and area for a design with more and more functionalities integrated into one single chip.

In this presentation, first, we will talk about simulation technologies to handle special effects introduced by advanced process nodes, such as high transistor speed, high transistors/RC capacities and reliability effects etc. with reasonable speed and performance while maintaining spice simulation accuracy. Secondly, we will also discuss about advanced integrated simulation environment targeting for different design phases to meet the tight design window. Finally, we will touch upon the importance of system integration for advance process nodes and bring up the solution for the system integration, which include IC/Package/PCB, from both implementation and analysis point of views.

Advanced Process Nodes Simulation Strategy
a. Simulation challenge for advanced process nodes.
b. Simulation technology overview
c. Reliability simulation
i. Aging simulation
ii. Self-heating simulation
iii. EMIR Simulation
d. Summary

Advanced integrated Simulation environment
a. Why we need integrated simulation environment?
b. Environment for individual block
c. Environment for block integration.
d. Environment for verification and regression.
e. Summary

. System integration: integrated IC/package/PCB together
a. Implementation flow
b. Analysis flow

Summary

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