Trends in Radiation Effects for sub-65 nm Technologies

TWEPP 2017, Santa Cruz CA

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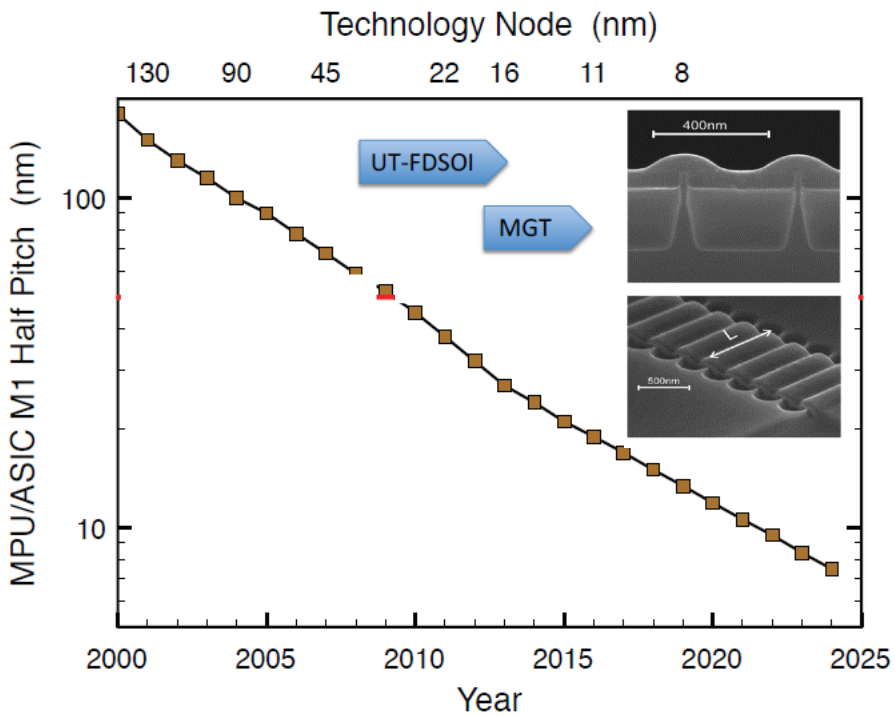
Overview

- Background
- Environments
- Total Ionizing Dose (TID) Effects:
  - Planar FDSOI, PDSOI, Bulk FinFETs and SOI FinFETs
  - Benefits of current processing techniques
  - Geometry considerations
- Single Event Effects
  - Effects of scaling on Soft Error Susceptibility & Cross sections
  - MCU considerations
  - Effects of geometry and processing
- Modeling Considerations
- Beyond Si CMOS, novel Memories

From Planar to 3D Topologies

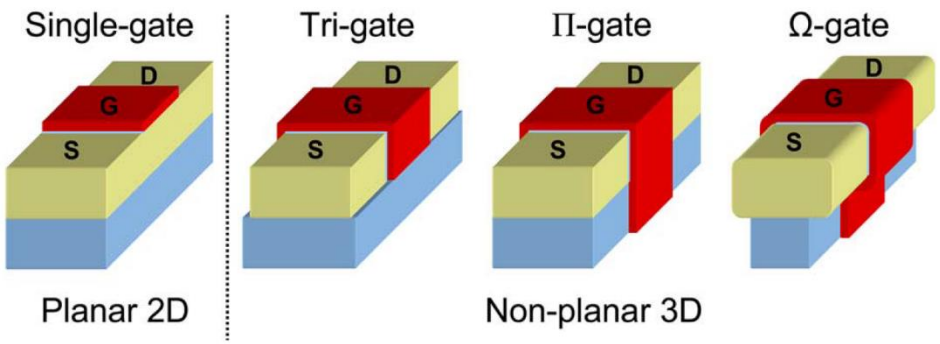
- Geometric scaling dominated miniaturization of Commercial industry for 3 decades
- Recent paradigm shifts
  - Fully Depleted Silicon-On-Insulator (FDSOI)
  - Multi-gate/FinFET Technologies
- Multi-gate transistors have a history dating back to 1980s
- Push to use Commercial Technologies
  - Mixed response to TID & SEE



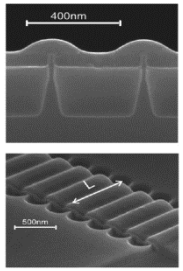
After, L. W. Massengill *et al.* IEEE Conference Proceedings IRPS 2012.

Sub-65 nm Si technology

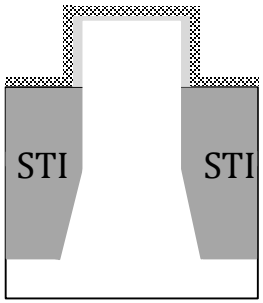
- Increased drive strength, reduced SCEs and potential for further miniaturization
- Industry standard is a 14 nm FinFET bulk Si CMOS
- NAND migrated to 3D structures
  - Metallization is Tungsten (implications for Neutron capture)
  - Process & noise challenges

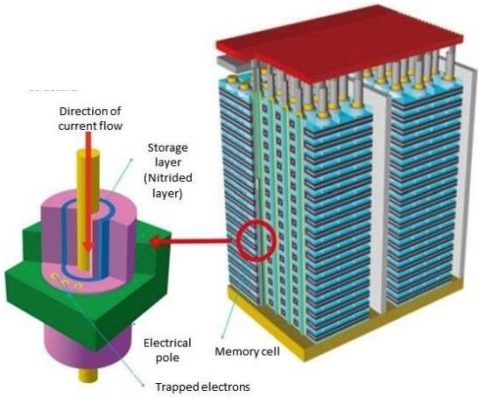


After, E. Simoen *et al.*, IEEE Trans. Nucl. Sci, vol. 60, no. 3, June 2013.



After, C.-H. Jan *et al.* Symp. On VLSI Tech. Dig. Of Techn. Papers, pp. 135, 2003.



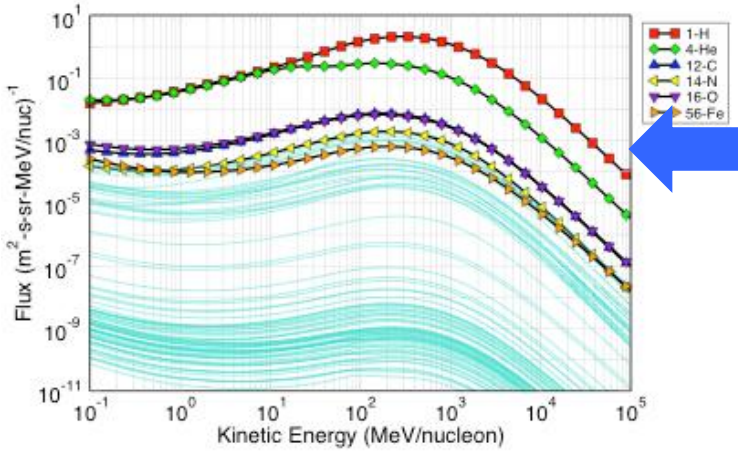


Toshiba BiCS 3D NAND Flash

After, https://www.storagenewsletter.com/2016/08/11/more-on-future-of-toshiba-3d-nand-flash-memory/

Radiation Environments

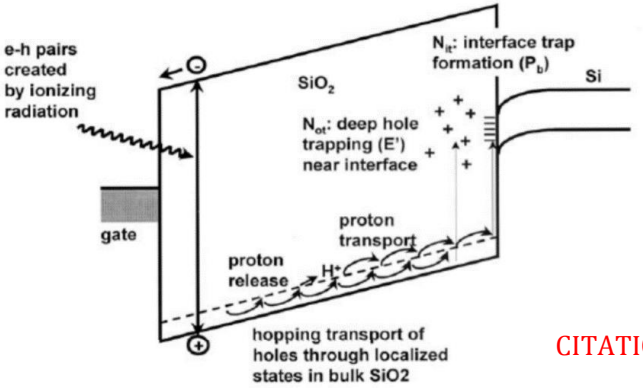
Environment		Particles	TID	SEE
Space				
	Typical GEO Orbit	Mostly lightly ionizing **Some heavy ions (Concerned up to Fe)**	$\leq$ **1*Mrad* (*SiO*$_2$)** ***Mission Lifetime***	$\sim 10^{15} cm^{-2}$
Accelerator		Lightly ionizing	**~1Grad (SiO$_2$)**	$\sim 10^{15} cm^{-2}$



Typical GEO orbit:
- Mostly lightly ionizing particles
- Some heavy ions

Total Ionizing Dose Effects

- TID Effects have been studied extensively for planar MOS devices.
  - Typical doses considered for space applications ≤ 1 Mrad(SiO_2)
  - Trends may or may not hold true for ultra-high doses
- Ionizing radiation induces flood of carriers
  - Initial recombination
  - Transport
  - Interface trapped charge & interactions with hydrogen
- Parametric shifts.
  - Threshold voltage shifts
  - Leakage current



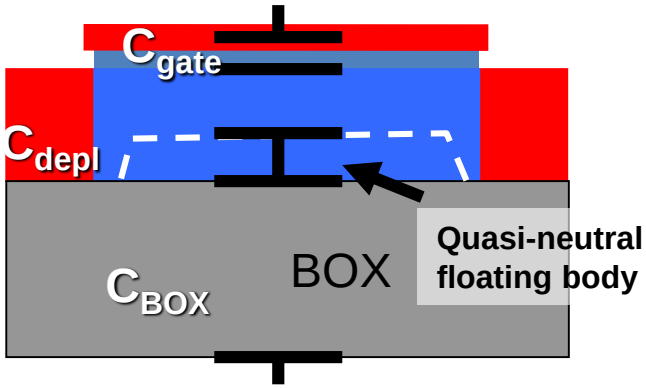
CITATION

Thin Film Silicon-On-Insulator (SOI)

- Two "modes" for planar CMOS on Silicon-On-Insulator (SOI)
- Depend on silicon thickness and doping

Partially Depleted (PD)

When ON, depletion region does not extend to the BOX

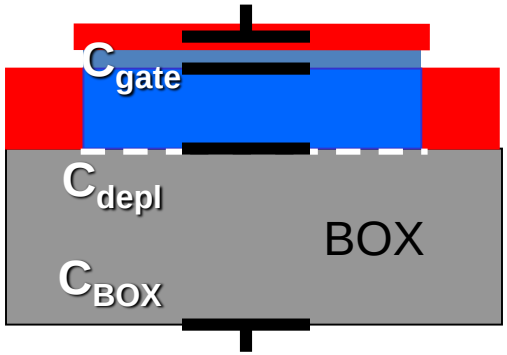


floating body

front gate decoupled from BOX

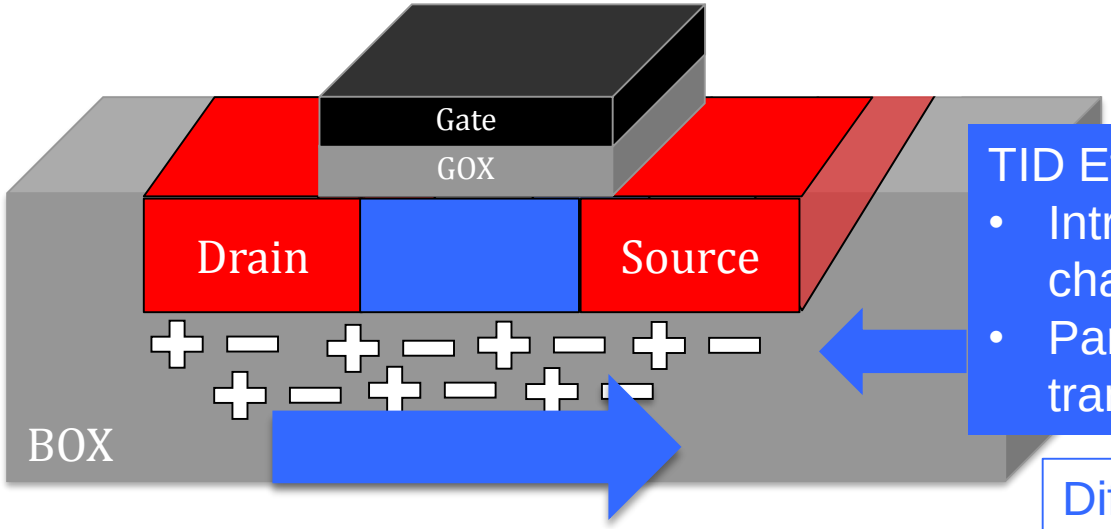
Fully Depleted (FD)

When ON, depletion region does extend to the BOX

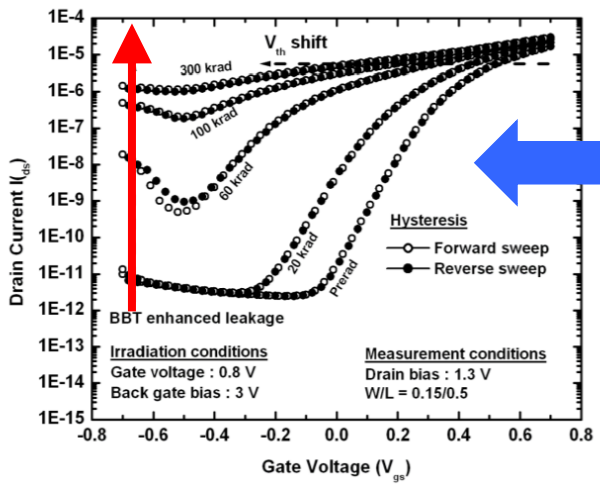


Front gate and BOX coupled

TID in Planar SOI



TID Effects in SOI
- Introduction of trapped charge in BOX
- Parasitic back gate transistor



F. E. Mamouni *et al.* IEEE Trans. Nucl. Sci. vol. 55, no. 6, pp. 3259-3264.

V_{th} shifts & increase in OFF-state leakage

Different TID mitigation approaches for FD- and PDSOI

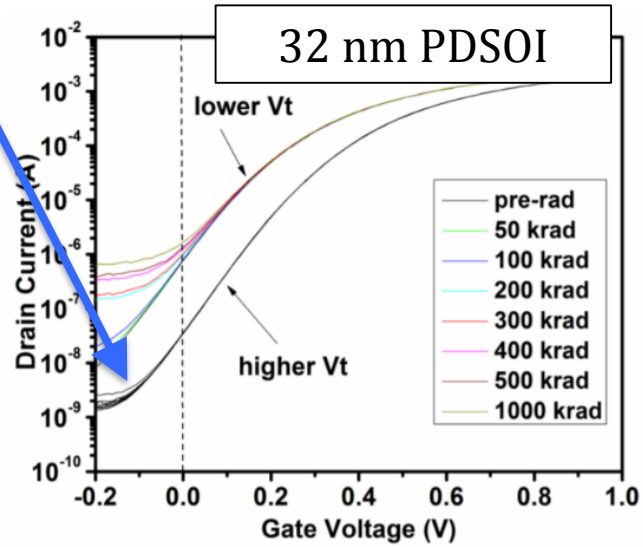
Reducing the BOX thickness exacerbates parasitic transistor

Highly dependent on Electric field in the BOX

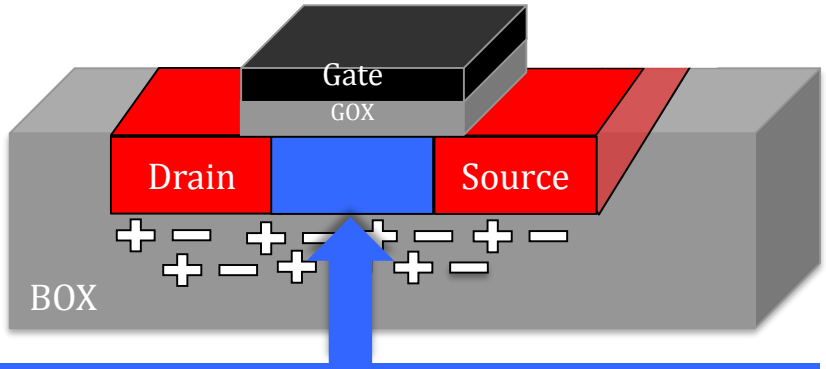
TID in FDSOI vs PDSOI

- FDSOI typically poor TID tolerance
  - Parasitic back gate is worse (lower doping)
  - Mitigate by removing substrate
- Commercial PDSOI 32 nm devices show promising TID hardness
  - Scaling processing techniques work to our advantage

Higher doping levels increases TID tolerance



N. Rezzak *et al.* IEEE International SOI Conference 2012.

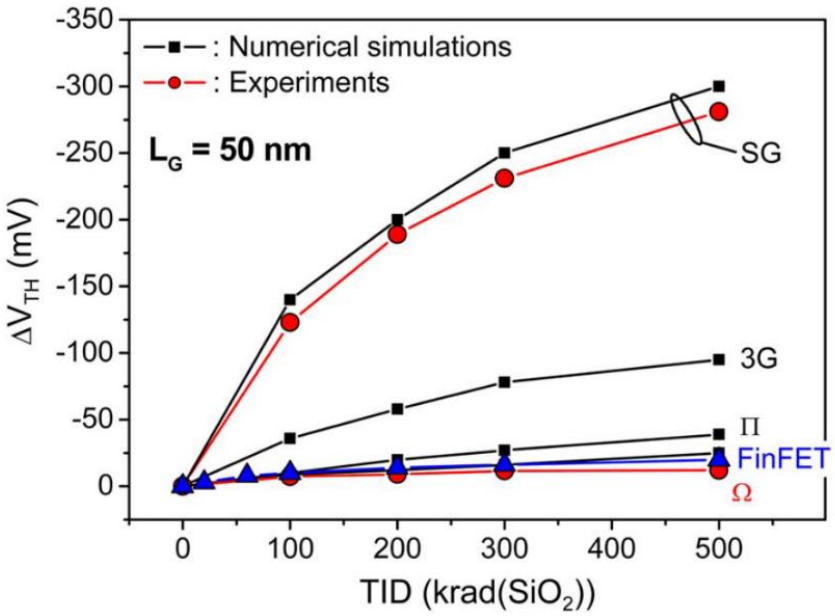


Introduction of retrograde doping in PDSOI mitigate SCEs

Requires more trapped charge in the BOX to turn on the parasitic transistor

TID in FinFETs v.s. Planar

- FinFETs present the promising TID tolerance
  - Screening of parasitic effects through lateral gates
- Bulk v.s. SOI
  - Similar problems encountered as in planar technologies



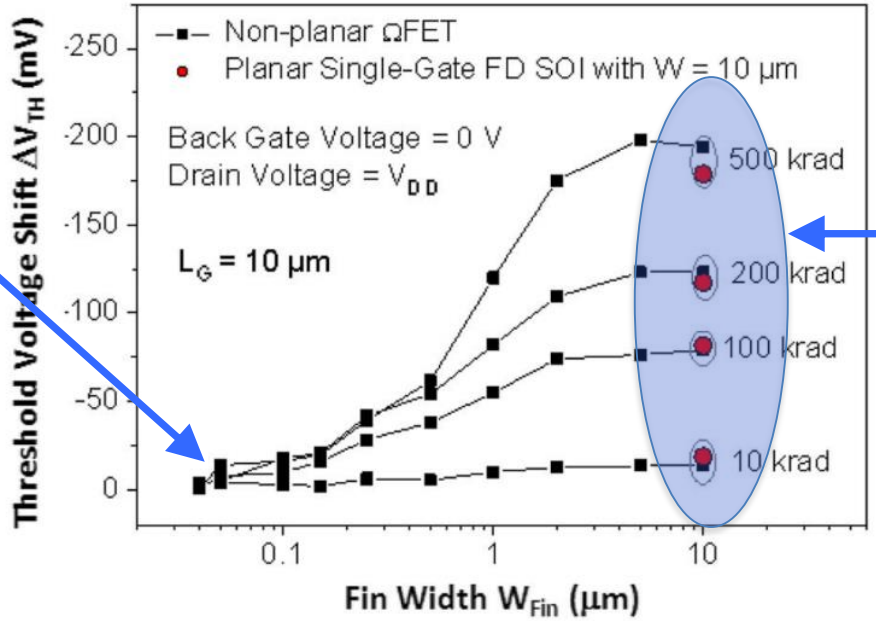
Various factors affect TID tolerance in FinFETs
- Geometry
- SOI v.s. Bulk
- Doping

After, E. Simoen *et al.* IEEE Trans. Nucl. Sci., vol. 60, no. 3.
M. Gaillardin *et al.* IEEE Trans. Nucl. Sci., vol. 53, no. 6. F. El Mamouni *et al.* IEEE Trans. Nucl. Sci., vol. 56, no. 6.

TID Dependence on W_{fin} in SOI FinFETs

Increased performance due to screening effects from lateral gates.

Increased tolerance to TID with scaling

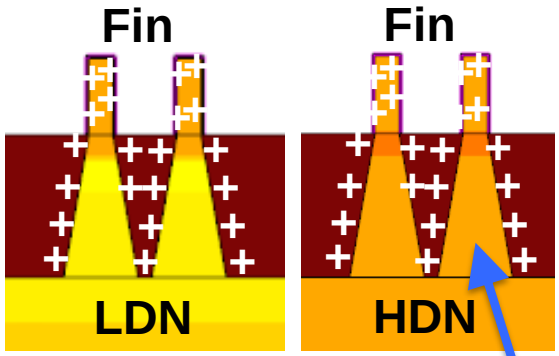


Large w_{fin} FinFETs look like their planar counterparts

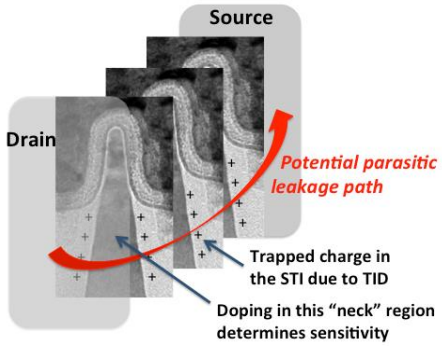
M. Gaillardin *et al.* IEEE Trans. Nucl. Sci., vol. 53, no. 6.

TID in Bulk FinFETs

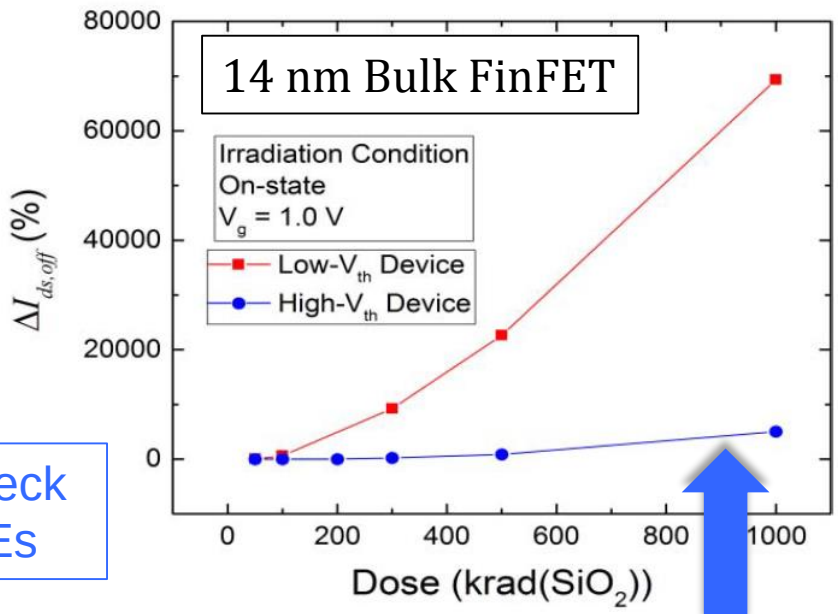
- TID dominated by trapped charge in the Shallow Trench Isolation (STI)



Highly doped neck to reduce SCEs



http://www.chipworks.com/blog/technologyblog/2012/04/23/intels-22-nm-tri-gate-transistors-exposed/



Highly doped neck region mitigates TID effects.

More trapped charge required in STI to turn on lateral parasitic transistor

After, M. P. King *et al.* IEEE Trans. Nucl. Sci., vol. 64, no. 1.

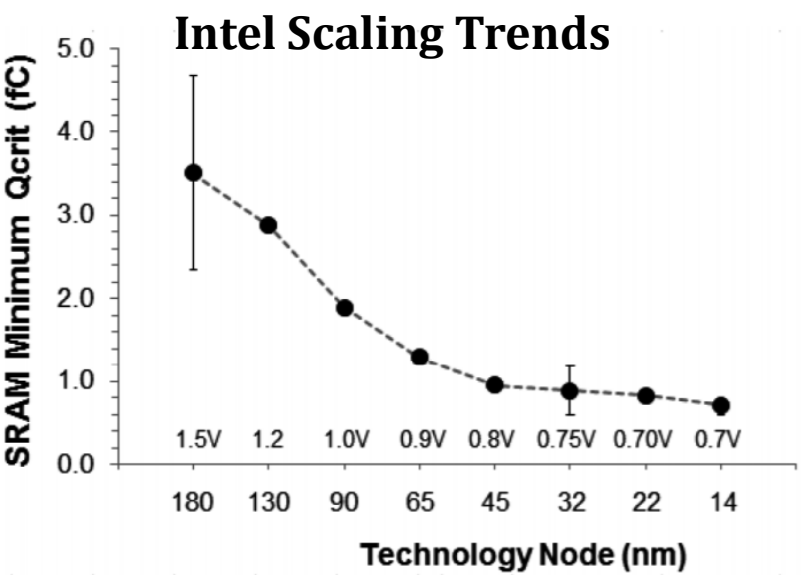
TID Summary

- FDSOI
  - Typically poor TID tolerance due to low doping levels
- PDSOI and Bulk FinFETs
  - TID effects mitigated with high retrograde body doping
- Commercial 32 nm PDSOI is likely a good alternative to FinFET counterpart
  - Accessible commercial technology with comparable TID tolerances

Single Event Effects

SEEs in Scaled Technologies

- Soft Errors is a major reliability concern
  - Increasingly for CMOS logic.
  - Competing mechanisms
- Considerations for circuit susceptibility beyond physical scaling.
  - Particle type (lightly ionizing versus heavy ions)
  - Indirect Strikes



N. Seifert *et al.* IEEE Trans. Nucl. Sci., vol. 62, no. 6.

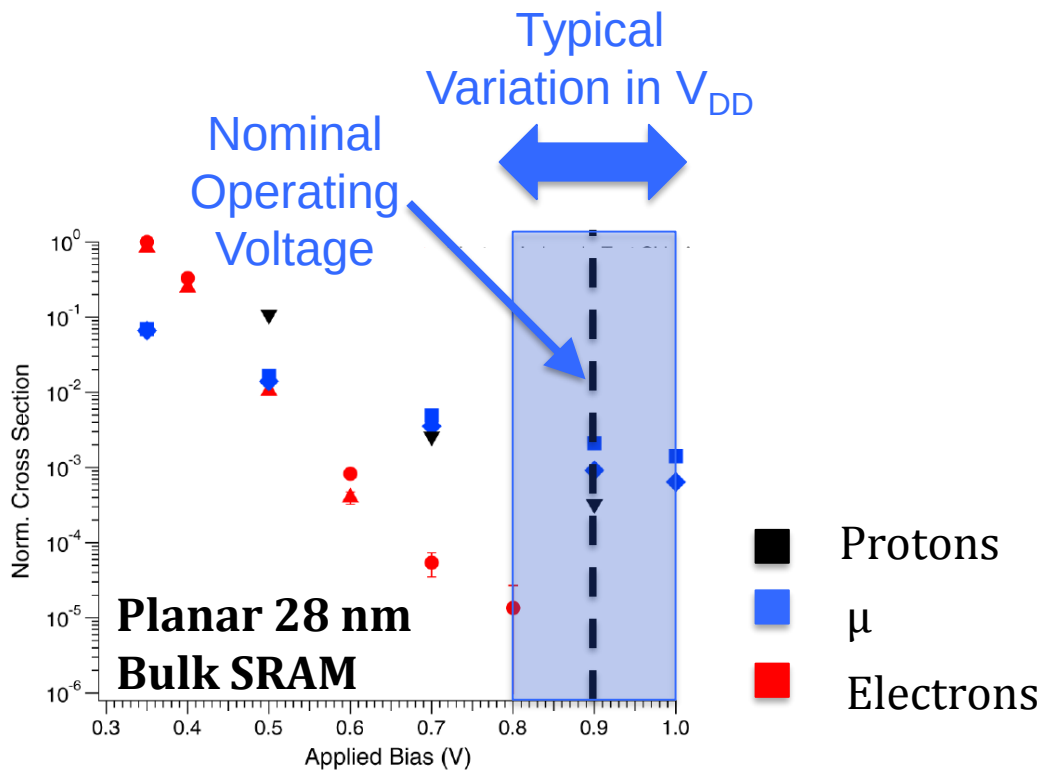
Smaller Physical Dimensions:

- ***Single cell less likely to be struck***
- ***Smaller SETs (particularly for SOI)***

- ***Small Q_{crit}***
- ***Larger packing densities***
- ***Faster clock speeds***

Increasing Sensitivity

Lower critical charges result in increased sensitivity to lightly ionizing particles.
Electron upsets could occur from indirect strikes.



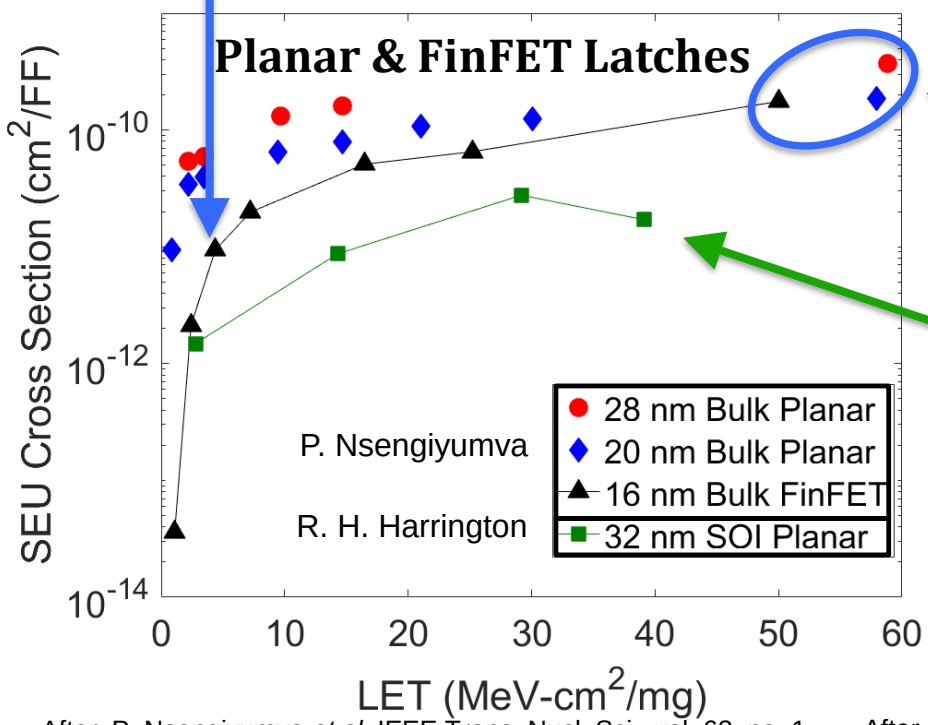
M. P. King *et al.* IEEE Trans. Nucl. Sci., vol. 60, no. 6.

The contribution of electrons to overall SER will depend on particular radiation environment

Technology Scaling and SEU Cross Sections

- Increased sensitivity, yet lower likelihood of direct strike on a given sensitive node

At low LETs there must be a direct strike on a fin



For High LET particles Bulk FinFETs look like planar counterpart
Large charge cloud encompasses multiple fins/devices.

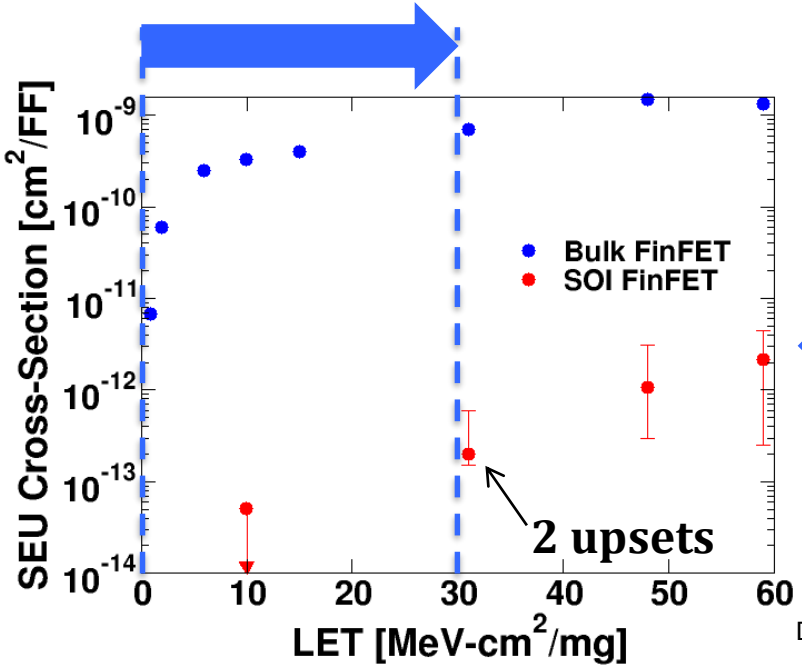
32 nm PDSOI commercial parts have smaller SEU cross section

After, P. Nsengiyumva *et al.* IEEE Trans. Nucl. Sci., vol. 63, no. 1. After, R. H. Harrington *et al.* NSREC REDW, 2015.

SEUs in SOI FinFETs

- SOI FinFETs have been found to be remarkably hard
- Increased LET_{th} attributed to smaller and shorter SETs

~20x increase in LET_{th}

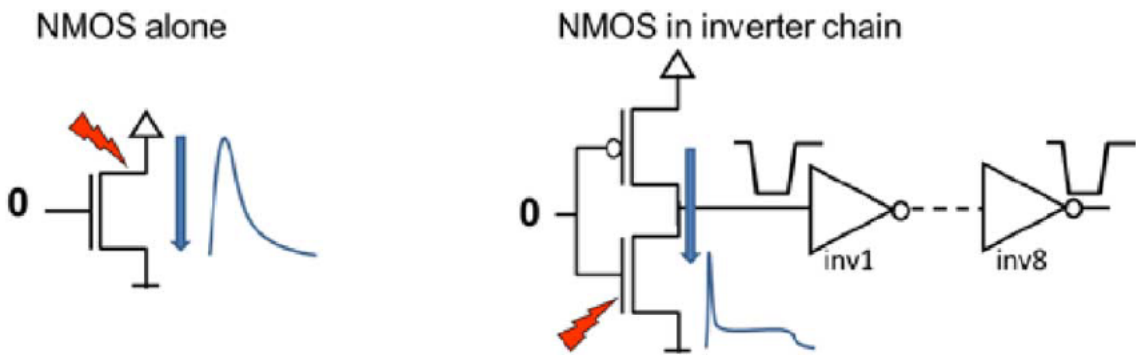


SOI shows 3-4 orders of mag. lower cross sections at high LET (consistent with historical trends)

D. Ball *et al.* IEEE Trans. Nucl. Sci., In Press.

SET propagation in sub-65 nm

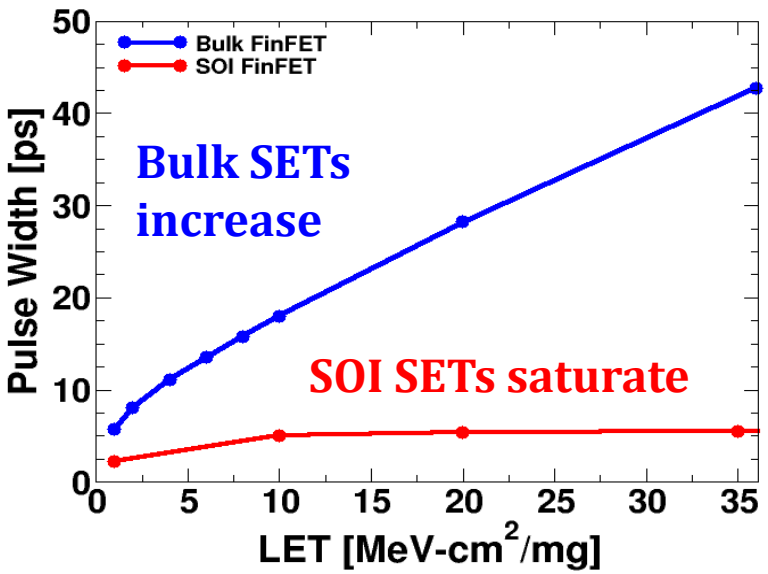
- Soft errors dominating combinational logic over memory for technologies below 65 nm
- Propagation of SETs can induce an error when
  - A sensitive logic node is struck
  - An open path to a latch or memory element exists
  - SET has sufficient amplitude and width
  - SET arrives during “window of vulnerability”



V. Ferlet-Cavrois et al., IEEE Trans. Nucl. Sci., vol. 53, no. 6,.

SET Error Rates and Scaling

- SETs resulting in an SEU is improved with the introduction of SOI
  - Small active region limits total charge collected
  - For SOI FinFETs SET approximately the switching speed of inverter chain



D. Ball *et al.* IEEE Trans. Nucl. Sci., In Press.

SOI (FinFETs and Planar) reduce SET pulse widths.

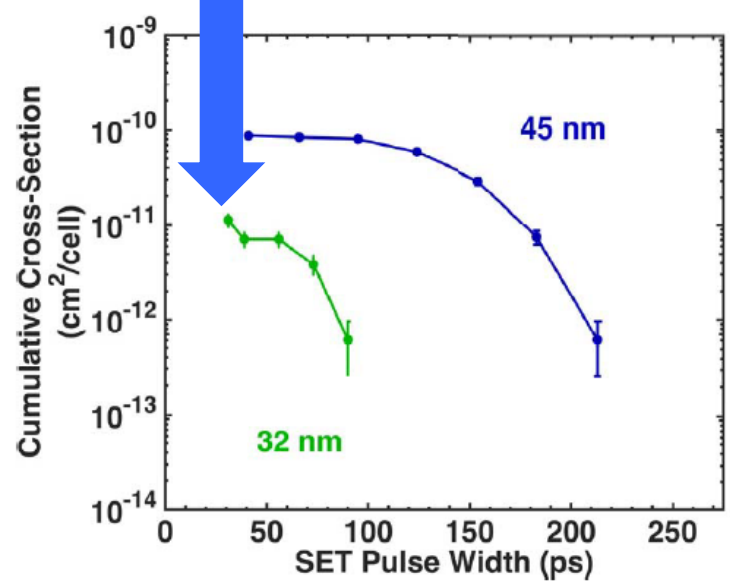
Pulse width plays an important role

SET Pulse Widths in sub-65 nm

- Can no longer ignore small pulse widths
- Traditional approaches for predicting SET-induced SEU breaks down

Small SET pulse widths are now on order of clock speed

Now PW of 50 ps can result in an error

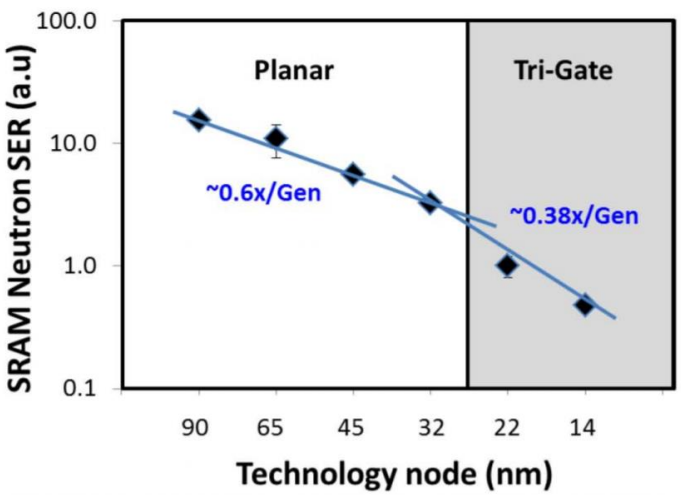


Errors from low LET particles will now be important for SER prediction

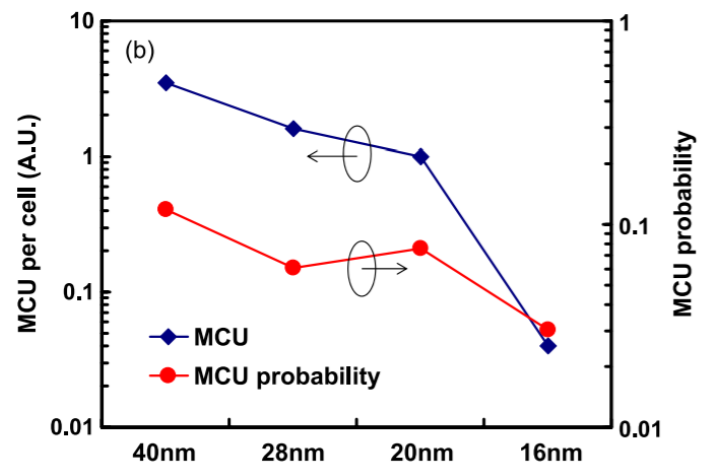
R. H. Harrington *et al.* IEEE Trans. Nucl. Sci., vol. 64, no. 8

Increased Packing Densities

- Competing factors
  - Smaller cross-section per sensitive node
  - Increased number of nodes in a given area
- Overall SER is affected by many factors
  - Generally reducing with technology scaling
- MCUs make up non-negligible fraction of total upset
  - Important environments where nuclear reactions present



N. Seifert *et al.* IEEE Trans. Nucl. Sci., vol. 62, no. 6.



Y.-P. Fang *et al.* IEEE Trans. On Dev. And Mat. Rel., vol. 16, no. 2.

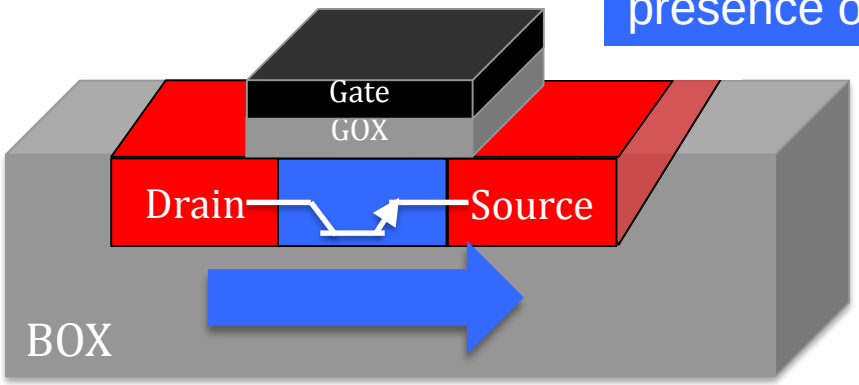
Single Event Characterization

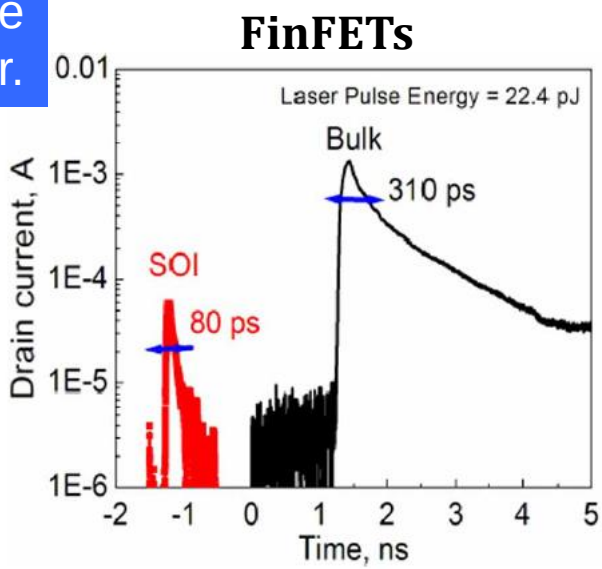
- **What are the contributing factors to SEE tolerance?**
  - Geometry, doping, parasitic effects…
- Experimental Characterization
  - Pulsed laser (Single and Two-photon Absorption)
  - Heavy ion (microbeam and broadbeam)
  - 3D Hydrodynamic simulations
  - Radiation transport simulations
  - Broadband oscilloscopes
    - *Often transients push/exceed the bandwidth capabilities of equipment*
  - High speed packages and bias tees

Parasitic Effects

- SOI devices are susceptible to Parasitic Bipolar effects
- However you must consider overall circuit operation
  - 32 nm PDSOI cannot ignore parasitic bipolar
  - sub-20 nm FinFET not likely to result in SEU

Very small transients despite presence of parasitic bipolar.



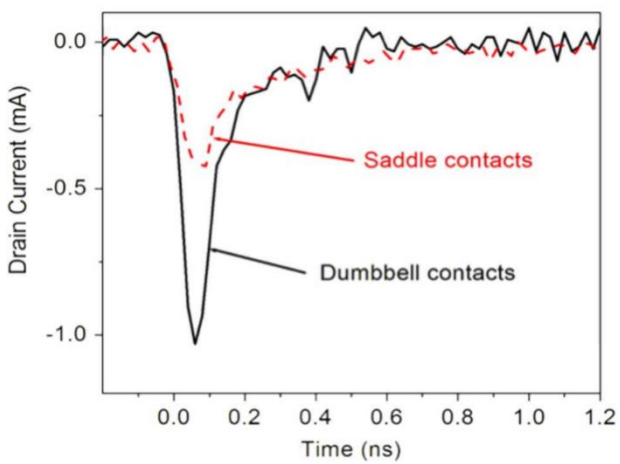


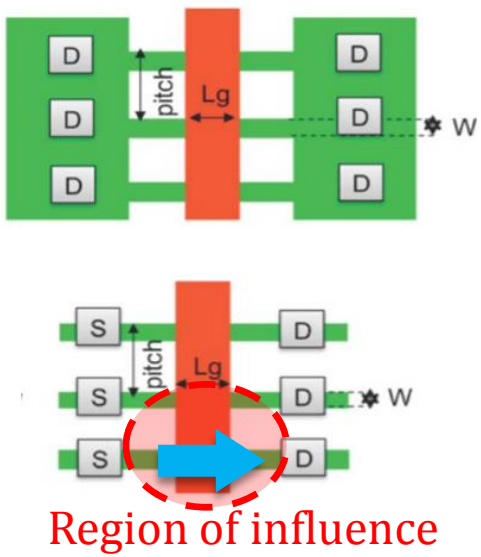
F. El-Mamouni *et al.* IEEE Trans. Nucl. Sci., vol. 59, no. 6.

SET Geometry Dependence

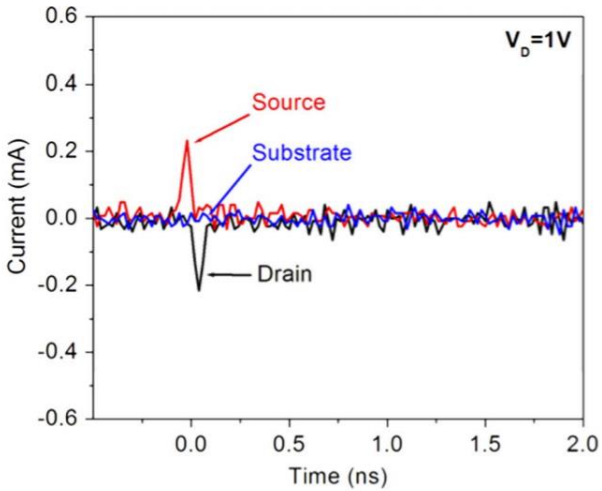
- Single Event Transient is geometry dependent
  - Potential collection from multiple fins
  - Large active area may not be from channel (drain region)
  - Track structure on the order of device dimensions results in shunt effect

Bulk FinFETs





FinFETs $w_{fin} = 20nm$

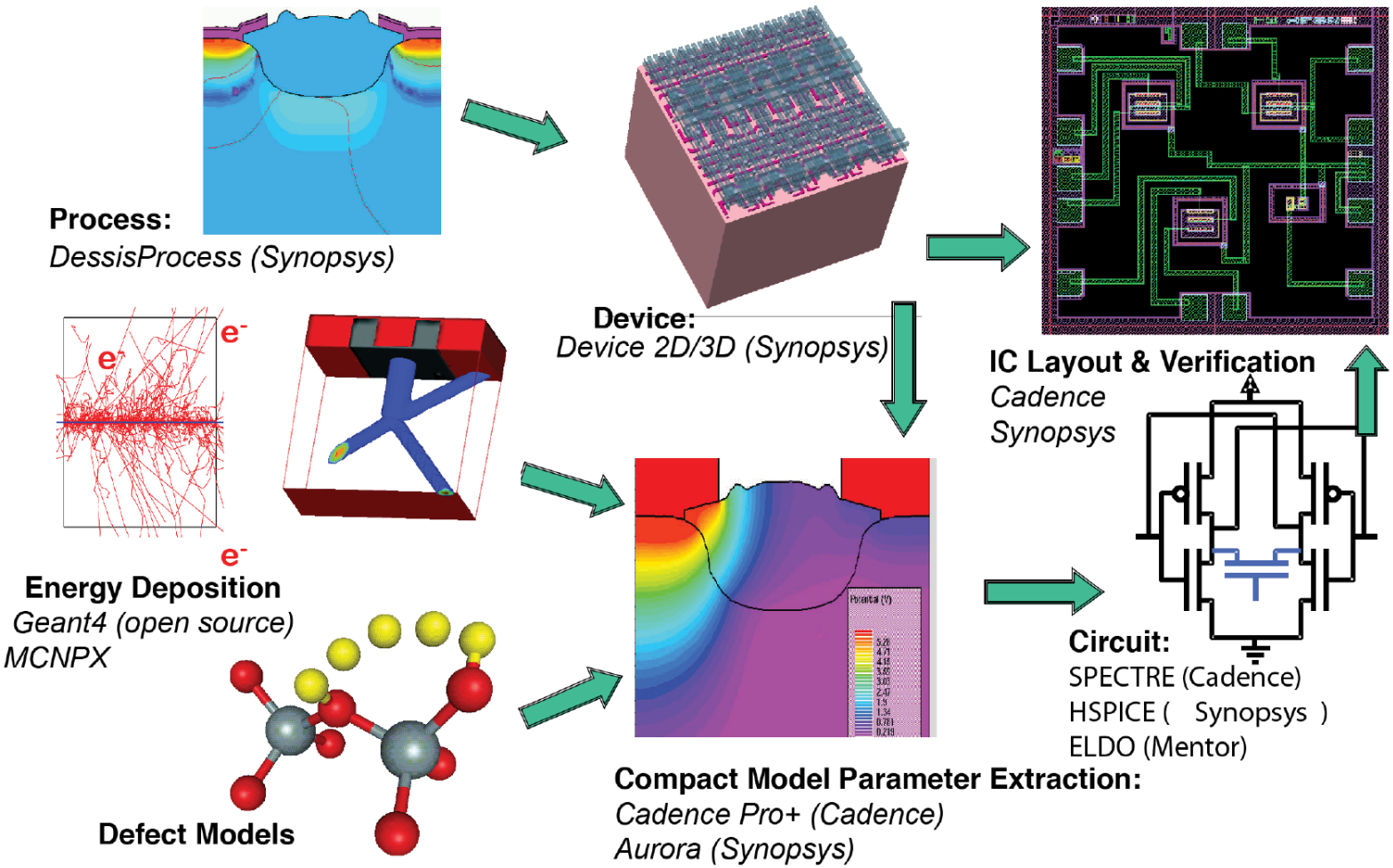


F. El-Mamouni *et al.* IEEE Trans. Nucl. Sci., vol. 59, no. 6.

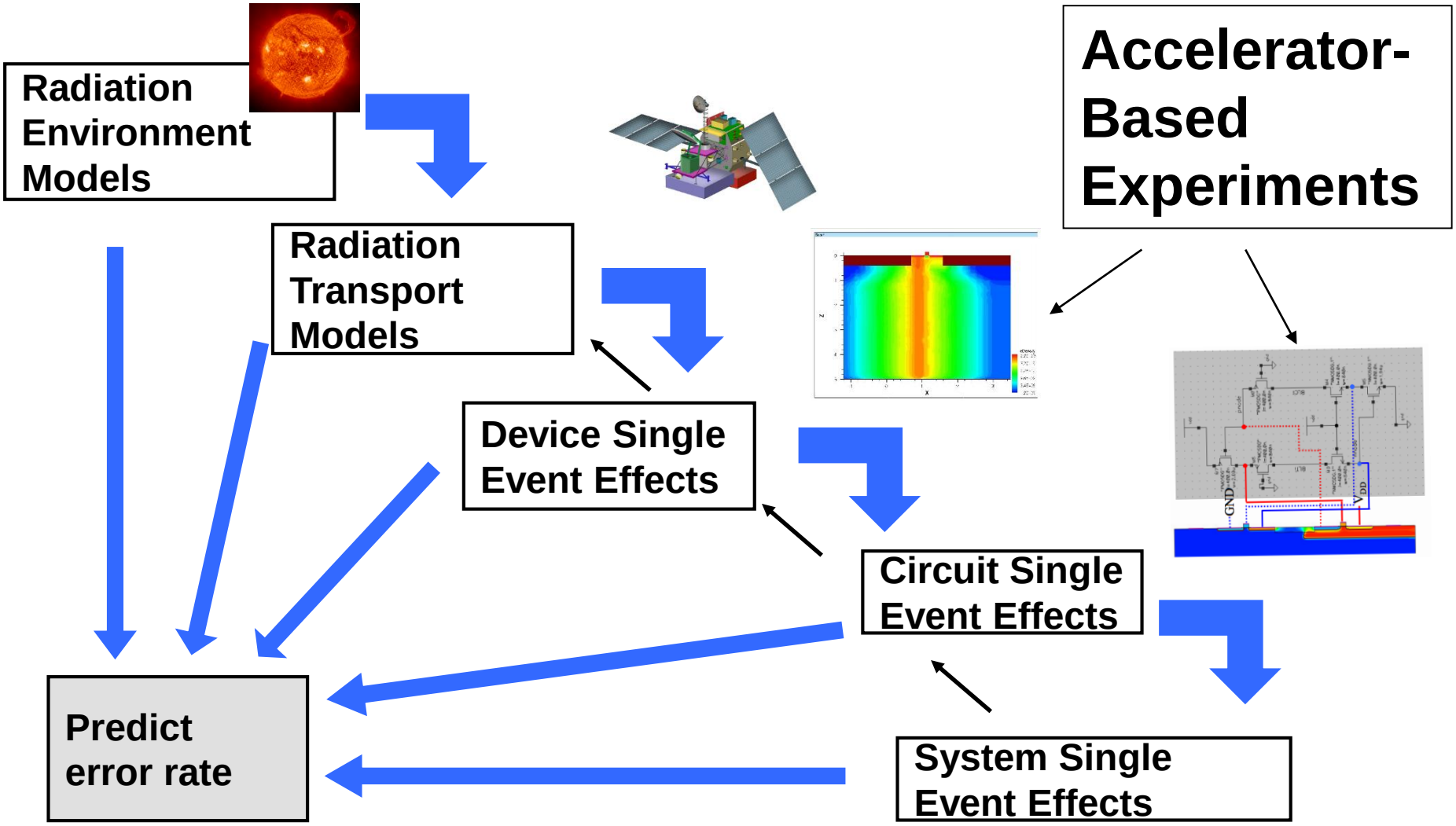
3D Modeling

Necessary to understand how devices will behave in particular radiation environments

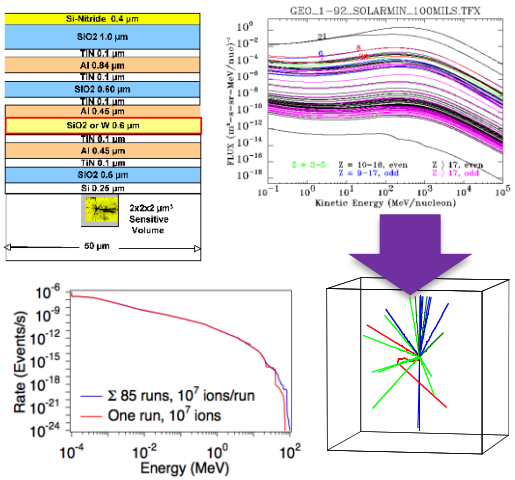
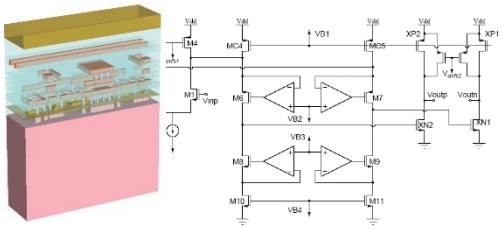
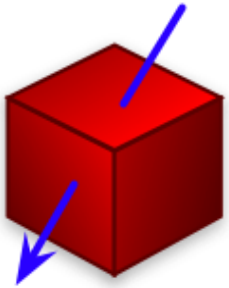
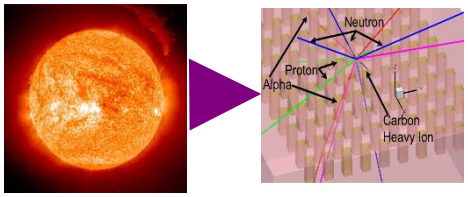
Simulation Capabilities



Radiation Effects Analysis
Automated Model Connections

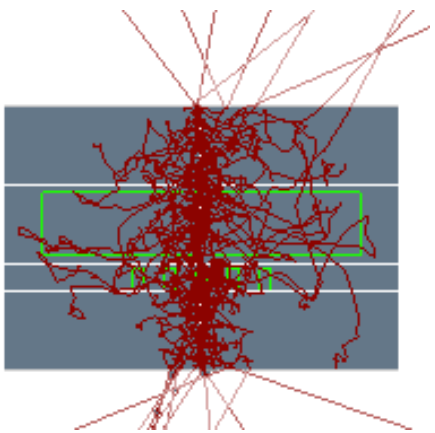


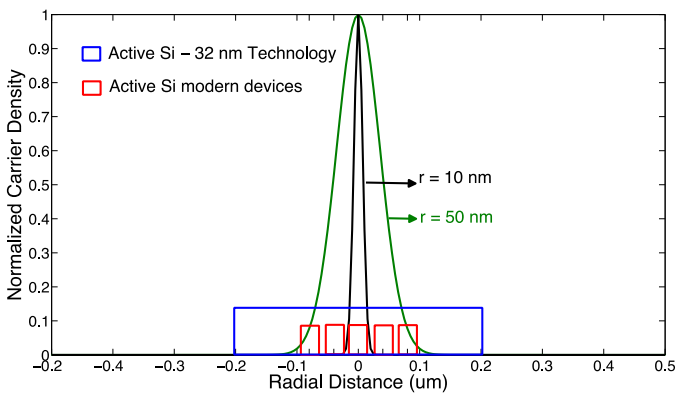
Virtual Irradiation Capabilities

	CREME96	CREME-MC	VU Research
Device/Circuit/System Virtualization			
Radiation Event Generation			
Response Prediction	Integral over path length Distribution + critical charge	Multi-volume Calorimetry + Charge-collection models + Critical charge	Calorimetry TCAD or SPICE in the loop coincidence analysis

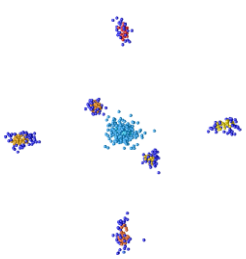
Modeling Considerations for Scaled Technologies

- TCAD simulation tools assume
  - Gaussian spatial distribution (50 nm Radius)
  - Carrier generation based on LET
- Assumption breaks down for highly scaled technologies
  - Average carrier generation (extreme events likely important)
  - 50 nm Gaussian
- New approach to modeling bridge gap between Radiation Transport and TCAD

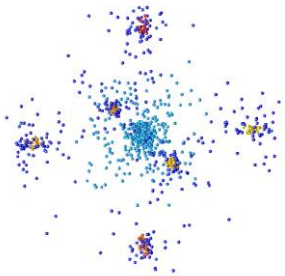




Equilibrated



Hot Carrier Injection



Alternative Memories

Paradigm Shift: Storage Node

- Present
  - **Moving electrons** (charge-storage)
    - SRAM
    - DRAM
    - Flash
- Emerging
  - **Moving spin** (electron spin)
    - (STT-) MRAM
  - **Moving atoms**
    - **RRAM**
    - **CBRAM**
    - Nanomechanical
    - Etc.

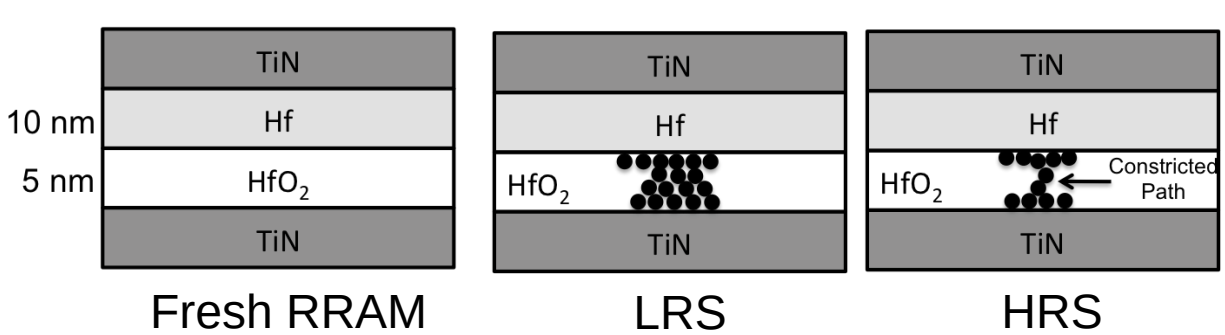
Currently commercially viable and have shown very promising radiation tolerance

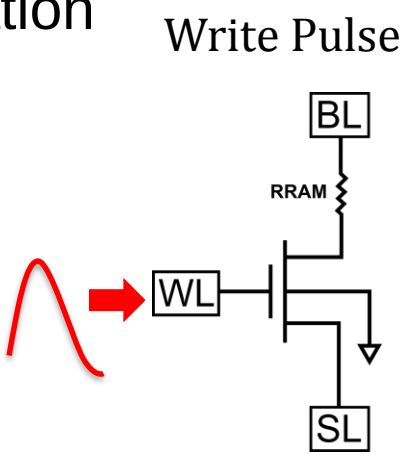
Transient noise including single events is dominant reliability issue

Material wear-out (endurance) is dominant reliability issue

Oxide-based RAM

- RRAMs have a binary high or low resistance state
  - Conductive filaments of oxygen vacancies
  - ε-field moves vacancies,
  - high resistance (HRS) or low resistance (LRS) states.
- Conductive Bridge RAM (CBRAM) similar principal
  - Moving ions
  - Particularly sensitive to material degradation

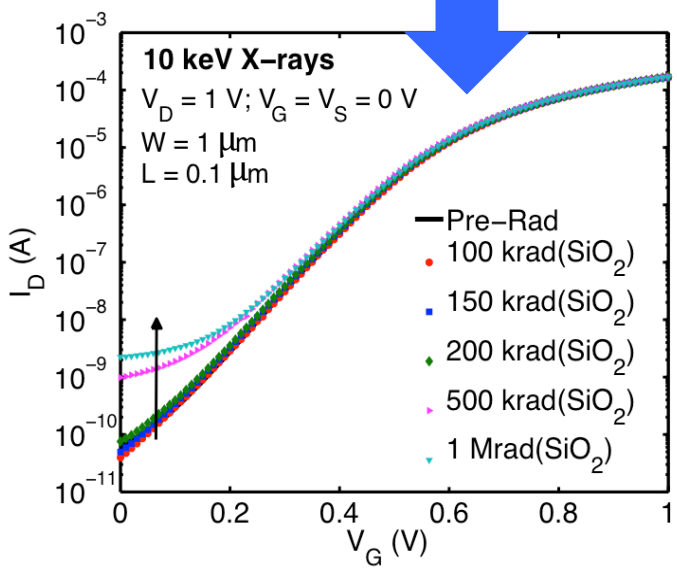


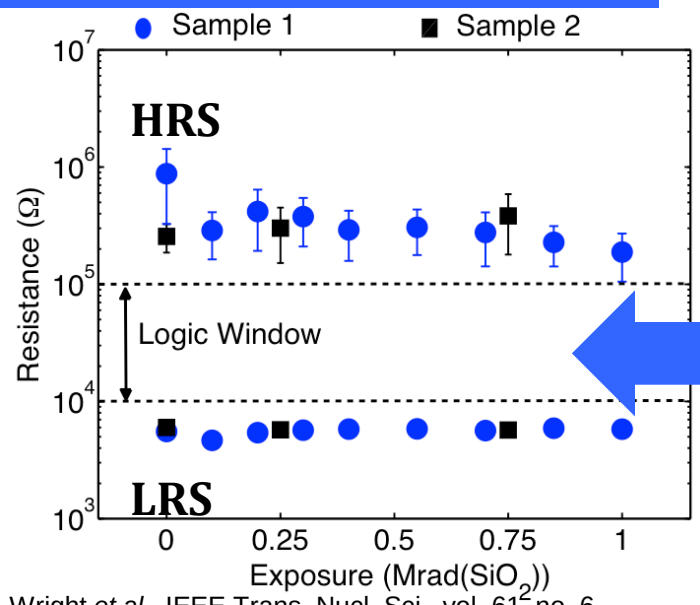


TID in RRAM & CBRAM

- Memory element alone has been shown to be tolerant to high TID for RRAM
- Recent study on CBRAM (not shown here) Y. G.-Velo *et al.*, IEEE Trans. Nucl. Sci., vol63, no. 4.
  - Just memory element (no CMOS circuitry)
  - Maintained logic window up to 10 Mrad (SiO_2)

Despite presence of **vulnerable access transistor** RRAM is still able to maintain performance





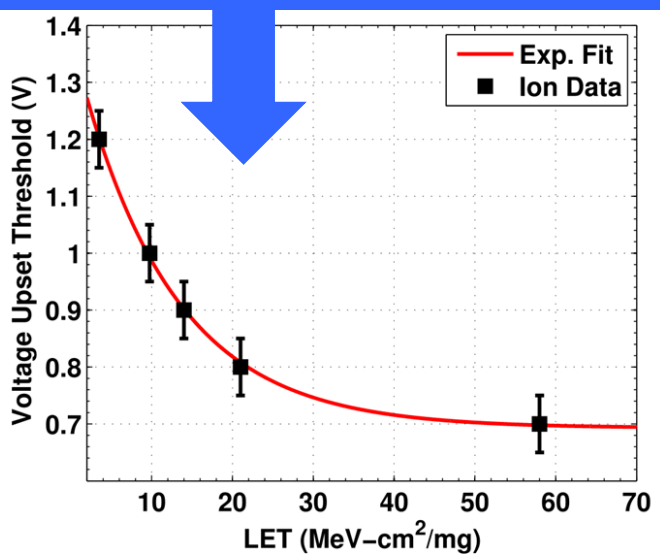
No loss of logic window

S.L. Weeden-Wright *et al.*, IEEE Trans. Nucl. Sci., vol. 61, no. 6.

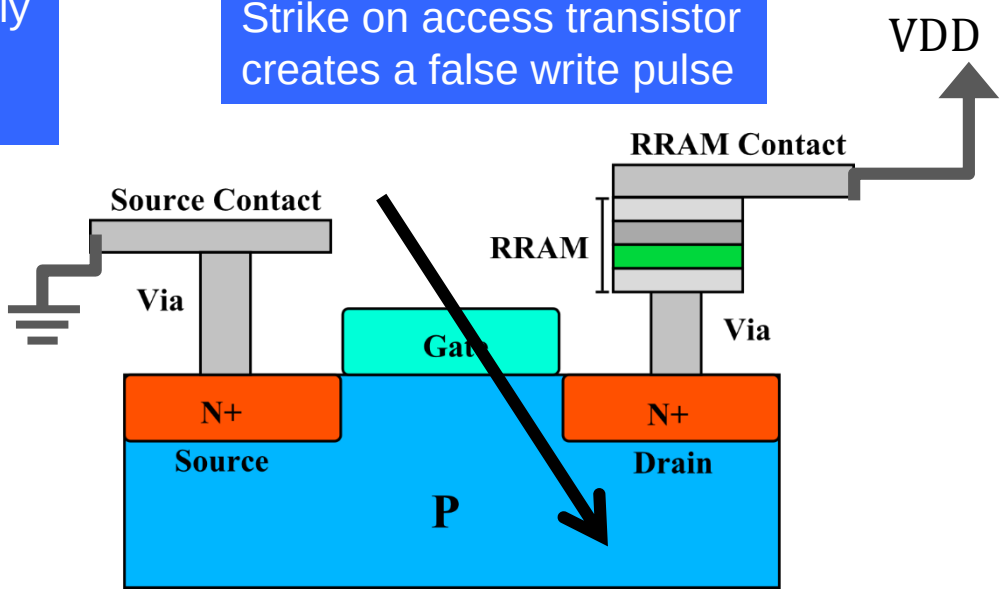
SEE in Oxide-based Memories

- Vulnerability dependent only on CMOS
- Laser or ion strike to access transistor when in write cycle (i.e. V_{DD} is applied)
  - Window of vulnerability <0.5%
- Strikes can be cumulative (multiple events drive HRS to LRS)

Tolerance to low LET particles. Highly dependent on the CMOS process used.



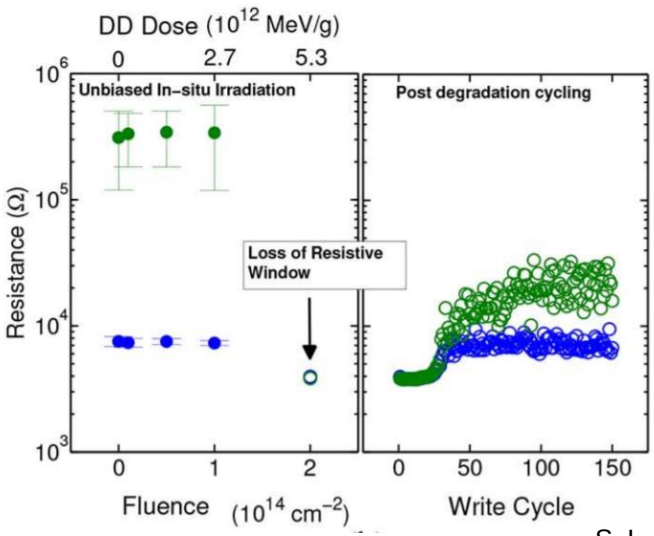
Strike on access transistor creates a false write pulse



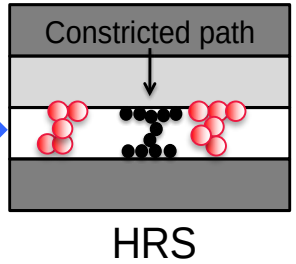
W. G. Bennett *et al.*, IEEE Trans. Nucl. Sci., vol. 61, no. 4

DD effects in RRAM

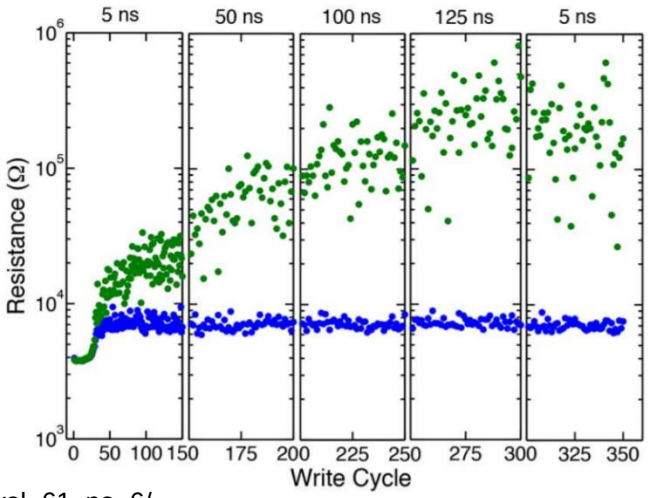
- Oxide-based RRAMs are susceptible to displacement damage effects
  - 1.8 MeV Proton irradiation collapse memory window
  - Through percolative oxide breakdown
- RRAM recovered by applying longer HRS write cycle



Additional Conduction paths from displacement damage



Full recovery of resistive window



S. L. Weeden-Wright *et al.* IEEE Trans. Nucl. Sci., vol. 61, no. 6/

Emerging Memory: General Observations

- Change from charge-based to spin/atomic – based arrangement
  - Can reduce TID and SE vulnerability
  - Increased wear-out concerns (material breakdown, etc.)

- CMOS integration poses biggest vulnerability
  - Currently CMOS-based access circuitry required
  - Read/Write etc.
  - Vulnerability of CMOS leads to SE/TID vulnerability of memory element
  - Depend on the operating context for each technology

Takeaways

Technology	TID	SEE	Other Considerations
Sub-65 nm FDSOI Planar	• Large BOX • Low Doping • Capacitive coupling with back gate	• Small active region • Potential for low SEU cross-sections (dependent on active area)	
Commercial 32 nm PDSOI	• Higher Doping • Less capacitive coupling with back gate • TID tolerance $\leq 1Mrad\ (SiO_2)$	• Small active region • Low SEU cross-section • Low LET_{th}	• Standard technology
Bulk FinFETs	• Higher Doping • No BOX • TID tolerance $\leq 1Mrad\ (SiO_2)$	• Small active region • Low SEU cross-section • Low LET_{th}	• Not as widely available as 32 nm PDSOI counterpart

Thank you!

- I would like to thank the Institute for Space and Defense Electronics as well as the Radiation Effects Group at Vanderbilt.
- Thank you!

Questions?