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Trends in Radiation Effects for sub-65 nm Technologies

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Radiation-induced degradation and soft errors in electronics are important reliability issues for various space, defense and commercial applications. The continual miniaturization of CMOS technologies and the introduction of multi-gate device structures to mitigate short channel effects have had mixed consequences for radiation tolerance. The aim of this presentation is to review the current radiation-effects trends dominating sub-65 nm technologies for space and defense applications. Device structure and doping levels determine sensitivity to Total Ionizing Dose (TID) effects (e.g. sub-threshold leakage, threshold voltage shifts). Thinner insulators and higher dopings associated with scaling have reduced TID effects; however, fully-depleted silicon-on-insulator (FDSOI) devices, typically used to mitigate transient effects, have been shown to exacerbate TID effects due to trapped charge in the buried oxide. Typically parts are tested up to a maximum dose of 1 Mrad and special considerations should be made for the validity of these trends at the high doses of interest in the LHC community. Beyond TID effects, Scaling has resulted in increased sensitivity to Single Events (soft errors). This trend is attributed to the reduced operating voltages, decreased feature sizes, and higher packing densities, which result in low critical charge per node and more nodes within a region of influence of a single event. There is an increased interest in the use of commercial-off-the-shelf (COTS) parts in radiation environment because of accessibility and cost; here, the primary concern for radiation effects when using COTS is Single Event Latchup sensitivity which is tested using two photon absorption techniques. A brief discussion on radiation tolerance of beyond CMOS and other emerging technologies will be provided.

Summary

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Session Classification: Invited Talk