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Hardware Trigger Processor for the ATLAS MDT System

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We are developing a low-latency hardware trigger processor for the Monitored Drift Tube system in the ATLAS muon spectrometer. The processor will fit candidate muon tracks in the drift tubes in real time, improving significantly the momentum resolution provided by the dedicated trigger chambers. We present a novel pure-FPGA implementation of a Legendre transform segment finder, an associative-memory alternative implementation, an ARM (Zynq) processor-based track fitter, and compact ATCA blade architecture. The ATCA architecture is designed to allow a modular, staged approach to deployment of the system and exploration of alternative technologies.

Summary

The ATLAS Monitored Drift Tube (MDT) trigger system will be implemented as a set of 32 or 64 ATCA blades, each handling one or two sectors of the ATLAS muon system. Each ATCA blade will provide up to 144 optical transceivers capable of operating at 10 Gbps.

MDT hits are received in real time over GBT links from the detector with minimum latency. Simultaneously, regions of interest (ROI or seed tracks) are provided by the ATLAS muon sector logic to the trigger processor.

Matching of MDT hits to regions of interest will be performed in an FPGA on the blade. Tube coordinates are transformed to convenient chamber-local coordinates and drift time converted to a drift radius. The processed MDT hits are then passed to sector processors on mezzanine boards.

Two alternative mezzanine board designs are under consideration. The first uses content-addressable memory devices (also known as Associative Memories or AM).The AM devices store a library of all possible track patterns and compare actual hits against the track library in a massively parallelized way.

The second uses FPGA logic to implement a Legendre transform based segment finder. This logic evaluates in parallel a total of 128 possible track segment angles for each MDT hit, calculating in a fast FPGA pipeline the offset of each track candidate from an arbitrary origin for each angle and hit. The (angle, offset) pairs are used to fill a 2D histogram, with the maximum peak in the histogram representing a likely track where a number of tubes “agree” on the position and angle of a possible track.

Each station (inner, middle, outer) will process hits and identify track segments independently. All hits are then transferred back to the blade, where a Xilinx Zynq FPGA with embedded ARM processor cores will be used to evaluate a final parameterized track fit. We expect the resulting p(T) to be substantially more precise than that provided by the dedicated trigger chambers, and approach the resolution currently achieved by the off-line fitting.

A detailed conceptual design with extensive simulation studies is being prepared now, to be published in the ATLAS TDAQ TDR. A first generation of hardware prototypes is planned for 2018-2019, with a full system ready for installation during LHC Long Shutdown 3.

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