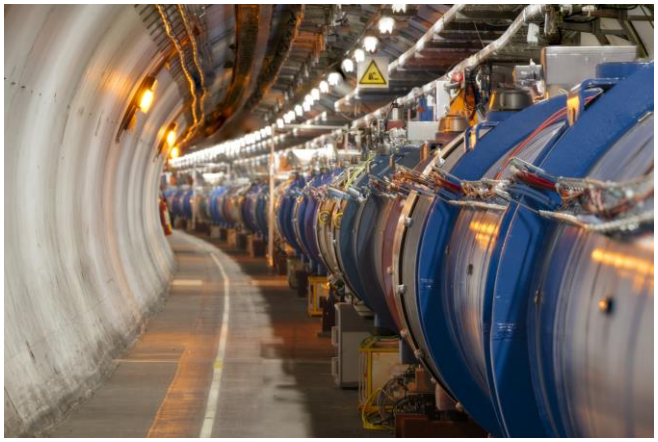
SmartFusion2 and Artix 7 radiation test results for the new developments

G. Tsiligiannis, S. Danzeca (EN-STI-ECE)

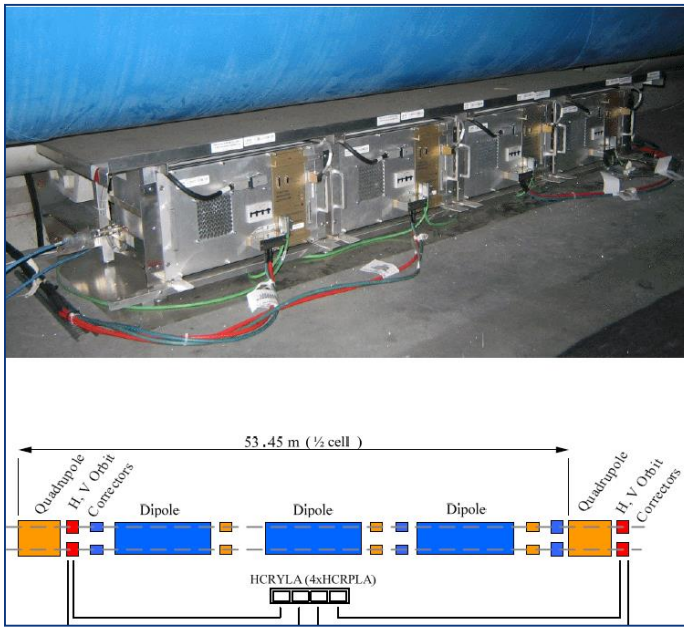
Outline

- CERN accelerator FPGAs
- SmartFusion2 Characterization
- SmartFusion2 System Level Test
- SmartFusion2 System on Chip Test
- Artix7 Application level test
- Conclusions and Outlooks

CERN Accelerator FPGAs



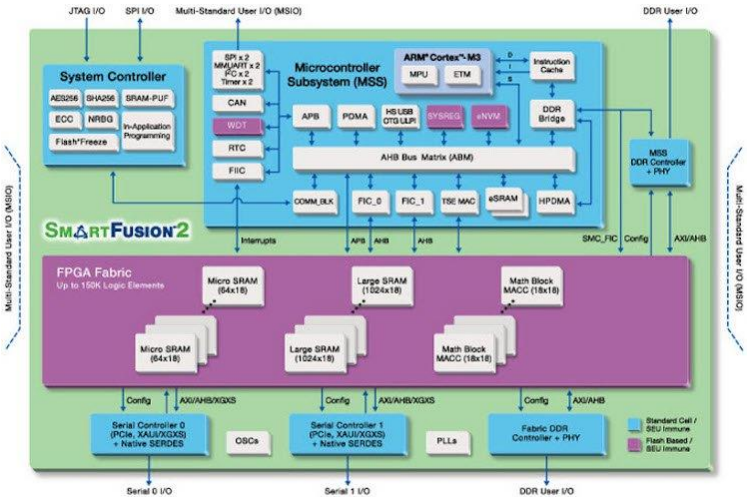
- Increasing needs for new electronics developments for HL-LHC
- Harsh Radiation Environment in the tunnel areas
- Thousands of installed equipment
  - RadHard electronics are prohibitive due to cost
  - COTS are the only solution for most systems
- The **reliability** of the CERN equipment is a main concern
- The **criticality** of the equipment can be very high
- Tiny fractions of the stored beam are sufficient to quench a superconducting LHC magnet or even to destroy parts of the accelerator
- Traditionally, FLASH based FPGAs have been used
  - **ProASIC3** being the main part in most systems because of the very low SEU cross section and insensitivity to SEL
  - TID is a showstopper for most cases
- Several efforts to improve computational power, size, cost and TID endurance
  - **New FLASH based FPGA** components
  - **SRAM based FPGAs** approach



Why testing SmartFusion 2 and the difference with the ProAsic3

- ProASIC3E is a 130nm Flash based FPGA
  - Flash based FPGA are known to be more tolerant to SEU
  - Previous tests show good TID performances: ~500 Gy
  - Lost reprogrammability at ~200 Gy

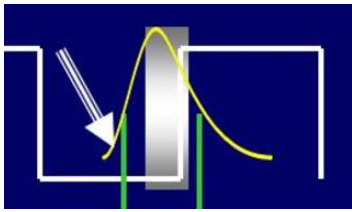
- **SmartFusion2** is a **65nm Flash based FPGA**
  - FPGA fabric + **ARM Cortex M3**
  - **DSP** blocks integrated
  - Interesting device for communication protocol implementation and signal processing



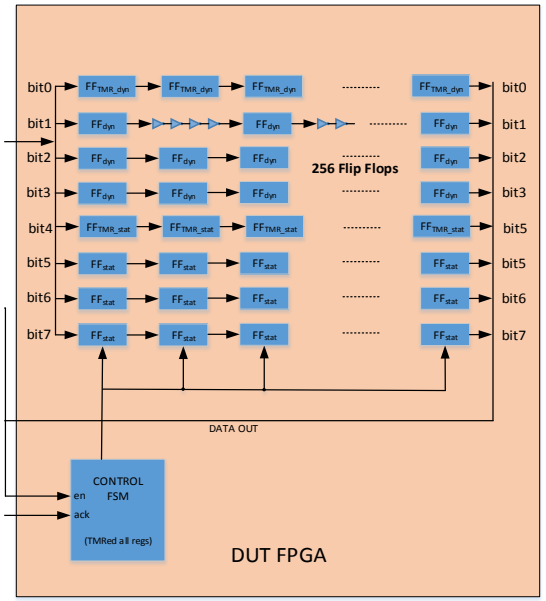
SmartFusion2 Characterization

- Followed standard FPGA testing methodology [1] from NASA with several adaptations on the embedded components under test
- Full characterization under 200MeV proton beam at PSI
- Chains of Flip Flops using normal configuration, TMR, SET enhancement (NOT gates) 8 chain x 256FF
  - Normal FF → 1.14E-14 cm^2/bit
  - TMR FF → 3.79E-15 cm^2/bit

TMR FF X3 less sensitivity!



- SRAM embedded blocks 21 blocks x 18kbit (accessible from the FPGA): static tests with CKB pattern
  - LSRAM cross section → 2.24E-14 cm^2/bit
- PLL: tested for loss of lock and for jitter/synchronization issues
  - loss of lock → 4.76E-12 cm^2

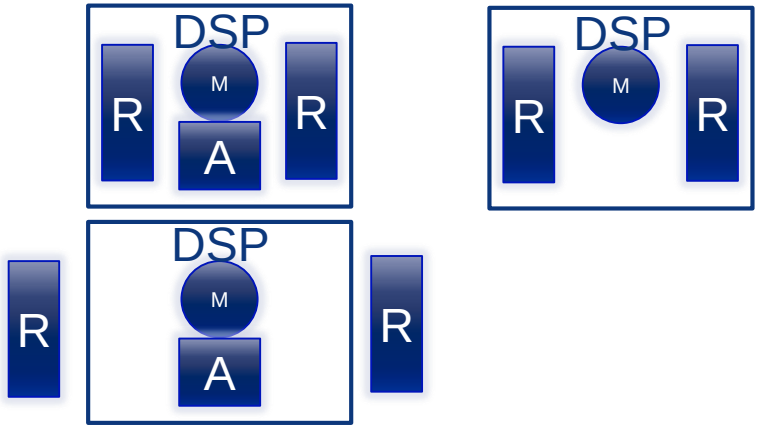


[1] M. Berg, "Field Programmable Gate Array (FPGA) Single Event Effect (SEE) Radiation Testing", NASA Electronic Parts and Packaging (NEPP)

SmartFusion2 Characterization

- Multipliers: registered/non-registered I/Os under two different configurations: with/without accumulator -> 4 different configurations in total
  - I/O registeres do not affect the cross section → the accumulator adds sensitivity
  - Without Accumulator: 1.44E-11 cm^2
  - With Accumulator: 6.84E-12 cm^2

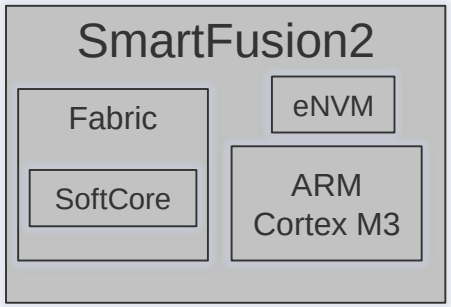
Accumulator X2 less sensitivity!



- Tests at application level (only FPGA)
  - **Counter Application Test**: 3 different counter implementations compared with a golden reference
    - Normal counter → 1.7E-14 cm^2
    - TMR → 4.73E-16 cm^2

TMR counter is ≈2 orders of magnitude more robust

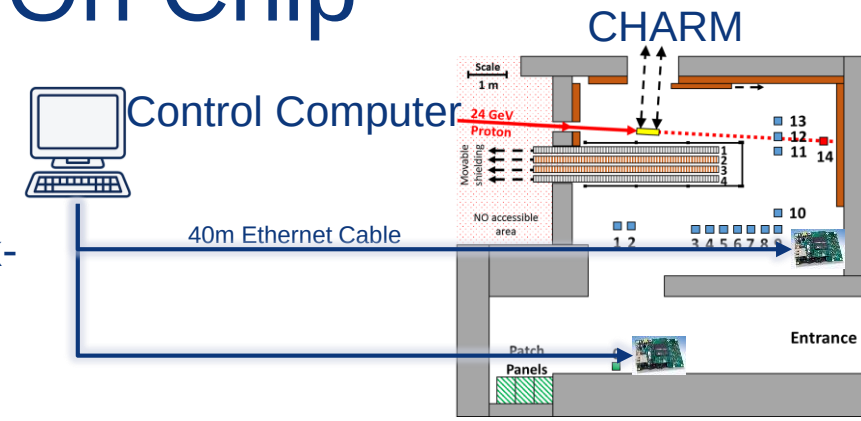
  - **SoftCore application test**: The application was reading and writing a TMRed SRAM
    - No SEUs observed in the triplicated memory -> Nor in the system

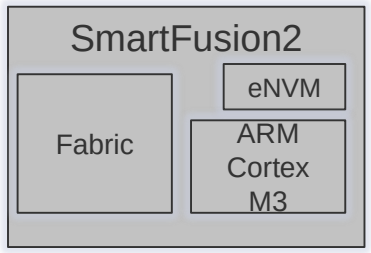


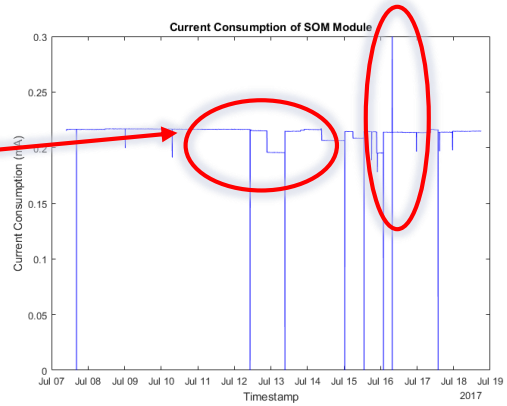
- TID limit→ Between 480Gy (multiply accumulator setup) and 660Gy (Flip Flop chains)
- Reprogrammability → lost at 70Gy BUT recovered after one day of annealing
- Next step → **System Test – Embedded ARM core**

SmartFusion2 System On Chip

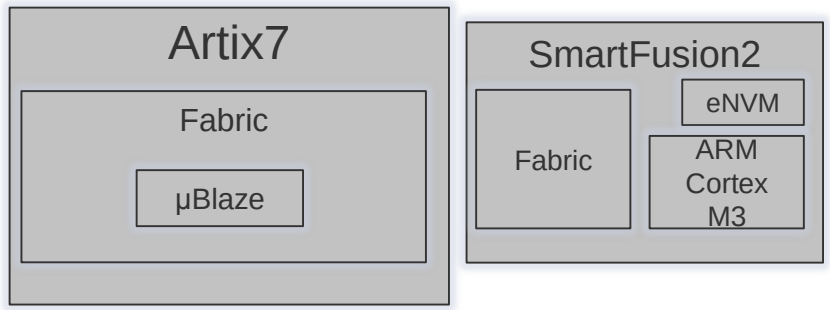
- Test the **embedded ARM Cortex-M3 in a communication application**
  - Transmit an array of data and verify on back-end the correctness
  - Packet size: 1kbyte
  - Protocol: Raw Ethernet
  - Application stored in the eNVM
- **16Mbps** average speed
- 400Gy of total dose received
- Three weeks of irradiation in total
- Failure rate: 12 packets/144GBytes/9.3E+9HEH (R10)
- Lost packets: 6088 packets out of 667GBytes/3.8E+10 HEH(G0)
- G0 → no system losses
- R10 → 3 drops of current/loss of communication
  - Recovered fully after power reset



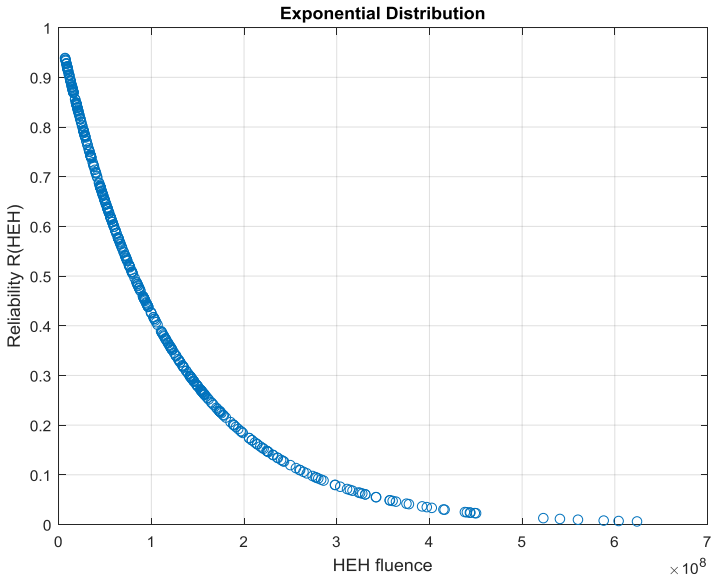




Artix7 Characterization and System Level Test



- Artix7 is Xilinx SRAM based FPGA → weak part is Configuration Memory (CRAM)
- First part of evaluation was testing at PSI with 200MeV protons of the CRAM and the block memory (BRAM)
  - CRAM σ = 9.37E-15cm^2
  - BRAM σ = 8.7E-15cm^2
- System level test! Same principle with previous setup with the difference that processor is soft core (fabric)
  - Using a MicroBlaze, we created an application → Ethernet Echo server, in order to test also SRAM based FPGAs for potential use at accelerators for Ethernet communication
- Tests performed at CHARM for two weeks in positions G0 (low intensity) and R1 (low to medium intensity)
- Since metric is fluence, not time, the metric is: Mean Fluence To Failure (MTTF) → the average fluence from all the samples where the design fails due to accumulated SEUs on the CRAM
- MFTF = **1.17E+8** corresponds to a 40% successful operation for a year at the RRs of LHC.
- Results confirm that such devices can be used for non critical applications



Conclusions and Outlooks

- SmartFusion2 is quite robust to SEU events and tolerant to TID up to 500-600Gy.
- The big problem is the reprogrammability lost at 70Gy
  - In a low dose rate environment could behave better
- The SEU sensitivity in an application can be reduced by 2 orders of magnitude if TMR is implemented
- The embedded ARM Cortex showed very good performances in the communication application
  - Some other mitigation strategies could be implemented at software level and/or at protocol level to avoid lost packet or errors on the packets
- Artix 7 showed that a possible implementation of a communication protocol is possible in radiation area implementing a soft-core in the FPGA.
- The MFTF has been defined and estimated showing that a possible use in the LHC cavern for low critical application is possible

Thank you

Backup Slides

SF2 results

Counter Application	
Chain	**XS (cm^2)**
Multiple Counter Application	2.46E-14
Double 512bit counter	1.70E-14
Double 512bit TMRed counter	4.73E-16

Multiplier version	SEU	Fluence	XS (cm^2)
MANR	27	8.48E+11	6.37E-12
MAR	29	8.48E+11	6.84E-12
MR	65	8.48E+11	1.53E-11
MNR	61	8.48E+11	1.44E-11

Flip Flop Average XS	
Chain	**XS (cm^2/bit)**
0 (TMR)	3.79E-15
1(WSR dyn)	1.78E-14
2(dyn)	1.22E-14
3(dyn)	2.59E-14
4(TMR st)	3.51E-15
5(st)	1.14E-14
6(st)	6.49E-15
7(st)	5.68E-15

Chain	XS (cm2)
PLL Flip Flop	5.25E-10
PLL TMR Flip Flop	7.24E-10
PLL Lock	4.76E-12

Test	Dose of first failure (Gy)
Flip Flop config 1 (Nov)	650
Flip Flop full TMR (Nov)	660
Flip Flop config 2 (Dec)	580
MAC (Nov)	480
Counter app (Dec)	610

SmartFusion2 System Level Test

Prototype double-channel card with Smartfusion2 FPGA

Current leads require an isolated version

- Resistive measurements relative to precision on-board references.
- 8 x Measurements (Sensor/Reference * current flow Positive/Negative * voltage Straight/Inverse) to remove thermoelectric effects, voltage offsets and OpAmp common mode error.
- Two independent channels supporting isolation.
- Isolation needed for channels on DFB current leads or when fault to ground. Isolation provided by the use of the ISO150AU.

- ***Initially, this new design was targeting non-radiation applications, but a test at CHARM was planned to explore potential use in the LHC tunnel.***

SmartFusion2 System Level Test

4 FPGA code versions

#1: Safe/Onehot, No TMR

#2: Safe/Onehot, TMR

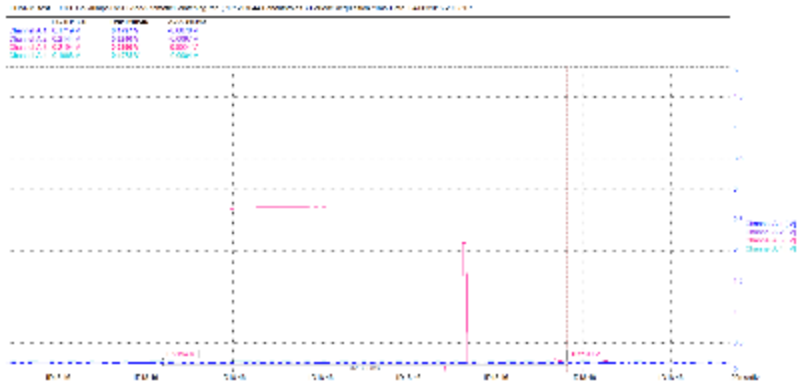
#3: Hamming 8/4, TMR

#4: Hamming 8/4, TMR with distant FFs

SEU/SET
#1 → 4 (3 on single FF, 1 complex on logic)
#2 → 2 (1 reset, 1 likely at the non-TMRed illegalpipe)
#3 → 1 (on median logic, diagnostics only, transparent)
#4 → 1 (wdog FSM reset, diagnostics only, transparent)

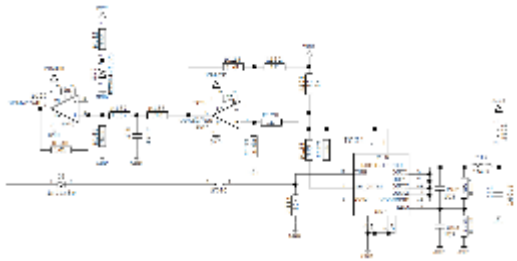
Cross-sections for SEL
Total HEHeq Fluence: 1.02 x 10^{13} cm^{-2}
# of events: 2

$\sigma_{SEL} < 1.96 \times 10^{-13}$

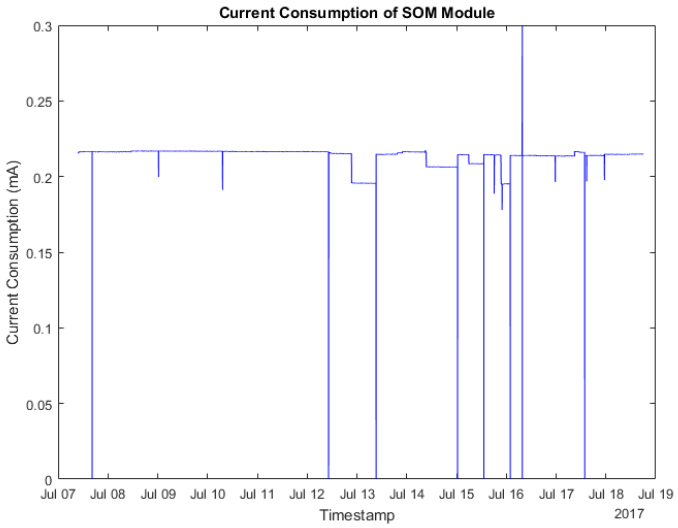


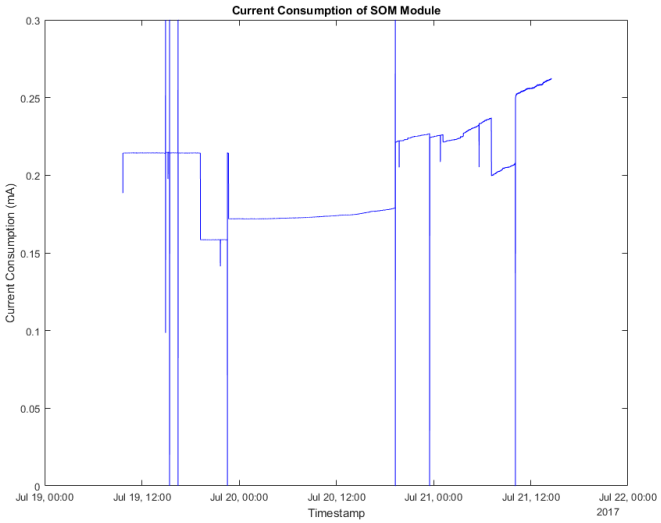
Event: The IO configuration of the card as lost, all outputs at high-Z.

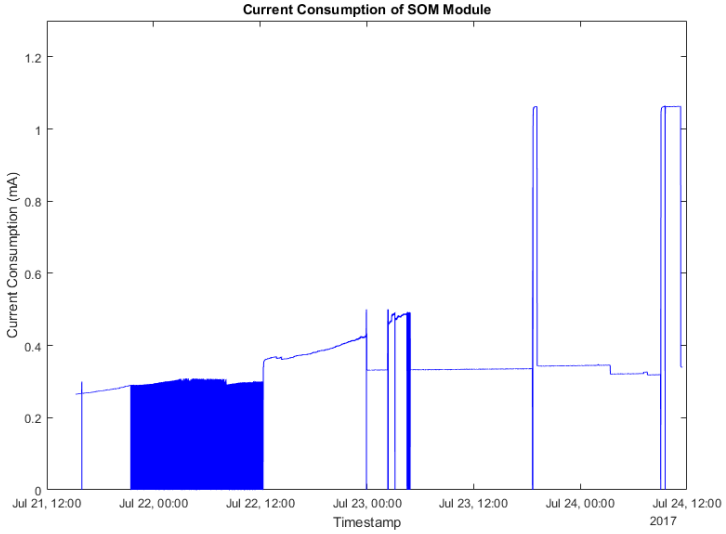
Total HEHeq Fluence: 1.02 x 1013 cm-2
# of events: 1

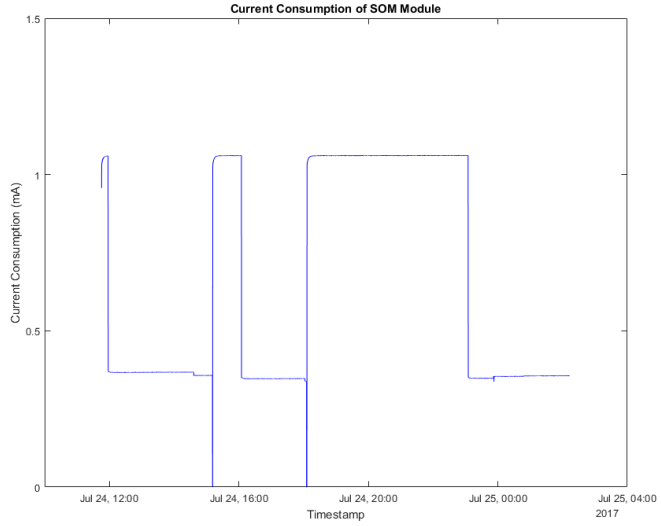


SmartFusion2 System on Module Test









Artix7 Characterization

- Completed study on characterization on different locations
  - RADECS publication: "*Radiation Effects on Deep Sub-micron SRAM-based FPGAs for CERN applications*" -> Oral
- Observed difference in sensitivity between shielded and non shielded zones:
  - Thermal Neutron Contribution!!!
- Using the R-factor to derive the HEH and the thermal neutron cross section and compare it to experimental data at ILL (thermal) and PSI and LPSC (protons and 14MeV neutrons)

$$\sigma^* = \sigma_{HEH} + R \times \sigma_{th}$$

TABLE I
CHARM IRRADIATION CAMPAIGN AT G0

Experiment	Bit flips	Fluence (HEH)	Cross Section (cm^2/bit)
BRAM N/S	483	$1.05 \cdot 10^{10}$	$3.18 \cdot 10^{-14}$
BRAM S	553	$3.15 \cdot 10^{9}$	$1.22 \cdot 10^{-13}$
CRAM N/S SEM	5651	$1.6 \cdot 10^{10}$	$2.36 \cdot 10^{-14}$
CRAM N/S RB	2566	$6.47 \cdot 10^{9}$	$2.65 \cdot 10^{-14}$
CRAM S SEM	1857	$1.86 \cdot 10^{9}$	$6.67 \cdot 10^{-14}$

N/S stands for No-Shielding, S stands for Shielding, SEM stands for Soft Error Mitigation controller of Xilinx (scrubber) and RB stands for ReadBack.

TABLE II
ILL, LPSC AND PSI IRRADIATION CAMPAIGNS

Facility	Experiment	Bit flips	Fluence (HEH)	σ* (cm^2/bit)
ILL	BRAM	290	$6.17 \cdot 10^{10}$	$3.27 \cdot 10^{-15}$
	CRAM	2172	$7.4 \cdot 10^{10}$	$1.96 \cdot 10^{-15}$
LPSC	BRAM	113	$8.1 \cdot 10^{9}$	$9.69 \cdot 10^{-15}$
PSI	BRAM	152	$1.21 \cdot 10^{10}$	$8.7 \cdot 10^{-15}$
	CRAM	1462	$1.4 \cdot 10^{10}$	$9.37 \cdot 10^{-15}$

TABLE III
R-FACTOR MEASUREMENT FOR G0

Configuration	HEH_{eq} fluence ($cm^{-2}pot^{-1}$)	Average HEH_{eq} flux ($cm^{-2}s^{-1}$)	R-factor
No Shielding	$4.16 \cdot 10^{6}$	$7.22 \cdot 10^{4}$	3.8
Shielding	$2.17 \cdot 10^{7}$	$3.79 \cdot 10^{3}$	21

TABLE IV
HEH AND THERMAL NEUTRON DERIVED CROSS SECTION

σ* (cm^2/bit)	BRAM	CRAM
σ_{HEH}	$1.19 \cdot 10^{-14}$	$1.76 \cdot 10^{-14}$
σ_{th}	$5.24 \cdot 10^{-15}$	$2.33 \cdot 10^{-15}$