First results on KINTEX-7 FPGA testing in mixed field radiation at CHARM facility

Vlad-Mihai PLACINTA

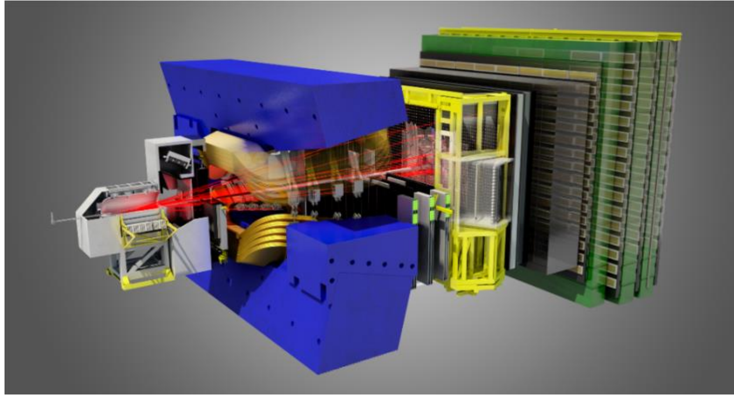
on behalf of the LHCb RICH PDMDB CHARM testing group

| vlad-mihai.placinta@cern.ch | www.nipne.ro/dpp/Collab/LHCb/upgrade.html |

Outline

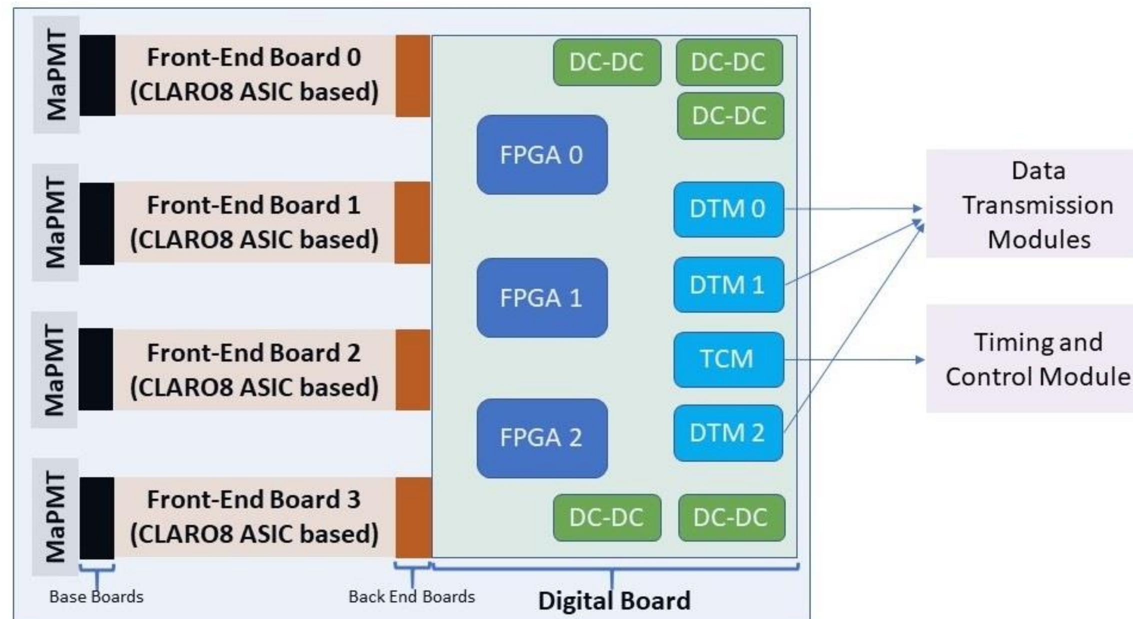
- Introduction
- Experimental Setup
- Preliminary Results
- Conclusions and Future Developments

Introduction



LHCb detector
https://lhcb-public.web.cern.ch/lhcb-public/

- **During the second LHC long shutdown (2019-2020) the entire LHCb detector will be upgraded to operate at higher luminosity;**
- **The LHCb RICH sub-detectors upgraded with a 40 times increased readout rate;**
- **For the Digital Boards an SRAM based FPGA from Kintex-7 family has been proposed: *XC7K70T-FBG676*; (800 pieces)**

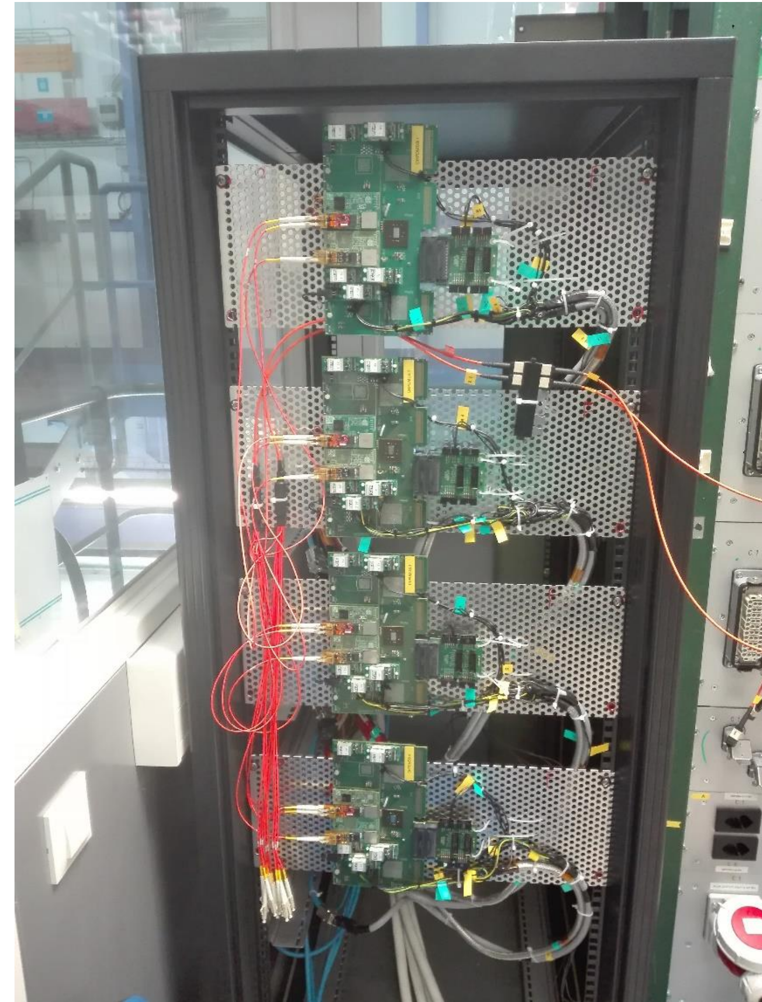


Elementary Cell (typical architecture simplified)
8 x 64 readout channels (each digital board can read 8 MaPMTs signals)

The LHCb Collaboration, *LHCb Particle Identification Upgrade Technical Design Report*, available at: link.

Introduction

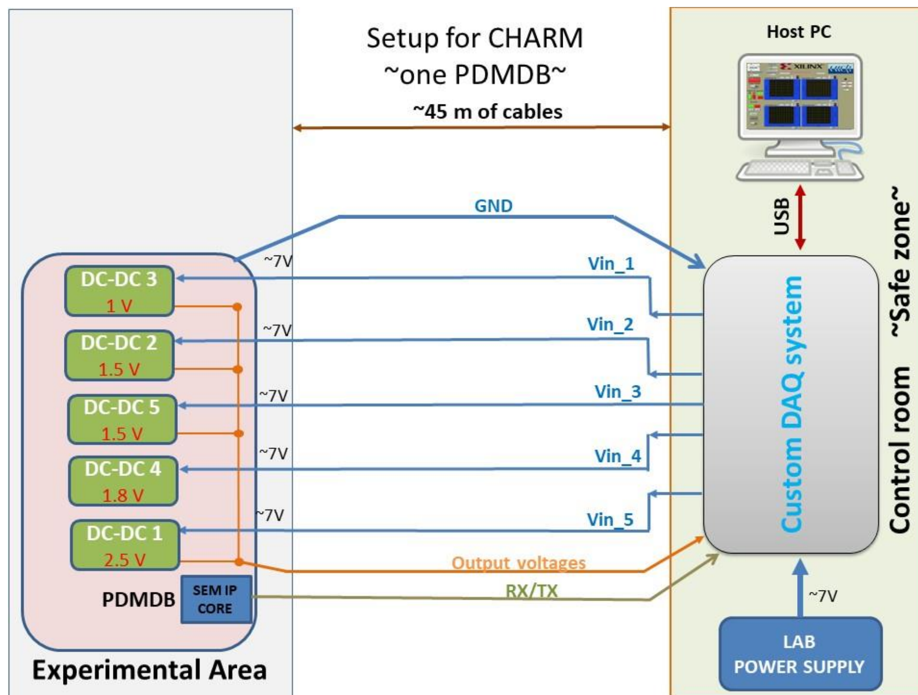
- **A successful irradiation run was done last month at CERN, using the mixed field radiation facility, CHARM;**
- **The radiation field is generated by the interaction of a 24 GeV proton beam with a Copper target;**
- **We used the position 10 of the facility, further away from PS beam;**
  - **Softer spectra compared to LHCb-RICH;**
- **The radiation was performed in 2 runs, each of them of about 1 week;**
- **4 boards, PDMDB type, with one FPGA KINTEX-7 each were irradiated.**



http://charm.web.cern.ch/

Experimental Setup

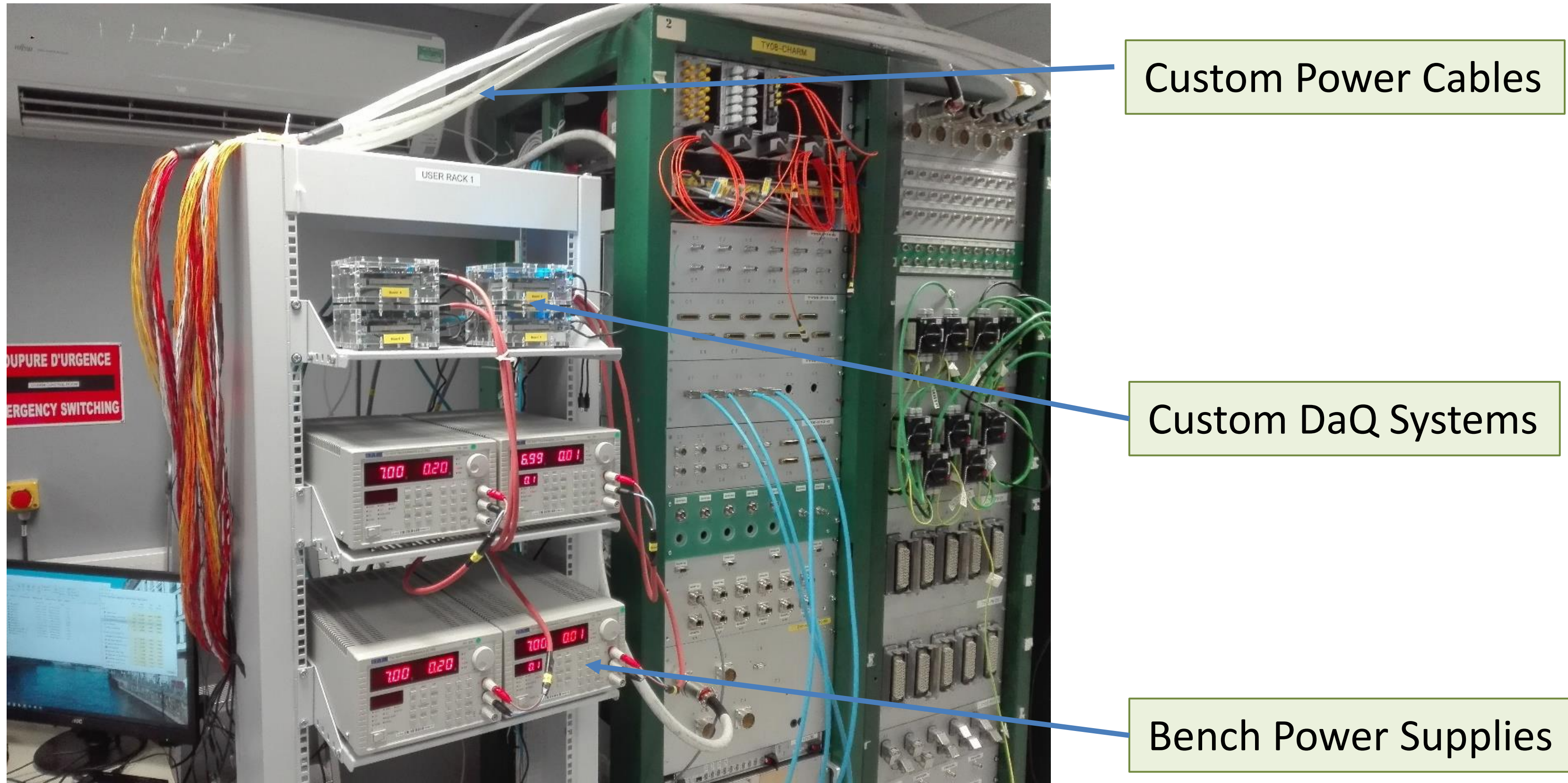
~power and electrical monitoring~



- Was implemented for each board;
- 2 of them had an UART interface used for SEM IP Core readout as CRAM mitigation;
- The power was monitored on VCCINT, VCCAUX, VCCIO and the main board supply rail;
- Boards were powered at 7 V, as will be in the Upgraded detector;
- Fail-safe functions were implemented: power cycle, reconfigurations request, alarms etc. ;
- Data was sampled at each 100-200 ms and saved in ASCII files;
- LabVIEW based GUIs.

Experimental Setup

~power and electrical monitoring~



Experimental Setup

~data read-out~

- **Each board was configured using GBT-SCA through JTAG interface controlled by the MiniDaQ system via optical fibers;**

- **The MiniDaQ and the electrical monitoring systems were connected together using a DIM server (Distributed Information Management System)**
  - **for data exchange, power cycle request, reconfiguration request etc.;**

- **Logic and CRAM SEU were monitored;**

- **The FPGA firmware architecture was simple, with small logic usage but similar with the one proposed to be used in the future (most logic, ~90-95% , was a check routine, not to be used in RICH, and not counted in logic failures):**
  - **no inputs were used, a known pattern was implemented in firmware.**
  - **2 versions were used one with SEM IP Core, one without.**

Firmware type	Total CRAM bits	Essential bits used	SEM IP core essential bits
with SEM IP	18884576	346335 (1.8 %)	154474 (0.82%)
without SEM IP	18884576	~191861 (1 %)	

Experimental Setup

~Sem IP Core~

- **Soft Error Mitigation IP Core is a special IP provided free by Xilinx and used to perform SEU detection, correction and classification for the configuration memory, CRAM;**

- **The error correction is an optional feature which can be done using one of the following method:**
  - **Correction by Repair method: ECC algorithm: supports correction of configuration memory frames with single-bit errors; (one bit in each frame)**
  - **Correction by Enhanced Repair method: ECC and CRC algorithms: supports single-bit or double-bit adjacent errors;**
  - **Correction by Replace method: supports correction of configuration memory frames with arbitrary errors. (external memory needed, hence this method was not used for obvious reasons)**

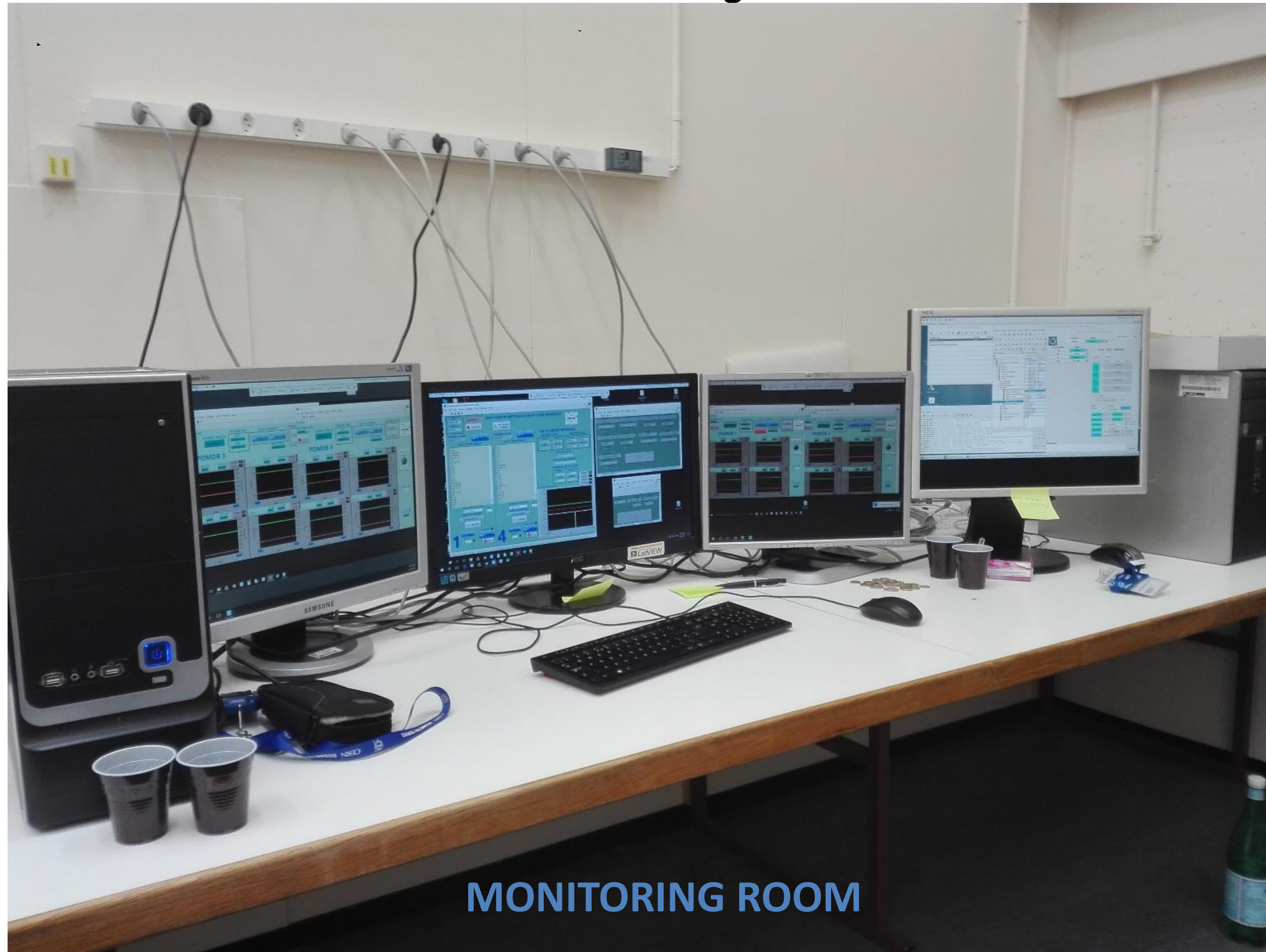
- **Using the classification capability the user can determine if corrected errors have affected configuration memory in locations essential to the user design;**

- **Supports error injection: with this feature the user can inject SEU in the configuration memory which is useful for establish the critical bits ratio of he user design.**

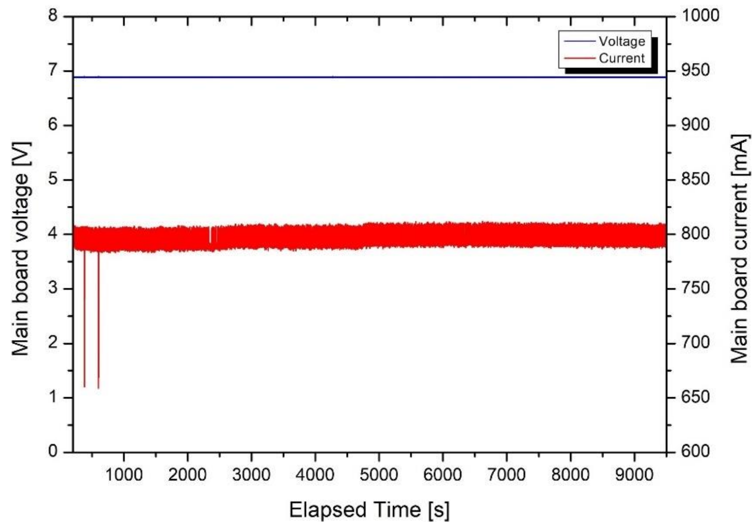
https://www.xilinx.com/products/intellectual-property/sem.html

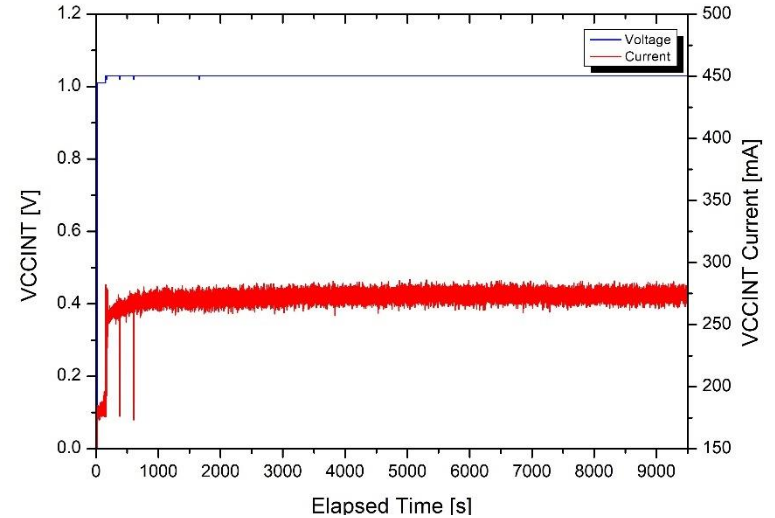
Experimental Setup

~monitoring~

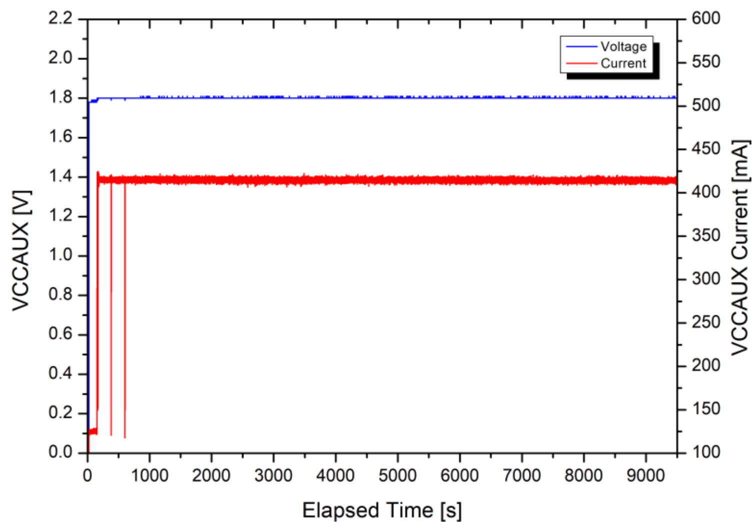


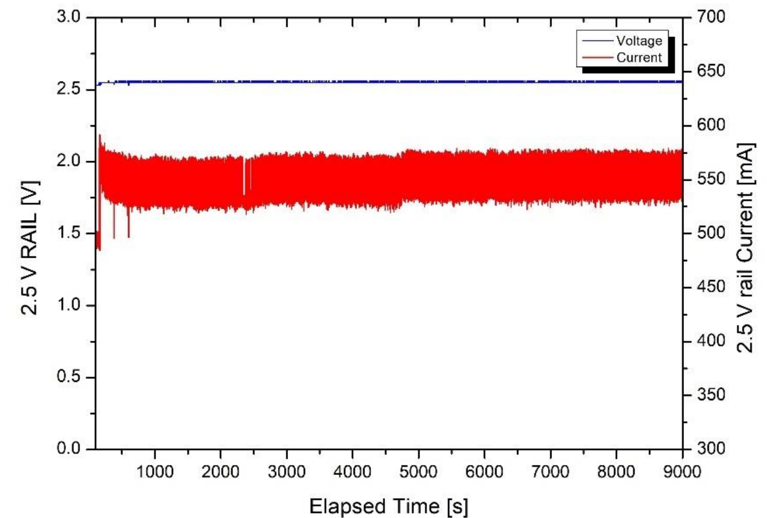
Preliminary Results



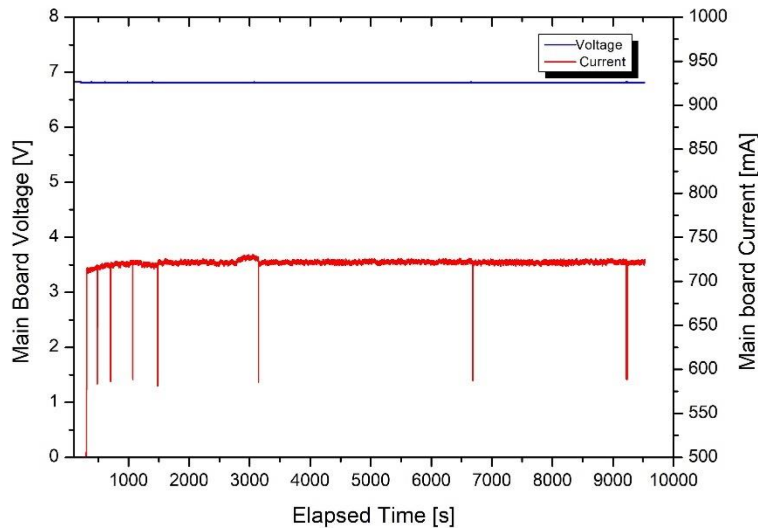


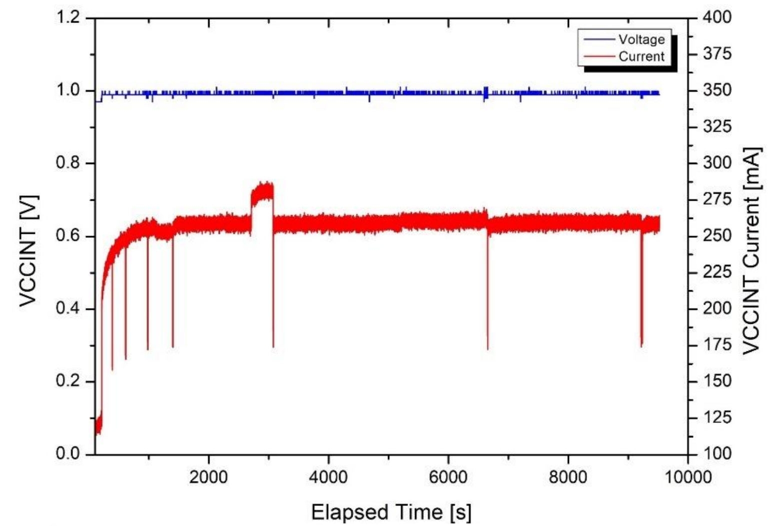
Second PDMDB @ RUN 22 (without CRAM mitigation)



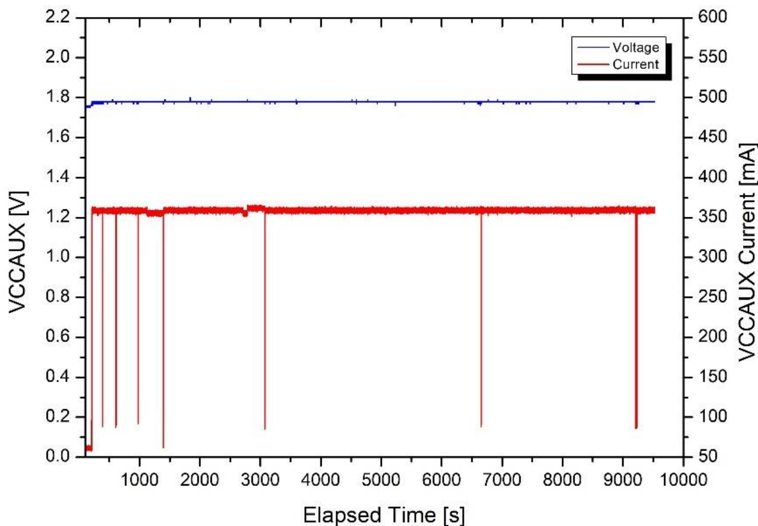


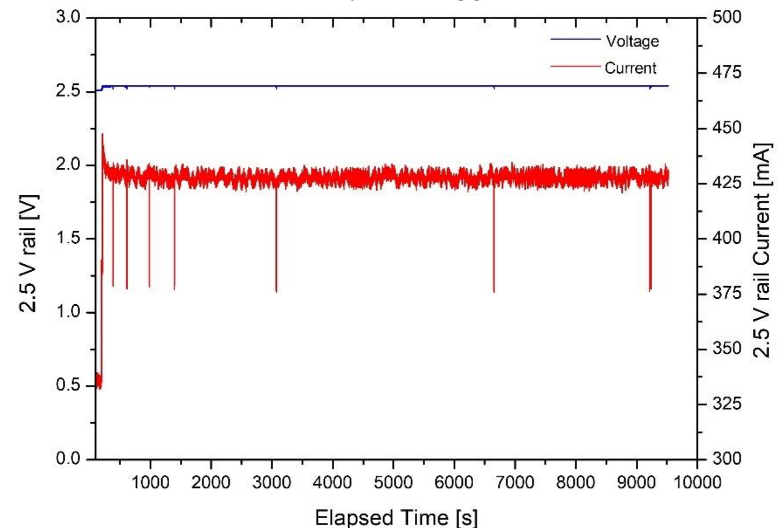
Preliminary Results



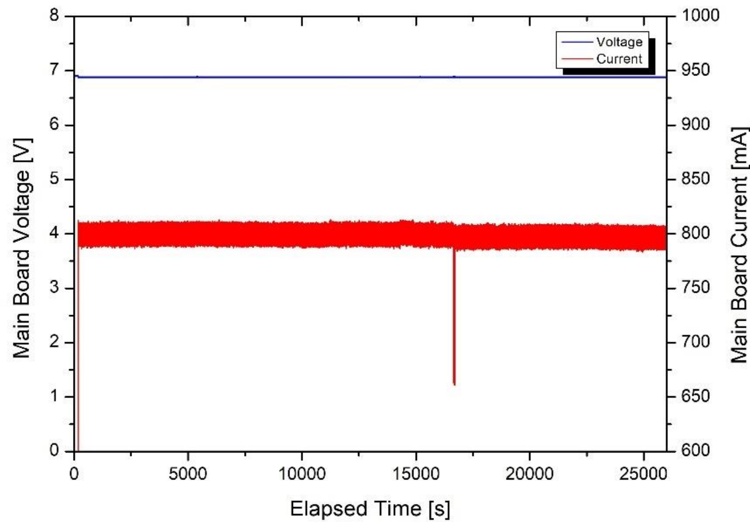


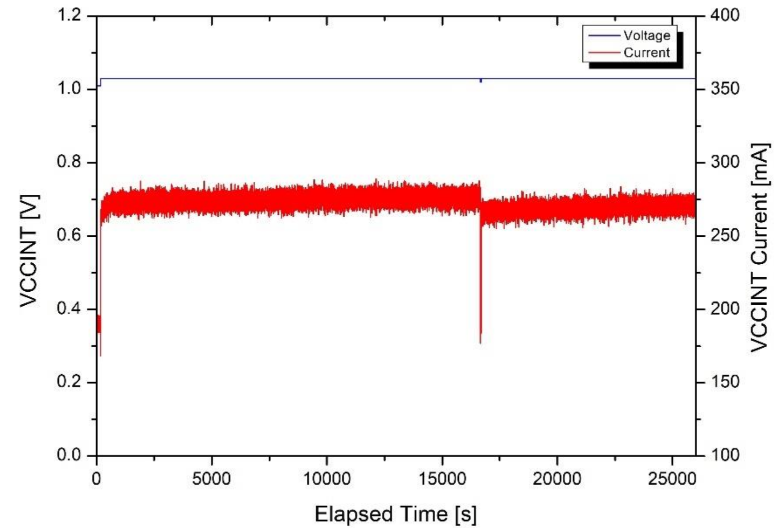
Forth PDMDB @ RUN 22 (with CRAM mitigation)



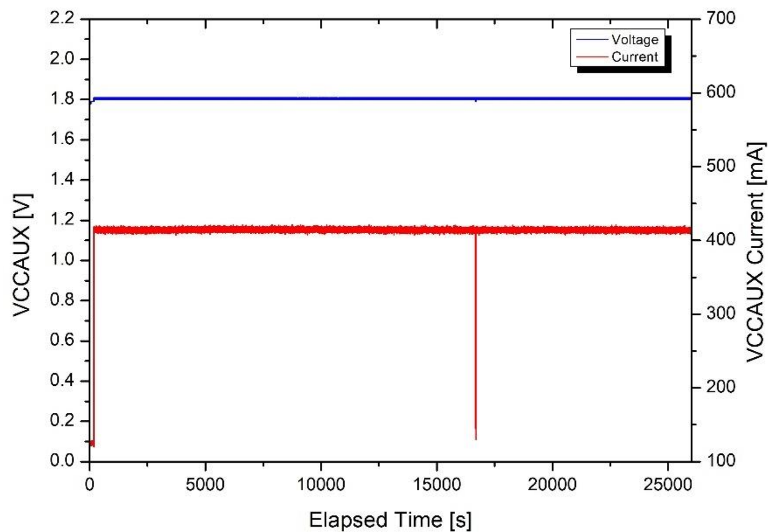


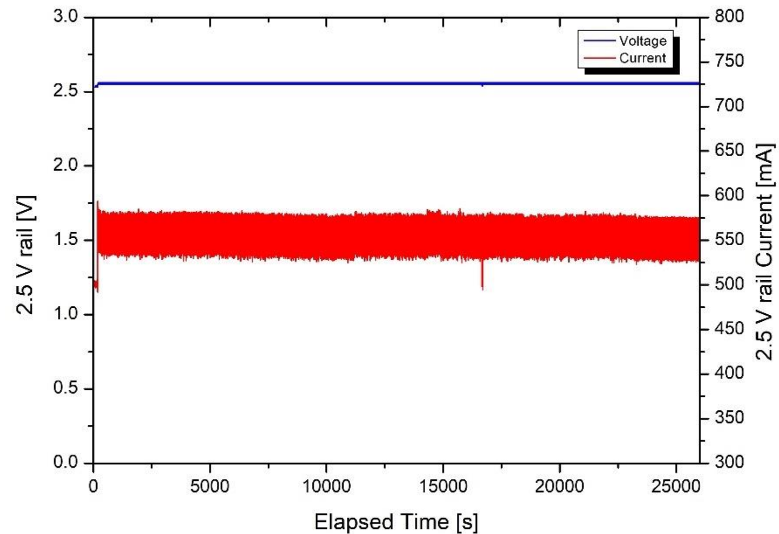
Preliminary Results





Second PDMDB @ RUN 17 (without CRAM mitigation)

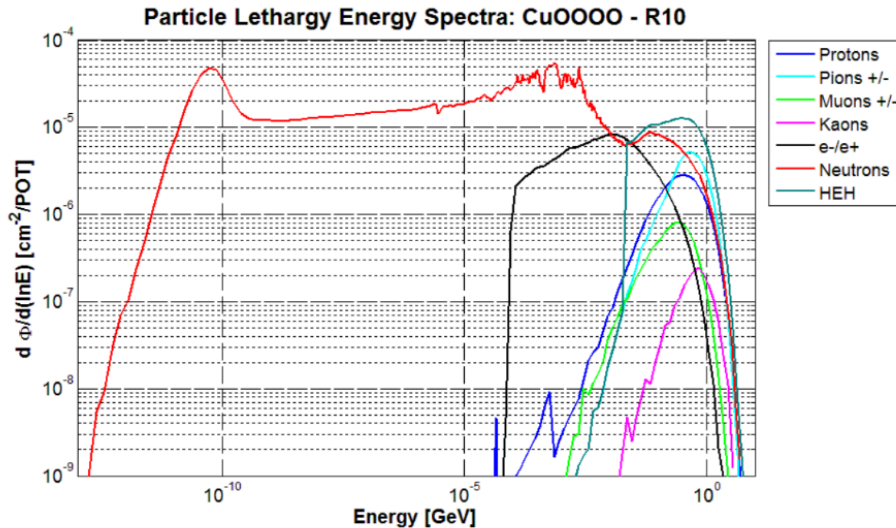




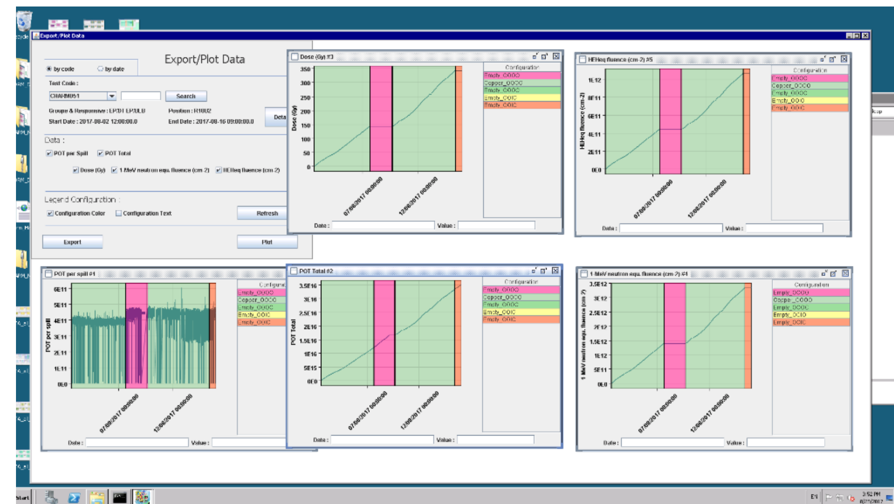
Preliminary Results

~CHARM user dosimetry~

- **34.27 krad TID, 35 % error;**
- **Total HEH fluency 10.68*10^{11} with close to 70 % neutrons (> 20 MeV);**
- **CHARM environment similar to LHC tunnel, TID and HEH fluency order of magnitude close to expectation values for RICH-LHCb Upgrade phase at 50 fb^{-1};**



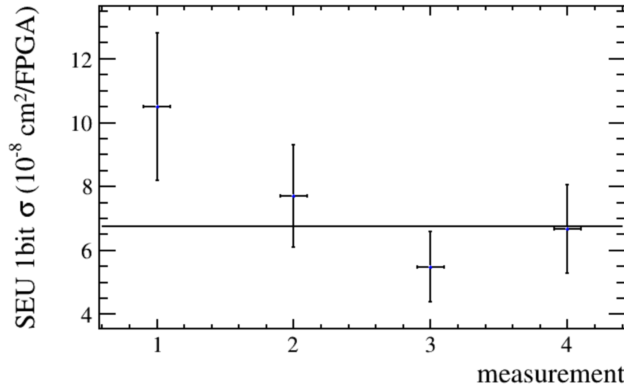
HEH spectra in position 10



TID and HEHeq

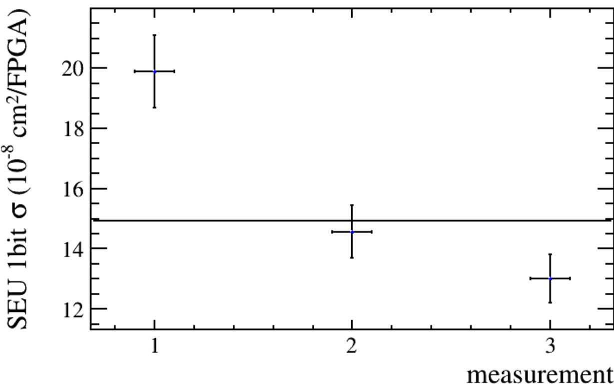
Preliminary Results

~SEU cross-section for PSI/Juelich/CHARM~

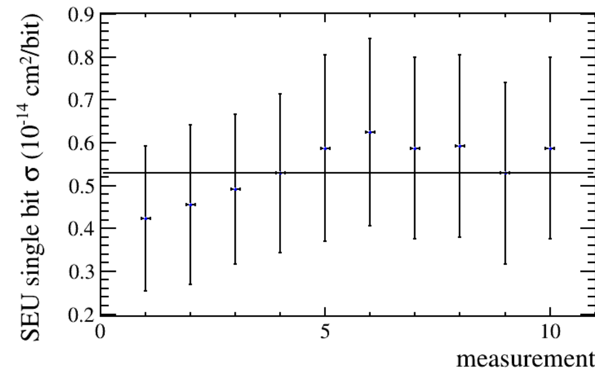


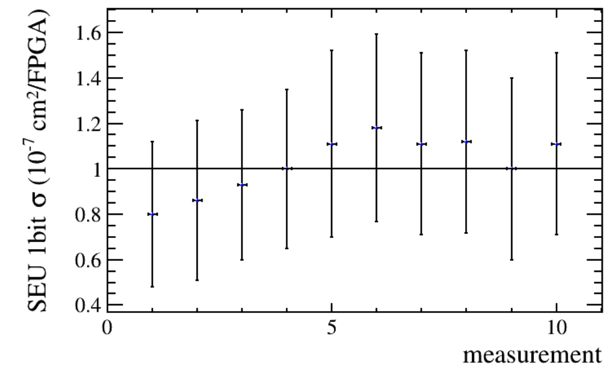
SEU cross-section PSI

- Measurement of CRAM SEU rates through SEM IP CORE:
  - PSI: 200 MeV protons, 500 krad per DUT, 3 DUTs;
  - Juelich: 35 MeV protons, 200 krad per DUT, 3 DUTs;
  - CHARM: Mixed field, close to 100 MeV average, 34 krad, 4 DUTs;



SEU cross-section Juelich





SEU cross-section CHARM

Note: This DUT has 18884576 bits of CRAM memory.

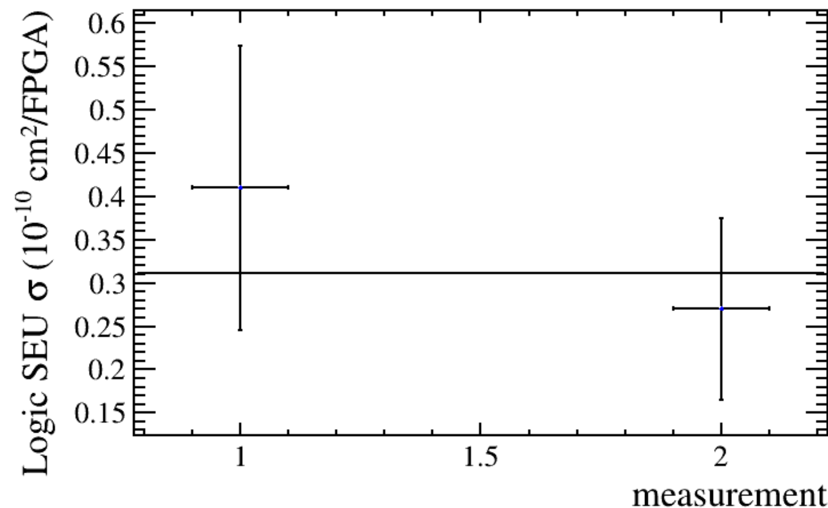
Preliminary Results

~SEU Logic errors~

- **Logic Errors are SEUs which corrupt partially or totally the User Logic on device;**
- **Firmware used in CHARM close to the RICH-LHCb Upgrade firmware for Digital Boards;**
  - **Very low number of critical CRAM bits: 6000 bits out of 18884576 bits;**
- **29 logic SEUs were seen for 14.4 krad TID, with 80% DUT operational time out of all beam time, 2 DUTs;**
- **38 logic SEUs were seen for 19.9 krad with 80% DUT operational time, 3 DUTs;**

- **σ_1= 0.41 $*10^{-10}$ cm^2 (40 % error, dominated by fluency uncertainty);**
- **σ_2= 0.27 $*10^{-10}$ cm^2 (39 % error, dominated by fluency uncertainty).**

Logic SEU cross-section



Preliminary Results

~Extrapolation~

- CHARM rates for few DUTs need to be extrapolated to 800 FPGA for RICH1 and RICH2 detectors;
- 50 fb^{-1} integrated luminosity and 10^{12} HEH fluency and 200 krad over the LHCb Upgrade phase;
- Assuming for LHCb Upgrade phase a TID/hour of 200 krad/7000 and HEH fluency/hour of 10^{12} /7000:
  - 4-5 logic SEUs in 800 FPGA during one hour;
  - About 12000 single bit SEUs in 800 FPGAs during one hour of planned LHC luminosity;
- Further uncertainty:
  - Upper values should be scaled with a safety factor of 2 to account for a harder pion spectrum in RICH versus CHARM's position 10 measurement;
  - An extra safety factor of 2-4 should be also included for uncertainty in number of critical bits of the final firmware;
  - Potential SEL events are to be discussed separately;
  - SEU in I/O banks.

Conclusions and Future Developments

- Measurements done at CHARM on Kintex-7 FPGA have outlined a large SEU rate;
  - Cross-section of $10^{-7}\mathrm{cm}^2$;
- The extrapolation to 800 FPGA for LHCb during Upgrade phase - HEH 10^{12}:
  - Have lead to large SEU numbers and few tens of SEUs in user logic per hour;
  - it is clear that operating the 800 FPGAs for TID of 200 krad and close to LHCb primary interaction point will present challenges due to hard spectra and large incident angles;
- Though not seen in CHARM measurements, SEL are probable, even in large numbers:
  - CHARM spectrum of 100 MeV average energy with neutron “flavour” (70%) omits the hard events expected for RICH Upgrade (several GeV pions);
  - Large HEH rates above GeV and large angles make probable the SEL events seen already in ion beams for 15 MeV*cm^2/mg (micro-SEL) and 32-35 MeV*cm^2/mg thresholds.