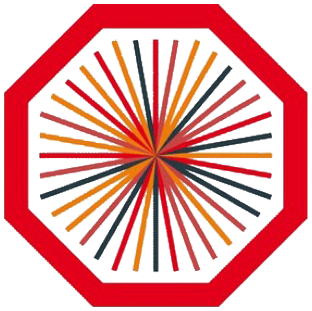
ALICE



Methodology, experimental testing and results for evaluation of the Kintex-7 operation in radiation environment

Krzysztof Marek Sielewicz[1,2], Matthias Bonora[1,3]

On behalf of the ALICE Collaboration and the ALICE Inner Tracking System Upgrade Project

[1]The European Organization for Nuclear Research (CERN), Geneva, Switzerland
[2]Warsaw University of Technology, the Institute of Electronic Systems, Warsaw, Poland
[2]University of Salzburg, Salzburg, Austria

TWEPP-2017 FPGA working group meeting, 13 September 2017

Motivation for the study

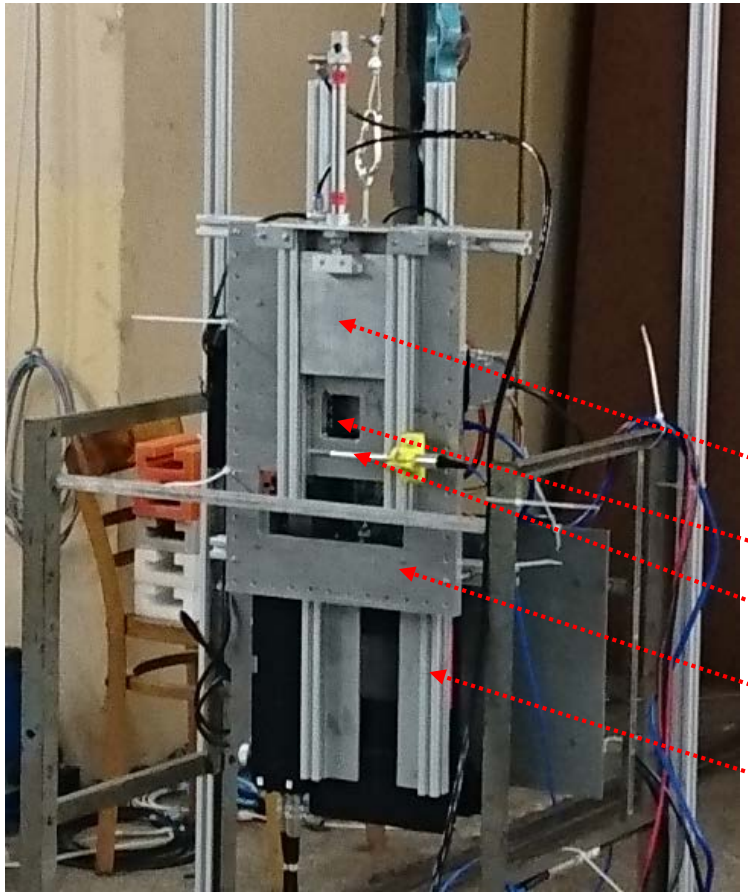
Motivation for this study was to quantitatively compare different TMR topologies, evaluate CRAM scrubbing effectiveness, and investigate performance of the built-in memory ECC protection mechanism.

For more information please check our IEEE REDW-2017 paper!

K. M. Sielewicz, G. Aglieri Rinella, M. Bonora, P. Giubilato, M. Lupi, M. J. Rossewij, J. Schambach, T. Vanat, „Experimental methods and results for the evaluation of triple modular redundancy SEU mitigation techniques with the Xilinx Kintex-7 FPGA", IEEE REDW-2017

Radiation testing facility and beam test setup

The irradiation experiments were conducted at the isochronous cyclotron [1] at the Nuclear Physics Institute of the Academy of Sciences of the Czech Republic in Rez, near Prague.



Beam test setup

The shown setup was used for testing:

- CRAM and BRAM cross-sections
- Combinatorial and sequential circuits
- Embedded ECC protection mechanism of built-in memory
- Operation of different CRAM scrubbers

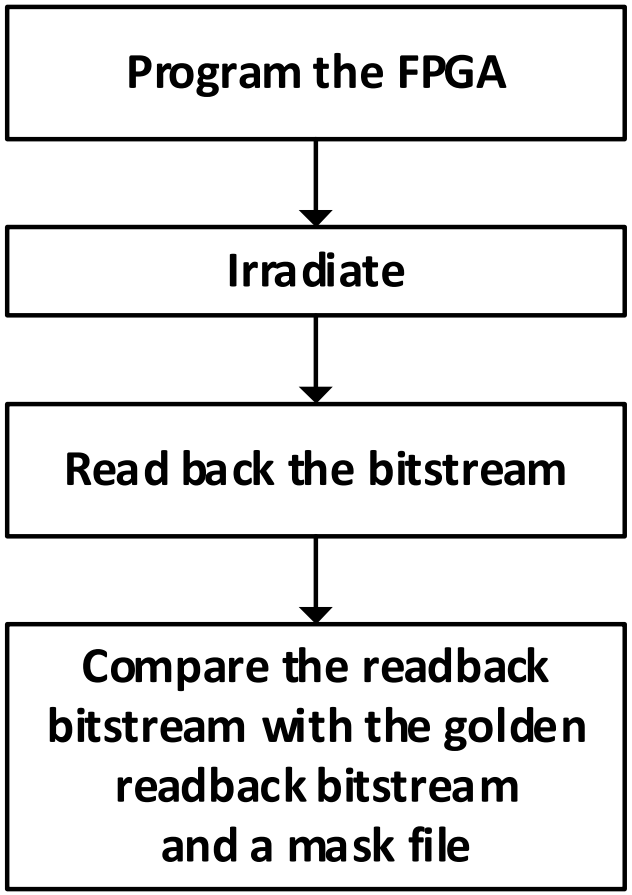
Xilinx Kintex-7 325T cross-section measurements

- CRAM and BRAM cross-sections were measured using 30 MeV[1] proton beam at LET of $\mathbf{1.148 \cdot 10^{-2}}\ \boldsymbol{MeVcm^2mg^{-1}}$

- Xilinx Kintex-7 325T
  - BRAM bits 16,404,480
  - CRAM bits 75,144,896

- $\boldsymbol{\sigma_{CRAM} = (4.52 \pm 0.03) \cdot 10^{-15} cm^2 bit^{-1}}$
- $\boldsymbol{\sigma_{BRAM} = (5.07 \pm 0.08) \cdot 10^{-15} cm^2 bit^{-1}}$

The systematic error for the calculated cross-sections is 10%, due to the uncertainty in the flux measurement.

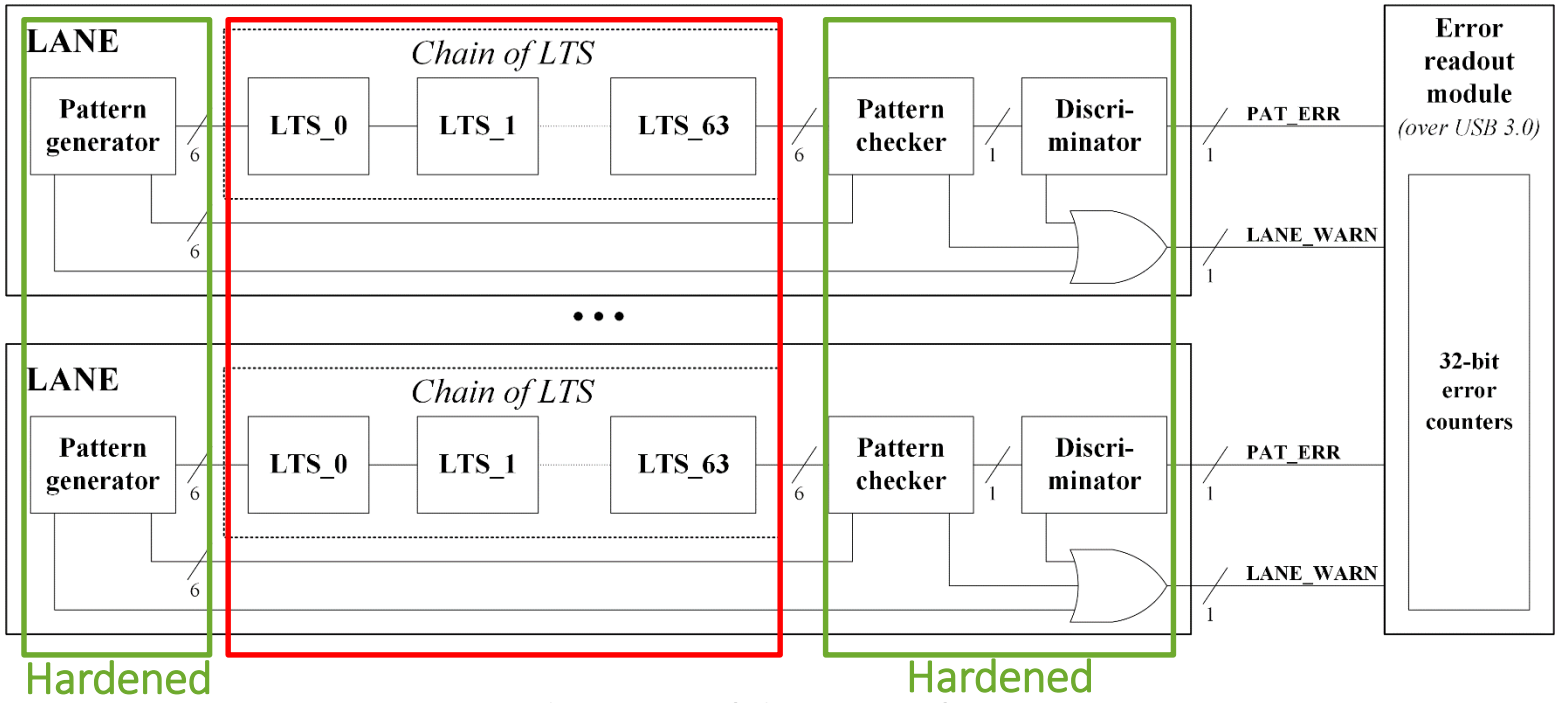


Algorithm of measuring the number of SEUs in CRAM

[1]at the surface of the FPGA

Testing design architecture

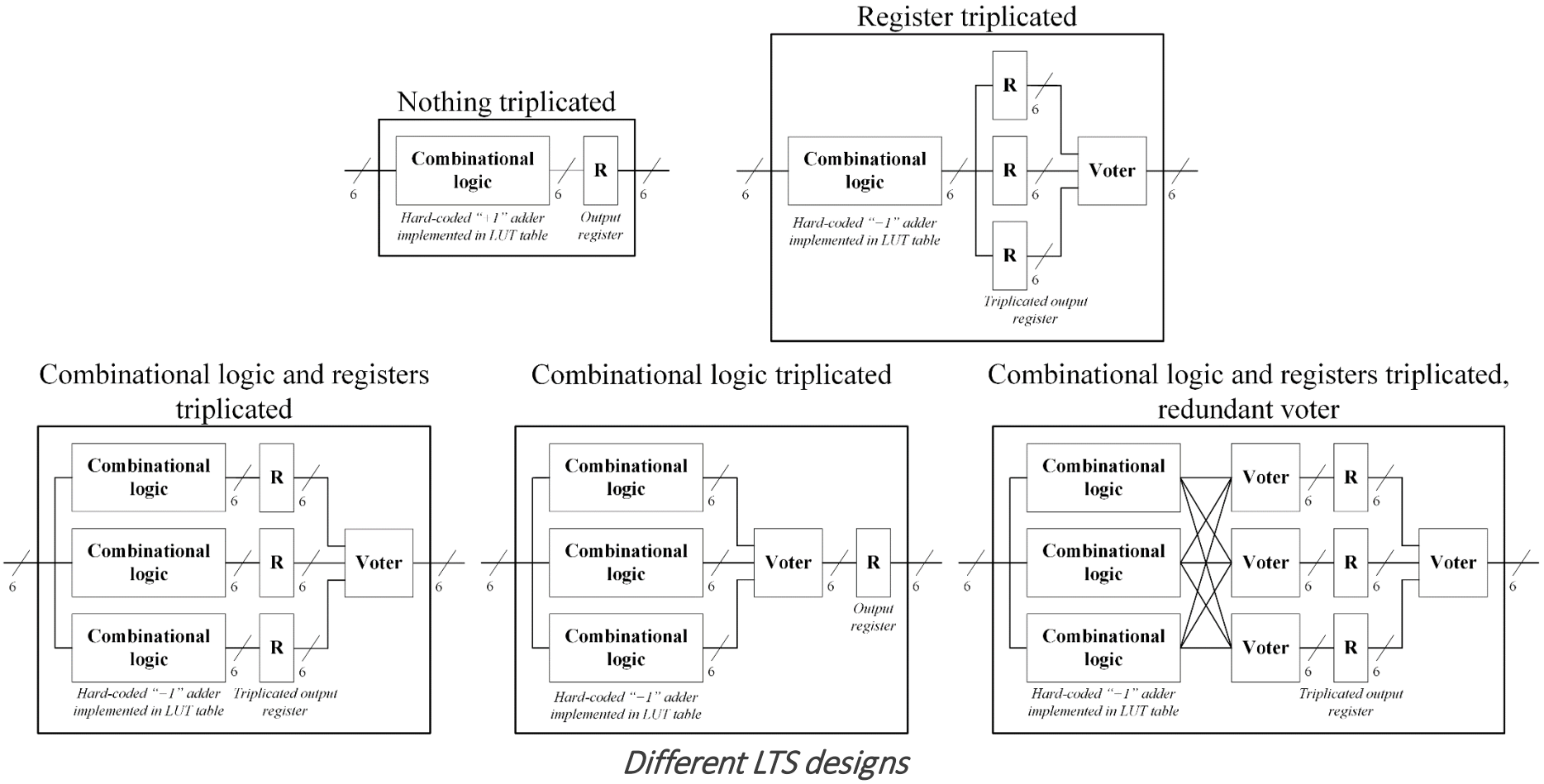
- FPGA is filled with identical modules called lanes
- Logic Test Structures (LTS) in the lanes can be implemented with different TMR topologies
- Test vectors generated by the pattern generator are continuously verified at the end of the lane by the pattern checker
- Error counters are periodically read out over USB interface
- Data are processed offline



Architecture of the testing firmware

Testing design architecture

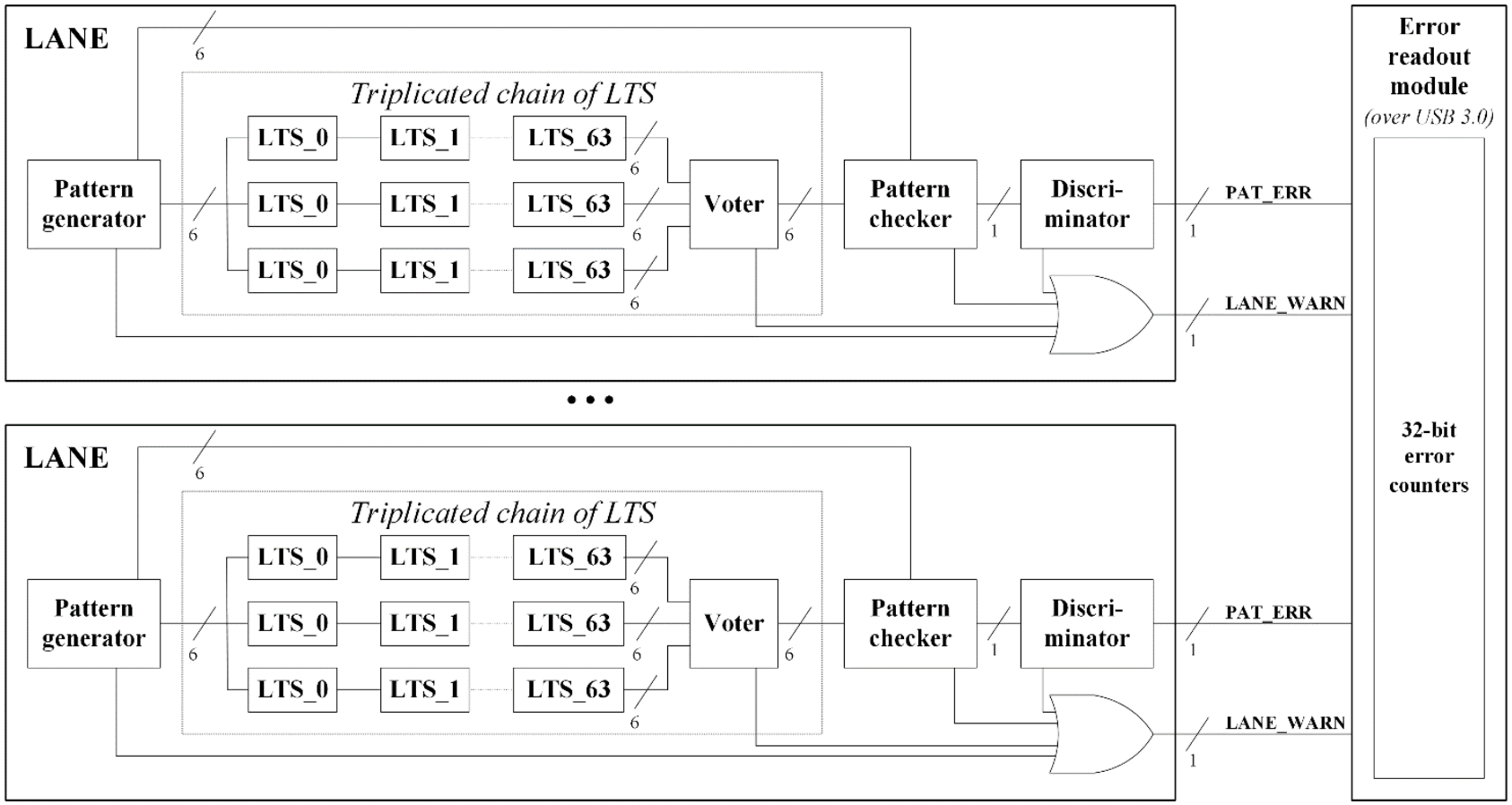
- Each lane contains a chain of 64 identical LTS
- The LTS is a “+1” adder implemented in a look-up table (LUT)
- 6 different LTS designs were tested and characterized



Different LTS designs

Testing design architecture

- Also a design with the whole chain of LTS triplicated was implemented



Comparison of the lane cross-sections without CRAM scrubber employed

Fault injection	Errors	Lanes	Faulty lanes		Lane σ	Error $\delta\sigma$
			Mean	SD	(cm^2 $lane^{-1}$)	(cm^2 $lane^{-1}$)
Nothing triplicated	408	256	23.72	6.07	$7.99 \cdot 10^{-11}$	$1.03 \cdot 10^{-12}$
Register triplicated	408	160	19.83	4.84	$10.70 \cdot 10^{-11}$	$1.29 \cdot 10^{-12}$
Combinational logic triplicated	408	128	6.00	2.53	$4.04 \cdot 10^{-11}$	$0.89 \cdot 10^{-12}$
Combinational logic and registers triplicated	408	128	5.59	3.00	$3.76 \cdot 10^{-11}$	$0.97 \cdot 10^{-12}$
Combinational logic and registers triplicated, redundant voter	408	64	2.80	1.70	$3.78 \cdot 10^{-11}$	$1.03 \cdot 10^{-12}$
Full chain of LTS triplicated	408	128	0.97	1.04	$0.65 \cdot 10^{-11}$	$0.32 \cdot 10^{-12}$
Proton irradiation tests	**Fluence** (cm^{-2})					
Nothing triplicated	$1.2 \cdot 10^9$	256	28.1	6.85	$9.70 \cdot 10^{-11}$	$3.22 \cdot 10^{-12}$
Registers triplicated	$1.2 \cdot 10^9$	160	23.43	5.89	$12.20 \cdot 10^{-11}$	$4.85 \cdot 10^{-12}$
Combinational logic triplicated	$1.2 \cdot 10^9$	128	5.55	2.87	$3.61 \cdot 10^{-11}$	$2.62 \cdot 10^{-12}$
Combinational logic and registers triplicated	$1.2 \cdot 10^9$	128	4.64	2.13	$3.11 \cdot 10^{-11}$	$1.85 \cdot 10^{-12}$
Combinational logic and registers triplicated, redundant voter	$1.2 \cdot 10^9$	64	2.32	1.71	$3.08 \cdot 10^{-11}$	$3.25 \cdot 10^{-12}$
Full chain of LTS triplicated	$1.2 \cdot 10^9$	128	0.95	0.86	$0.62 \cdot 10^{-11}$	$0.65 \cdot 10^{-12}$

12x improvement

15x improvement

$T = 120s$
$F = 10^7 cm^{-2} s^{-1}$

Comparison of the lane cross-sections with CRAM scrubber employed

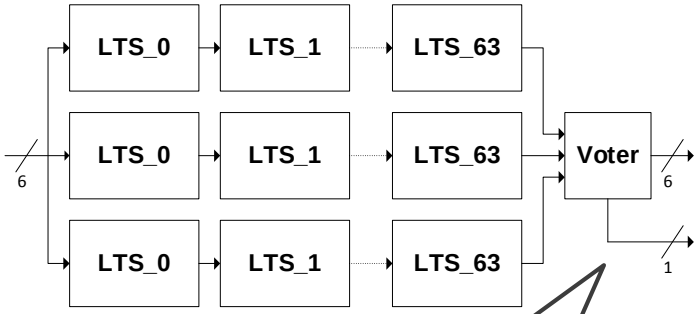
Fault injection (SEM IP scrubber)	Errors	Lanes	Faulty lanes Mean	Faulty lanes SD	Lane σ (cm^2 $lane^{-1}$)	Error $\delta\sigma$ (cm^2 $lane^{-1}$)
Nothing triplicated	408	256	22.58	5.19	$7.60 \cdot 10^{-11}$	$1.26 \cdot 10^{-12}$
Register triplicated	408	160	19.88	5.39	$10.70 \cdot 10^{-11}$	$1.81 \cdot 10^{-12}$
Combinational logic triplicated	408	128	5.98	2.49	$4.03 \cdot 10^{-11}$	$1.19 \cdot 10^{-12}$
Combinational logic and registers triplicated	408	128	5.39	2.5	$3.63 \cdot 10^{-11}$	$1.09 \cdot 10^{-12}$
Combinational logic and registers triplicated, redundant voter	408	64	2.87	1.65	$3.86 \cdot 10^{-11}$	$0.56 \cdot 10^{-12}$
Full chain of LTS triplicated	408	128	0.41	0.78	$0.28 \cdot 10^{-11}$	$0.30 \cdot 10^{-12}$
Proton irradiation tests (JCM scrubber)	**Fluence** (cm^{-2})					
Nothing triplicated	$0.48 \cdot 10^9$	256	13.50	3.15	$10.60 \cdot 10^{-11}$	$6.04 \cdot 10^{-12}$
Registers triplicated	$0.48 \cdot 10^9$	160	9.50	3.32	$11.60 \cdot 10^{-11}$	$9.67 \cdot 10^{-12}$
Combinational logic triplicated	$0.48 \cdot 10^9$	128	1.56	1.25	$2.57 \cdot 10^{-11}$	$4.80 \cdot 10^{-12}$
Combinational logic and registers triplicated	$0.48 \cdot 10^9$	128	2.47	1.39	$4.04 \cdot 10^{-11}$	$5.19 \cdot 10^{-12}$
Combinational logic and registers triplicated, redundant voter	$0.48 \cdot 10^9$	64	1.16	1.07	$3.77 \cdot 10^{-11}$	$7.99 \cdot 10^{-12}$
Full chain of LTS triplicated	$0.48 \cdot 10^9$	128	0.06	0.24	$0.09 \cdot 10^{-11}$	$0.92 \cdot 10^{-12}$

27x improvement

insufficient statistics

$T = 480s$
$F = 10^6 cm^{-2} s^{-1}$
SEU average rate
$0.4Hz$ $(2.5s)$
Blind scrubbing rate
$0.5Hz$ $(2s)$

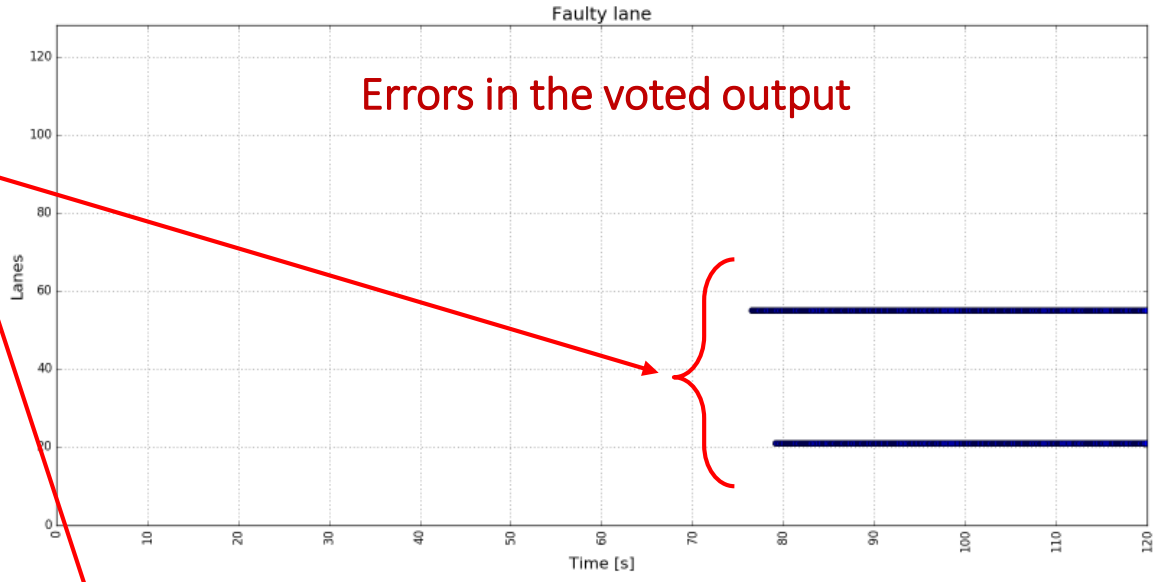
Testing design operation without scrubber

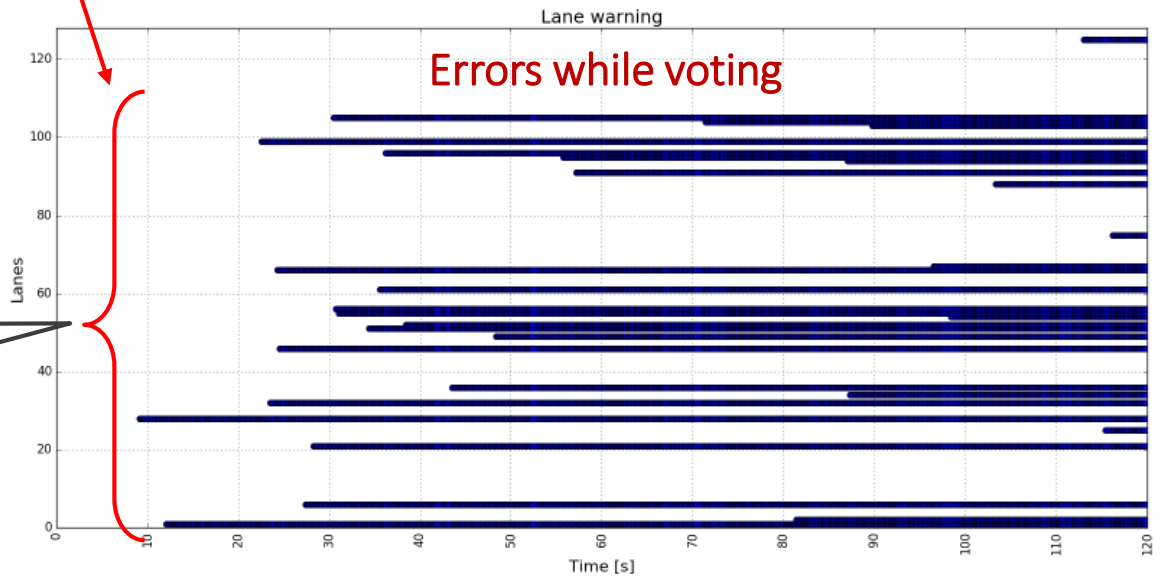


Voters report a warning (voting mismatch)

As a scrubber isn't employed single branches stay faulty

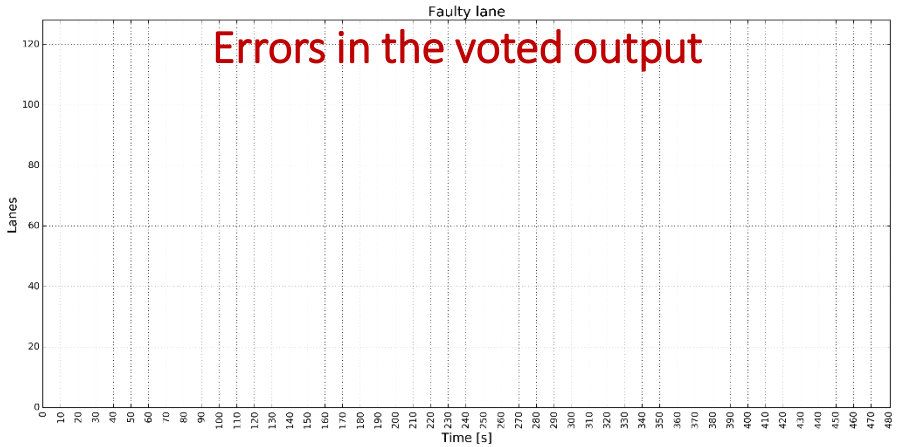
No scrubber employed,
test duration 120s, flux $10^7 cm^{-2} s^{-1}$

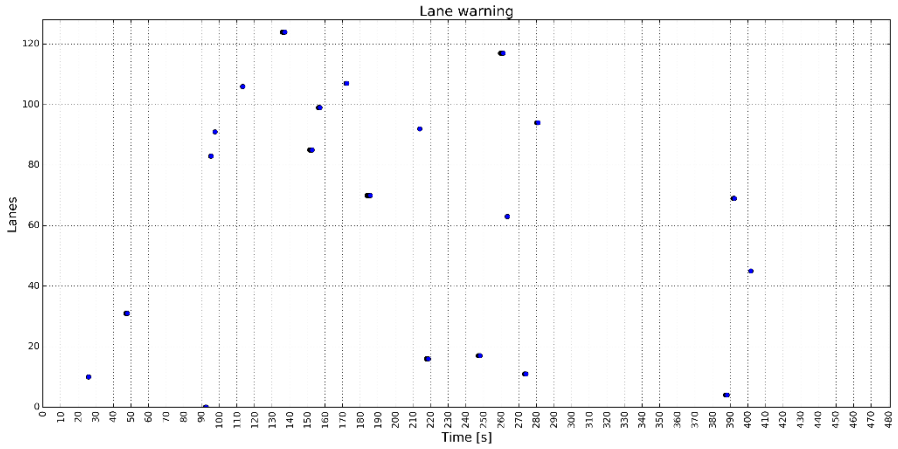




TIME [s]

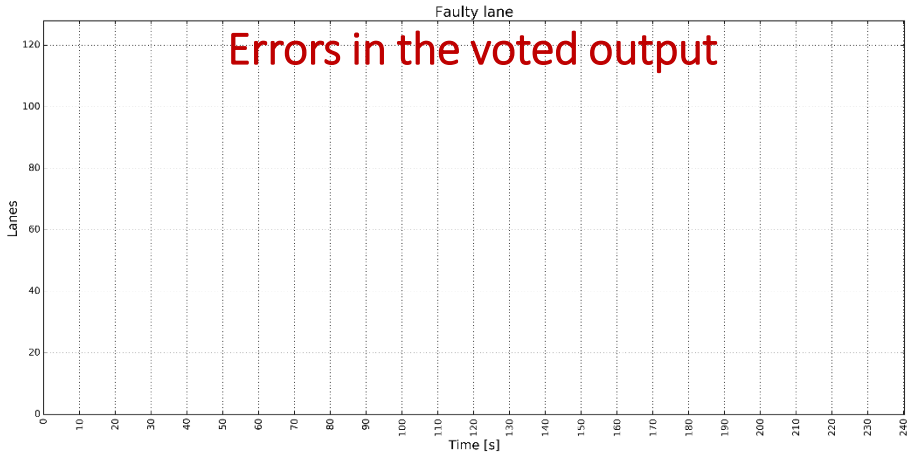
Testing design operation with the CRAM scrubber employed (JCM [2])

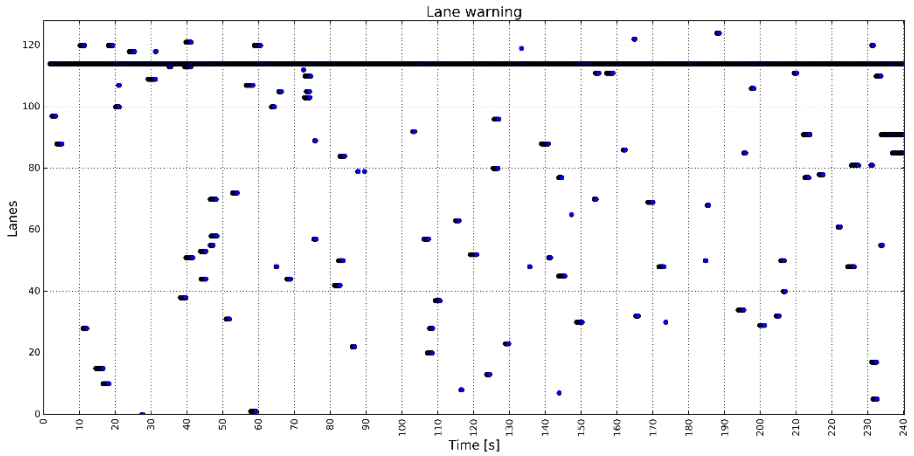




Voters report a warning (voting mismatch)

JCM scrubber, test duration 480s,
flux $10^6 cm^{-2} s^{-1}$





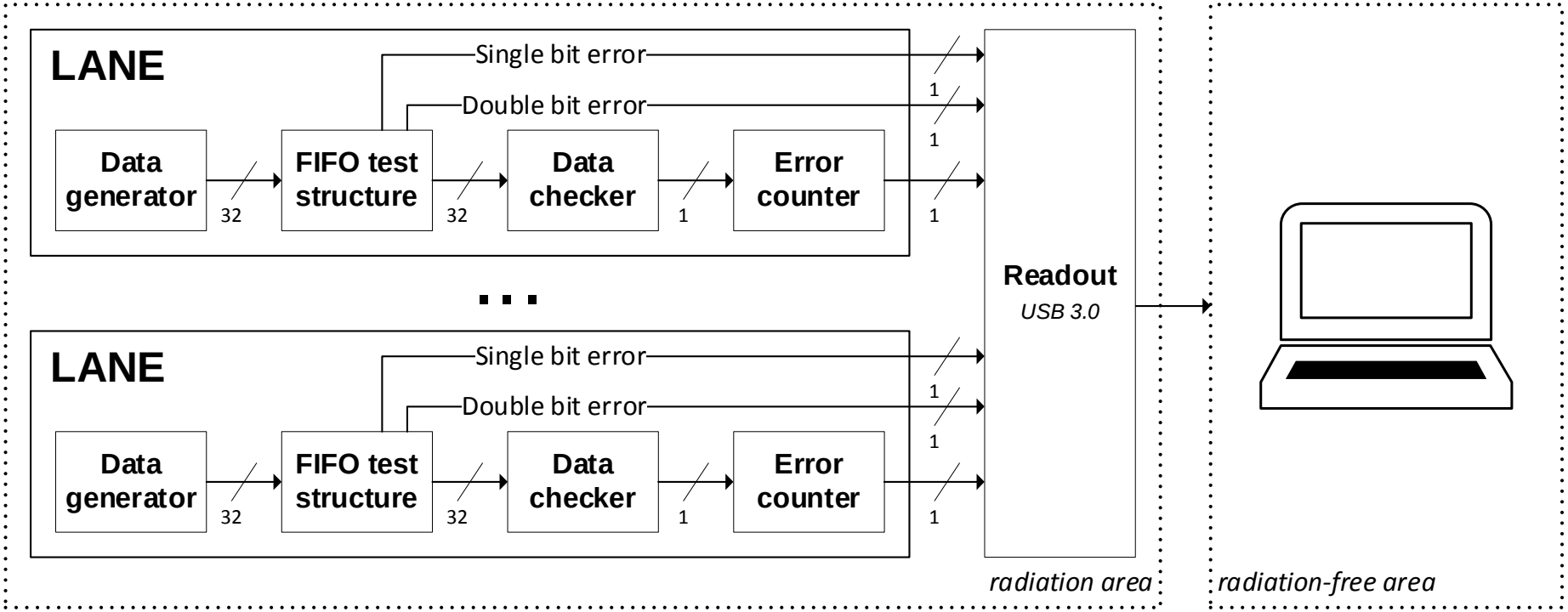
Voters report a warning (voting mismatch)

JCM scrubber, test duration 240s,
flux $10^7 cm^{-2} s^{-1}$

Scrub cycle is 2s and the flux $10^7\ cm^{-2} s^{-1}$
in the final readout system a scrub cycle will be ~1s and flux $10^3 cm^{-2} s^{-1}$

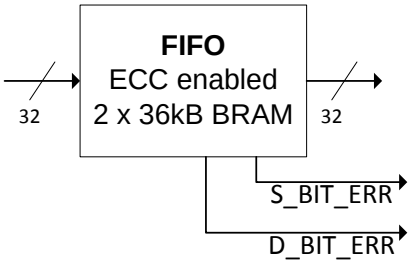
Built-in memory protection testing design

- Block memory (BRAM) has an optional built-in error correction, 8-bit error correction code (ECC) for 64 bits of data
- This functionality was tested with *beam* and FIFOs implemented in BRAM

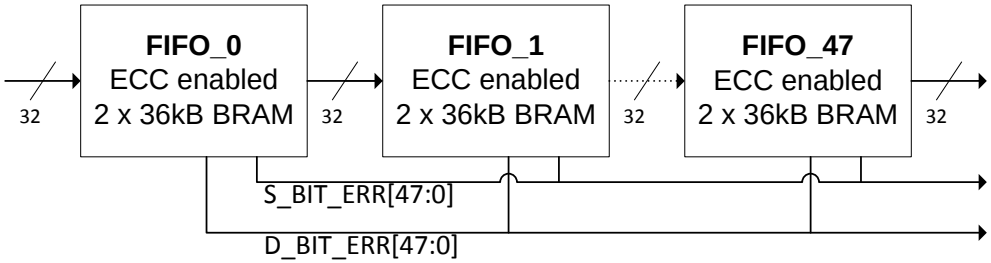


Architecture of the FIFO testing firmware
(88% of total BRAM in the Kintex-7 325T utilized)

Built-in memory protection testing design



Single FIFO (72 kB)



Chain of FIFOs (3456kB)

Observed errors:

Test conditions ($30MeV$ protons, $T = 120s$, $F = 10^7 cm^{-2}s^{-1}$, data pushed through FIFO at $100MHz$)

- Single bit errors in FIFO (successfully corrected by the built-in error correction mechanism),
- Errors in FIFO routing (SEUs induced to the input and output routing of the BRAM block utilized by the FIFO)

- Observed number of single bit errors is consistent with calculations
- No double bit errors were seen

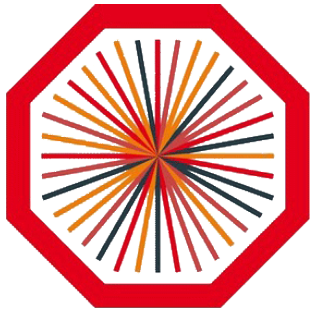
Data stored in BRAM can be expected to be safe as long as mitigation methods are utilized to harden the input/output routing

Conclusions

- Environment for fault injection was implemented
- FPGA designs for testing different TMR topologies were developed
- Conducted fault injection tests and beam tests assessing
  - Different TMR schemes
  - Built-in FIFO protection mechanism
  - Scrubbers performance

Literature

1. T. Vanat, Physical Fault Injection and Monitoring Methods for Programmable Devices. PhD thesis, Czech Technical University in Prague, 2017.
2. A. Gruwell, P. Zabriskie, and M. Wirthlin, “High-speed FPGA configuration and testing through JTAG,” in 2016 IEEE AUTOTESTCON, pp. 1–8, Sept 2016.

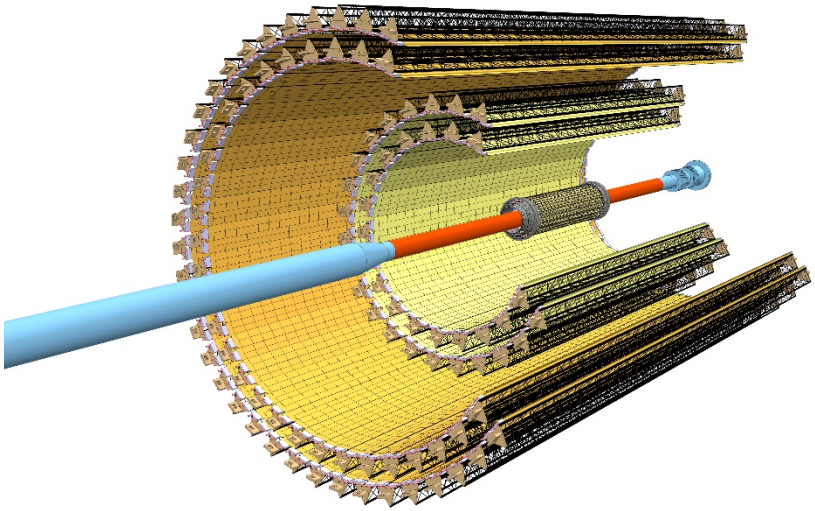


Backup slides

The upgraded ALICE Inner Tracking System

The upgraded ITS Readout System[3] key points:

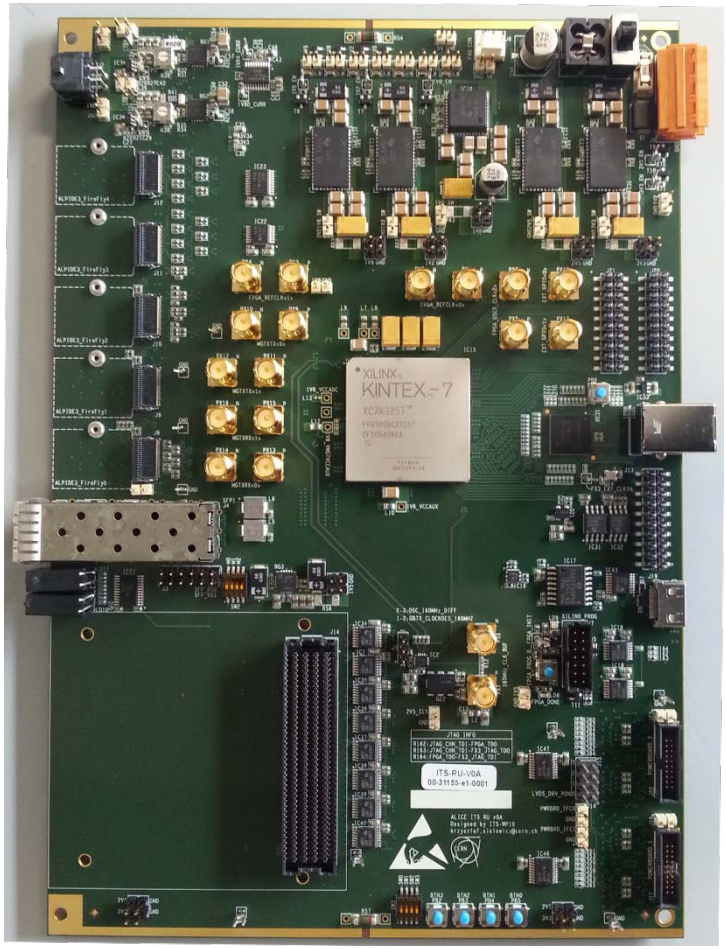
- 192 SRAM FPGAs (Xilinx Kintex Ultrascale XCKU060)
- Radiation environment parameters:
  - TID: $10\ krad$ (with a safety factor of 10)
  - high-energy hadron flux ($E_{kin} > 20MeV$): $10^3 cm^{-2} s^{-1}$
  - $1\ MeV\ n_{eq}$ fluence: $1.6 \cdot 10^{11} cm^{-2}$ (integrated over 10 years)



Upgraded ALICE Inner Tracking System

Radiation testing facility and beam test setup

- Readout Unit v0 [4] was used as a platform for all radiation tests
- A custom beam dosimetry system [5] was utilized



Readout Unit v0

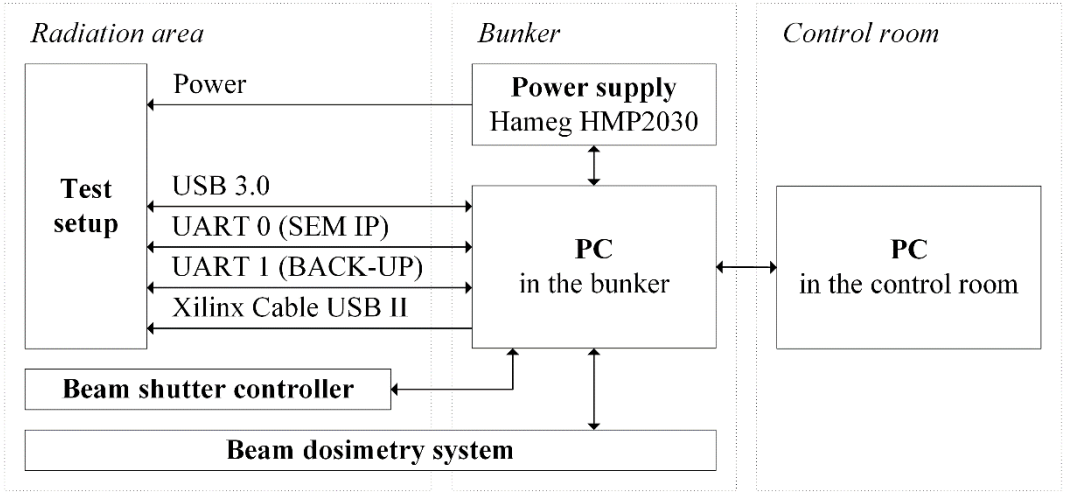
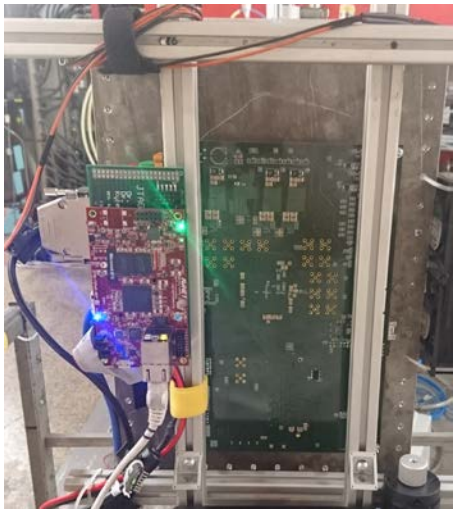


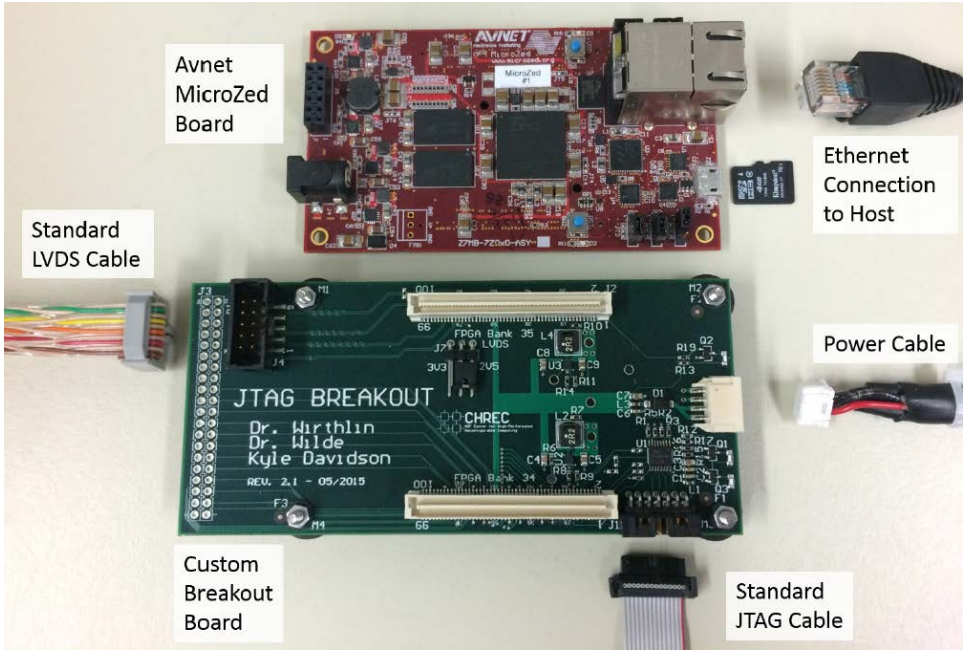
Diagram of beam test setup connections

JCM CRAM scrubber

JCM scrubber is an external device serving many different functions regarding operations on the FPGA's CRAM (e.g. blind scrubbing, readback scrubbing, error injection).



JCM scrubber installed in the beam test setup



Architecture of the JCM scrubber

Literature (extended)

1. T. Vanat, Physical Fault Injection and Monitoring Methods for Programmable Devices. PhD thesis, Czech Technical University in Prague, 2017.
2. A. Gruwell, P. Zabriskie, and M.Wirthlin, “High-speed FPGA configuration and testing through JTAG,” in 2016 IEEE AUTOTESTCON, pp. 1–8, Sept 2016.
3. ALICE Collaboration, “Technical Design Report for the Upgrade of the ALICE Inner Tracking System,” Tech. Rep. CERN-LHCC-2013-024. ALICE-TDR-017, Nov 2013.
4. K. M. Sielewicz, G. A. Rinella, M. Bonora, J. Ferencei, P. Giubilato, M. J. Rossewij, J. Schambach, and T. Vanat, “Prototype readout electronics for the upgraded ALICE Inner Tracking System,” Journal of Instrumentation, vol. 12, no. 01, p. C01008, 2017.
5. T. Vanat, J. Pospisil, F. Krizek, J. Ferencei, and H. Kubatova, “A System for Radiation Testing and Physical Fault Injection into the FPGAs and Other Electronics,” in 2015 Euromicro Conference on Digital System Design, pp. 205–210, Aug 2015.