TWEPP 2017 Topical Workshop on Electronics for Particle Physics

Report of Contributions

https://indico.cern.ch/e/twepp2017
A 2.56 GHz Radiation Hard Phase Locked Loop ASIC for High Speed Serial Communication Links

Monday, 11 September 2017 16:55 (25 minutes)

This works presents the design and experimental study of a radiation hardened Phase Locked Loop (PLL) for high speed serial-communication links. These research results are used for the LpGBT (Low Power Gigabit Transceiver) chip which will be widely used for optical data-links between the detectors and the counting rooms in the HL–LHC experiments. The PLL features a novel LC-oscillator architecture which is 600× less sensitive than traditional structures. Additionally, the circuit uses triple-modular redundancy and is designed in 65nm CMOS. The paper will present experimental results on X-ray Total Ionizing Dose (TID), heavy ion SEU and two-photon absorption laser tests.

Summary

Future upgrades to the HL-LHC at CERN will demand ever increasing data-rates from the detector modules to the counting rooms without an increase of the overall power consumption of the links. The LpGBT (Low Power Gigabit Transceiver), which is currently being developed, will make this speed available to the experiments with an uplink data-rate of 10.24 Gbps and a downlink data-rate of 2.56 Gbps which will be widely used in the different experiments around the LHC like ATLAS, ALICE, CMS and LHCh. This work presents the design of a radiation hardened Phase Locked Loop (PLL) that will be incorporated in the PLL/CDR of the LpGBT. To ensure the stability of the link, a small single-event upset (SEU) cross section is required and a Total Ionizing Dose (TID) resistance of 200 Mrad is targeted for the overall SoC.

The PLL presented in this work has a nominal output frequency of 2.56 GHz which is locked to the 40 MHz LHC reference clock through a divide-by-64 circuit. The oscillator consists of an integrated LC-tank with MOSCAP tuning diodes which are AC-coupled to the tank to improve the SEU rejection. The LC-oscillator has a tuning range from 2.2 GHz up to 3.2 GHz. The novel tuning strategy improves the SEU sensitivity by more than 600× compared to the standard LC tuning topology which makes this oscillator the best among current reported state-of-the-art oscillators in ionizing environments. The PLL measured jitter is less than 350 fs rms with a power consumption smaller than 10 mW at 1.2V. The radiation hardness is assured with the novel VCO architecture and the triplication of all digital blocks which use a custom digital library with enclosed-layout transistors cells for TID hardness. The phase-frequency detector in the PLL is triplicated with a novel asynchronous TMR structure such that no cycle slips can occur due to a single SEU error. A comparison in terms of SEU sensitivity is made with a non-triplicated phase-frequency detector. A detailed discussion on the charge injection mechanisms in this oscillator shows that a trade-off is required between the VCO cross section and the phase-noise (jitter)/power consumption of the oscillator together with the phase jump magnitudes encountered in the circuit. The VCO has a configurable power supply circuit which can be switched from voltage limited operation to current limited operation.

An experimental test chip has been fabricated in a 65 nm CMOS technology and measured with ionizing radiation. The experimental tests were done in a cyclotron that produces heavy ions from 3.3 up to 62.5 MeV cm²/mg and the findings were further investigated by scanning the circuit with two-photon absorption laser. X-ray TID tests up to 600 Mrad are discussed which show almost no

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change in the oscillation frequency since, for this topology, the frequency is essentially set by the passive LC resonant tank. Temperature effects are briefly discussed. In this paper, the design of radiation hardened PLLs for harsh environments will be discussed which is applicable to all CMOS integrated clock generation circuits.

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**Session Classification:** ASIC

**Track Classification:** ASIC
Low Jitter, Radiation Hardened by Design, 2.56 Gbps LVDS/SLVS Based Receiver for Analog Time Transmission

Tuesday, 12 September 2017 17:05 (15 minutes)

This paper proposes a novel 2.56 Gbps radiation hardened by design LVDS/SLVS like receiver for use in transmission systems requiring timing accuracy. The circuit, designed in a commercial 65 nm CMOS technology, uses a replica receiver with charge pump feedback. This feedback loop equalizes the propagation delay of the outputs rising and falling edge, independent of total ionizing dose (TID) radiation effects. The measured output signal has an RMS jitter of 3 ps at a maximum data rate of 2.56 Gbps. The circuit consumes only 1 mW of power from a 1.2 V power supply.

Summary

High precision time-domain signal processing circuits are required in many of today’s applications like particle detectors in high energy physics experiments such as the CMS and ATLAS experiments at the Large Hadron Collider (LHC) in CERN or laser-ranging sensors. These applications embed their key information in the time difference between multiple signals or events. This timing information is usually converted to the digital domain by a time to digital converter (TDC). However, in large and/or complex systems, the distance between the event generator and the TDC can become rather large necessitating long distance transmission of these signals, while preserving their timing information.

Because of their high speed, low power consumption and interference robustness, Low Voltage Differential Signaling (LVDS) and Scalable Low Voltage Signaling (SLVS) are commonly used. The SLVS standard is comparable to LVDS, but with a lower voltage swing and a 200 mV common mode voltage instead of 1.2 V. For communication applications, the regenerative nature of the receivers allows for some jitter tolerance, provided that the bit error rate remains sufficiently low. However, in the envisaged applications the LVDS link will be placed in the accurate time signal path. Hence, any jitter or distortion introduced by this link will decrease the systems resolution. So to allow the use in accurate time-domain circuits, the propagation delay of all output edges must be the same and the jitter must be minimized.

This paper focuses on the design of a Total Ionizing Dose (TID) radiation hardened by design LVDS/SLVS receiver for long distance analog timing signals transmission. The proposed receiver uses an NMOS input pair, single ended output op-amp structure. In radiation environments, the total ionizing dose (TID) will cause degeneration of the charge carrier mobility and shifts in the threshold voltage. These effects will introduce a mismatch between the propagation delay of the outputs rising and falling edge. The proposed circuit compensates this mismatch by introducing a replica receiver with charge pump feedback. An ideal clock at the input of this replica receiver generates a clock signal at the output with a duty cycle of 50 % and a common mode voltage of VDD/2. Any deviation from this 50 % duty cycle, caused by the TID effects, will alter the common mode voltage. This error signal is then used to adjust the currents through the proposed receiver, in order to equalize the propagation delay of the rising and falling output edges. At 500 Mrad, simulation results of the proposed feedback circuit show a 44 times lower shift in propagation delay error compared to an open loop receiver circuit. The proposed receiver has a measured output jitter of only 3 ps at a 2.56 Gbps data rate while consuming only 1 mW of power from a 1.2 V power supply.
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Session Classification: POSTER Session

Track Classification: ASIC
Mini-EUSO is a telescope and detector designed by the JEM-EUSO Collaboration to observe the UV emission of the Earth from the vantage point of the International Space Station (ISS) in an Earth orbit of around 400 Km. The main goal of the mission is to map the Earth in the UV, thus increasing the technological readiness level of future EUSO experiments and to lay the basis for the detection of Extreme Energy Cosmic Rays from space.

This article introduces the motivation behind the Mini-EUSO multi-level trigger idea, details the readout hardware chain and reports test results on the trigger logic.

Summary

The Mini-EUSO instrument is an experiment by the JEM-EUSO Collaboration and approved by both, the Russian (Roscosmos) and Italian (ASI) space agencies. This telescope will be launched to the Zvezda module of the ISS, where it will look down to the Earth from a nadir-facing, UV-transparent window.

Mini-EUSO aims to be a pathfinder mission for a future space-based detector aiming to detect the fluorescence and Cherenkov light produced by Extreme Energy Cosmic Rays (EECR) atmospheric showers. The scientific goal is thus an unprecedented high-resolution UV map of the Earth (5 Km and 2.5 us respectively), collecting night-time data. Such observations are crucial for the understanding of the detection threshold of EECRs from space, in addition to estimating the duty cycle of future experiments. The same detector is also able to catch a variety of both, atmospheric and terrestrial phenomena, such as transient luminous events (TLEs), meteors, space debris, bioluminescence and anthropogenic lights. The variation of these events require a six orders of magnitude dynamic range, motivating a multi-level trigger system including given constraints on the duty cycle and data storage.

From a system level view, this detector is made up of three main sub-systems: the Fresnel-based optical system, the Photo Detector Module (PDM) and the readout electronics. The optical system consists of 2 double sided Fresnel lenses with a diameter of 25 cm allowing for a compact system with a large aperture. The lenses focus the light onto the focal surface, where it is detected by an array of 36 multi-anode photomultiplier tubes (MAPMTs) with UV filters, called PDM. Each MAPMT consists of 64 pixels, resulting in a 2304 pixels readout. Signals are pre amplified and converted to digital by the SPACIROC3 ASIC, before being passed to the data processing unit for data handling and storage.

The Mini-EUSO trigger logic is implemented inside the FPGA of a custom PCB, called Zynq Board (the PDM readout core). This trigger logic consists of two levels, working with different time resolution thus to capture categories of events on short timescales (e.g. showers), but also to provide continuous imaging on slower timescales as Mini-EUSO orbits around the Earth (e.g. lightnings). In order to achieve this efficiently, 3 different types of data are stored with different time resolution while the trigger rate is kept below 1 Hertz.

Prior to the implementation of the trigger algorithm in hardware, the logic has been extensively tested using both simulated data (using the EUSO Simulation and Analysis Framework software, ESAF) and data taken at TurLab, a laboratory equipped with a rotating tank and located in a dark
environment, with a series of different light configurations to reproduce the UV emission of the Earth. After those steps, the trigger algorithm has been integrated in the Zynq Board FPGA and tested with a hardware-synthesized artificial data generator, that allows standalone testing. Further trials involved the complete readout chain, stimulated using a pulse generator.

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**Session Classification:** POSTER Session

**Track Classification:** Trigger
The ALICE experiment at the LHC plans an upgrade of its TPC, due to the expected high Pb-Pb collision-rate after the shutdown of LHC in 2018. In the upgraded TPC, Gas Electron Multiplier (GEM) chambers and continuous readout system will replace MWPC chambers and conventional triggered readout, respectively. In the continuous readout, GEM signals will be processed using 32 channels of SAMPA ASIC (preamplifier and ADC). The SAMPA second-prototype was delivered in 2016 and the production of the final version is in progress. During the presentation, test results of the SAMPA coupled with GEM detector prototype will be presented.

Summary

During Run3 the interaction rate of lead ions at the ALICE experiment at the LHC is expected to be 50 kHz. Due to these high collision rates, the Multi-Wire Proportional Chambers of the present ALICE TPC will be replaced by readout chambers featuring Gas Electron Multiplier (GEM) foils. A continuous readout system will replace the existing triggered readout.

In the upgraded TPC readout, the current signals from the GEM detector pads will be readout by Front-End Cards (FECs) via custom-made SAMPA ASICs. The SAMPA contains a charge-sensitive preamplifier, a shaper, a 10 bit 10 MHz digitizer and a digital filter, processing and data compression chain. In the FECs, the output of the SAMPA will be multiplexed and transmitted using GigaBit Transceivers (GBTx) via optical links to a Common Readout Unit (CRU). The CRU is an interface to the on-line computer farm, trigger and detector control system. The upgraded readout system will utilize 3400 FECs, each containing 5 SAMPA ASICs (32 channels each), and in total of about 500k channels. The data rate from SAMPA to CRU via GBTx will be 1 TBytes/s.

This presentation will be focused on the qualification studies of the second prototype of the SAMPA ASIC. These studies are done using waveform generator and GEM detector prototype. The tests performed using waveform generator showed an excellent pulse shape stability and gain linearity at various input charges (5 fC to 110 fC). A significant improvement is observed in the noise and cross-talk performance of the present SAMPA as compared to its older version.

The SAMPA prototype performance is also studied by coupling it to the GEM detector prototype which consists of a stack of four 10 x10 mm² GEM foils with S-LP-LP-S configuration. Here S and LP refer to standard and large pitch, respectively, while pitch defines the distance between GEM holes. The GEM foil configuration is optimized to keep ion back-flow below 1%. The survival studies of the SAMPA input-protection from the GEM discharges will also be reported. The GEM discharges are created using two different alpha sources: firstly a standard Am-241 source followed by a gaseous Rn220 alpha source. The first source produced more localized sparks while the other source irradiates the detector volume more uniformly. The results obtained from these tests meet the ALICE TPC requirement and helped to finalize the SAMPA ASIC design. This work is relevant to the workshop topic Highly Integrated Detector and Electronics.

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**Session Classification:** POSTER Session

**Track Classification:** ASIC
Characterization of a Prototype Batch of Long Polyimide Cables Designed for Fast Data Transmission on ATLAS ITk Strip Staves

Tuesday, 12 September 2017 17:45 (15 minutes)

The silicon-strip system in the ATLAS ITk detector has individual sensor modules mounted on staves to provide integrated solution for mechanical support, power, cooling, and data transmission. The data and power are transmitted to individual modules on polyimide tapes placed on thermo-mechanical stave cores. The 1.4 m long tapes transmit module data at rates up to 640 Mbps, several multi-drop clock and command links, and power lines. The first batch of 25 tapes has been produced. We characterized the line impedance and its variation across the batch, examined the tape cross-section, and assessed the variation between design and fabrication.

Summary

Modern HEP experiments feature large-scale silicon-based tracking systems that require data and power delivery to individual modules cooled to required operational temperatures. Providing these services on the per-module basis would require too much material in the tracking volume causing deterioration of tracking performance. Therefore, higher level integrated solutions are necessary. The ATLAS ITk strips adopted the “stave” as a higher level object to accommodate an array of up to 14 modules on each side of cores providing mechanical support and thermal management. Data and power are supplied on tapes co-cured with carbon fibre skins, which are then glued to a carbon fibre honeycomb to form the stave cores. The modules are mounted on top of the tapes. To achieve a good thermal performance, the tapes need to be sufficiently thin, while tracking performance requires a minimal amount of metal inside. Due to large data volume coming from individual modules, a scheme of 640 Mbps point-to-point links is adopted for module data output. Due to the stave dimensions, these links are up to 1.4 m long. The design challenge is to achieve good signal integrity given the very tight space constraints. The clock and command lines are used in multi-drop configuration to save space and material. They are required to run at 160 Mbps.

We have designed a new prototype tape which takes into account several features that were found to be important in earlier tests. A bottom shield layer is placed underneath data lines to isolate the signals from dissipative effect of the carbon fibre layer under the tape. Individual receivers present impedance perturbation for the multi-drop lines. Since each stave side can have up to 14 modules, and each module has up to 2 data controllers, the line can have up to 28 receivers, which significantly affects the signal shape. In order to minimize such variation, we have split the multi-drop line into several lines connecting up to 5 modules each. Finally, we targeted 100 Ω impedance for individual data lines through the trace geometry and dielectric thickness.

The first batch of 25 prototype tapes has been produced and we started to characterize their performance. The Time Domain Reflectometry method is used to measure the line impedance. Measurements of the impedances of the lines within one tape show excellent uniformity with an RMS of about 1 Ω. Measurements for different tapes show a slightly larger but still acceptable variation. However the measured impedances are slightly different to the calculated ones and we are trying to understand the origins of this discrepancy. We are checking the dielectric properties and examining the fabricated line geometry with cross-sectional measurements of the tapes to identify variation with design parameters. We will incorporate the fabrication artefacts into future proto-
type tape designs to achieve the desired impedance. This work is relevant to experiments using fast data transmission on long polyimide tapes.

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**Session Classification:** POSTER Session

**Track Classification:** Production, Testing and Reliability
ALICE Trigger System for LHC Run 3

The ALICE Central Trigger Processor (CTP) is going to be upgraded for LHC Run 3 with completely new hardware and a new Trigger and Timing Control (TTC) system based on a Passive Optical Network (PON) system. The new trigger system has been designed as dead time free and able to transmit trigger data at 9.6 Gbps. A new universal trigger board has been designed, where by changing the FMC card, it can function as a CTP or as a LTU. It is based on the Xilinx Kintex Ultrascale FPGA and upgraded TTC-PON.

Summary

In LHC Run 3 the interaction rates at point 2 will increase to 50 kHz for Pb-Pb, and 200 kHz for p-p and p-A. In addition, where feasible a safety margin of two is applied in the system design. The aim of the ALICE trigger system is to select essentially all of these interactions. The new ALICE CTP will be based on 3 trigger levels (LM at 650 ns, L0 at 900 ns and L1 at 6.5 µs) with regular “Heartbeat” (HB) triggers for detectors running in continuous mode. The trigger system must also cope with detectors that still have dead-time during the readout. It is based on the Xilinx Kintex Ultrascale FPGA and it has several interfaces: upgraded TTC-PON, GBT, IPbus, I2C, SPI and also the original TTC. The board is equipped with 2 DDR4 memories (each 1 GB) and it can be equipped with a maximum of 20 SFP+ modules. A complex power system on the board is controlled by a UCD90120A power sequencer and is monitored via PMbus. The main interface between the LTU and the CRU (Common Readout Unit) will be TTC-PON, but the ITS and MFT detectors will also receive triggers directly at their FEE via GBT (in parallel to CRU via TTC-PON) due to a trigger latency constraints. The interface between the CTP and the LTU is also based on TTC-PON. The LTU will collect all BUSY signals (TTC-PON time multiplexed upstream) from the detectors and forward them to the CTP where an overall BUSY mask will be built. The new trigger system and the prototype of the trigger board will be presented.

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Session Classification: POSTER Session

Track Classification: Trigger
ATCA Thermal Management Study for the ATLAS Phase-II Upgrade

Wednesday, 13 September 2017 17:45 (15 minutes)

The AdvancedTCA (ATCA) telecom industry standard has been selected as the hardware platform for the "Phase-II Upgrade" of ATLAS at the Large Hadron Collider (LHC) at CERN.

In November 2014 a project dedicated to the study of the impact of the ATCA integration in the actual counting rooms was launched analyzing the impact on the cooling infrastructures. A spare rack equipped with two ATCA shelves, high power dissipating load blades, temperature and air velocity sensors were installed in a lab. Vertical and horizontal cooling performance were checked and some critical aspects identified.

The test results will be presented.

Summary

The AdvancedTCA (ATCA) telecom industry standard has been selected as the hardware platform for the "Phase-II Upgrade" of the back-end electronics systems of the ATLAS experiment at the Large Hadron Collider (LHC) at CERN. This hardware is going to replace part of the actual electronic equipment, mostly based on VME, and less demanding in terms of cooling performances.

For historical reasons at ATLAS experiment the electronics equipment in the so-called LHC racks are cooled by a closed vertical recirculating airflow system from bottom to top. All such racks are equipped with a main ventilation unit housing a smoke detection system on top of other ambient temperature sensors. This existing airflow system is not compatible with the default telecom industry ATCA standard based on horizontal airflow. Additionally, ATCA boards will dissipate a significantly larger power with respect to the actual equipment and the cooling performance of the existing rack infrastructure could become an issue.

During 2014, the Electronics Systems for Experiments (PH-ESE) group at CERN, has launched an evaluation project that mainly focuses on the electronics infrastructure itself towards the proposal of common specifications across the LHC experiments. However, the integration of these new shelf types in the existing rack infrastructure of the ATLAS experiment must be assessed separately especially the impact on the room cooling and noise. For this reason, the ATLAS technical coordination launched in November 2014 a project dedicated to the study of the cooling infrastructure capabilities for the upgrades.

An ATCA shelve can house up to 14 blades, the target max power dissipation foreseen is 450W/blades. Thus the total power dissipated by one shelve, including the required internal fan power, can exceed 7 kW. For the cooling integration study, a spare rack was equipped with about 200 temperature sensors, two ATCA shelves equipped with 28 load blades in total, 14 of them were limited to a maximum power dissipation of 350W.blade while the others could dissipate up to 600W.blade: the average power dissipation of 450W.blade could be checked properly.

Different shelf layouts (vertical and horizontal airflow), power loads, number of heat exchangers, fans configurations, failure modes and low water temperature configurations were tested and compared with simulations carried out by an ATCA shelf manufacturer. Many conditions were tested in order to assess the impact on the counting room environment (i.e.: air conditioning, noise, etc.). The very high noise level of these shelves was another important aspect to be studied; some preliminary tests on the integration of sound proofing panels in the rack were carried out too.
The project aimed also to provide guidelines to the electronic developer regarding the cooling limits of the racks in terms of horizontal and vertical airflow distribution homogeneity through the boards. The recommendations resulting from this study will be relevant also for the other LHC experiments that will based on ATCA their electronics systems upgrades.

The results of the whole rack cooling and integration test campaign, the cooling performances and improvements as well as the resulting conclusions will be presented.

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**Session Classification:** POSTER Session

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Quality Control Considerations for the Development of the Front End Hybrid Circuits for the CMS Outer Tracker Upgrade

Tuesday, 12 September 2017 08:55 (25 minutes)

The upgrade of the CMS Outer Tracker for the HL-LHC requires the design of new double-sensor modules. They contain two high-density front end hybrid circuits, equipped with flip-chip ASICs, passives and mechanical structures. First prototype hybrids in a close-to-final form have been received from three manufacturers. To qualify these hybrids a test setup was built, which emulates future tracker temperature and humidity conditions, provides temporary interconnection, and implements testing features. The system was automated to minimize the testing time in view for the production phase. Failure modes, deliberately implemented in the produced hybrids, provided feedback on the system’s effectiveness.

Summary

The second phase of the LHC operation imposes demanding requirements on the particle detectors. The total dose of particle collisions will be raised by a factor of 10 beyond the original design value (from 300 to 3000 fb⁻¹). The luminosity increase results in higher radiation and data rate. A complete replacement of the CMS Outer Tracker is foreseen to cope with these new constraints. Its design is optimized to provide the most useful and accurate information about the trajectories of the collision products, together with a reduction of the necessary data flow. To achieve these goals several features are implemented at the level of front end modules, such as lower mass, Level 1 track triggering functionality, data compression and a higher density of sensing channels.

The functional building blocks of the future CMS Outer Tracker structure are two types of double-sensor modules. Both types will be produced in different versions that vary in the distance between their sensor planes. Each module contains two high-density front end hybrid circuits. These hybrids host binary readout flip-chip ASICs, which are connected with silicon strip sensors. Additionally, each hybrid is equipped with auxiliary electronic components and mechanical reinforcement structures, which also serve as a cooling interface. In total ten different front end hybrid geometries are foreseen in the design of the future tracker. It is planned to produce as many as thirty thousand pieces.

The quality of delivered hybrids must be verified before they are used for module assembly. Testing is crucial in order to ensure a high yield of fully functioning modules during the production phase. Mechanical, electrical and functional test protocols are evolving to address possible failures affecting the hybrid’s performance. In the life time of the new CMS Outer Tracker, the temperature in the tracking volume will be gradually decreased below -30°C. A low temperature setup was built to conduct tests in an environment representative of the tracker operating conditions, requiring a specifically designed testing infrastructure. The constructed device cools the hybrid directly via its thermal contacts while protecting it against the humidity condensation. A dedicated software was developed to provide an environment control feature integrated with functional test algorithms, both automated in order to minimize the time consumption in view for the usefulness and scalability during the mass-production.

The first prototype front end hybrid variant, which matches the desired, close-to-final geometry, has been produced in 2017. Batches of mechanically compliant pieces were received from three manufacturers. Each batch was made and assembled using a different process with a unique set of design constraints and achievable product quality. Deliberately implemented failure modes and
an on-board temperature monitoring were used to characterize the test system as well as the developed functional testing procedures. The performance results are presented in terms of the quality control effectiveness, time consumption and hybrid cooling properties. The conclusions drawn from this experience have guided the strategy of the quality verification for the mass production phase of front end hybrids for the CMS Outer Tracker upgrade.

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**Session Classification:** Production, Testing and Reliability

**Track Classification:** Production, Testing and Reliability
NEBULA Large Band Digitiser for Radio Astronomy

Monday, 11 September 2017 16:55 (25 minutes)

NEBuLA is a large band autonomous digitiser under development, with use cases in radio astronomy. We present the scientific rationale and the specifications of the project. We describe the board overall architecture, the implementation of the different links: synchronisation, command, control and data transfer. We present the solution adopted to fulfil the main requirement of the project which is the possibility to synchronise the clocks of multiple boards separated by distances up to several km. Finally, we present the firmware and the software that we have developed for debugging, control and configuration and data transfer.

Summary

The PAON is the demonstrator of a transit radio interferometer radio devoted to make 3D map of the hydrogen in the universe through observation of the 21 cm emission of the atomic hydrogen at 1420 MHz.

Paon IV is composed of 4 dishes, with a diameter of 5 meter, and uses interferometric beam forming technique to map the sky. Each antenna is equipped with a dual polarisation feed connected to 2 acquisitions’ channels of 250Mhz bandwidth at 1375 MHz.

A frequency down conversion is performed by modules located under the antenna. A centralized VME crate including ADC boards, which sample the analogue signal at 500Mz, performed 8096 points FFT and transfer data on optical fibre to a PC farm for visibility computation.

One of the limitation of the current centralised acquisition system is the long length of coaxial cables, which are responsible of modulation by standing waves. This modulation limits the system performance and complexities the offline data processing. To deal with this problem we have developed a distributed architecture with ADC boards that could be deployed directly on the antennas. As a consequence, an efficient distributed clock synchronisation is mandatory, as well as a very low level EM field emission.

The Nebula board is an xTCA full size board base on ARRIA V GT FPGA which can also work in stand alone mode. It requires 12 V power supply and 2 optical links. It also include one 2 channels 1Gsp ADC a ADC08DC1020 from TI .

The clock synchronisation and the time distribution is performed by the white rabbit protocol which allows also the transmission of control and configuration signals of the board. The data transfer is handled by 2 x 10Gb links.

For the ADC clock, we can tolerate a maximum jitter of 300 fs. To obtain this low jitter level we use a LMK04828 in the white rabbit loop, the latter generates all the clocks of the board (10Gb Ethernet, 1Gb Ethernet, ADC, FPGA system). On chips configuration bus and the IPMI protocol is done by uC ATMEGA128. QDRII and FPGA parallel flash configuration are also implemented.

When NEBULA boards are plugged in a crate, the Ipbus should be used in place of the White Rabbit to configure and control the board.

For reading data, PCIe 4x Link is connected to the backplane. We mainly use the QSYS tool to
develop the system firmware. All the FPGA functions are interconnected by the Avalon bus. A specific interface has been defined for a dedicated link: white rabbit and Ipbus. A Control panel has been developed in QT for board debugging. Specific data acquisition and visibility computation software, as well as data visualisation tools using the SOPHYA C++ class library has been developed and runs on the PCs farm.

A more advanced version of the NEBuLA board is under development, to add local computation capability and to have a more versatile system, based on ARRIA 10Soc and replacing the ADC by one FPGA Mezzanine Card (FMC) socket.

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**Session Classification:** Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Manufacturing Experience and Test Results of the PS Prototype Flexible Hybrid Circuit for the CMS Tracker Upgrade

Thursday, 14 September 2017 14:50 (25 minutes)

The CMS Tracker Phase Two Upgrade for HL-LHC requires High Density Interconnect (HDI) flexible hybrid circuits to build modules with low mass and high granularity. The hybrids are carbon fibre reinforced flexible circuits with flip-chips and passives. Three different manufacturers produced prototype hybrids for the Pixel-Strip type modules. The first part of the presentation will focus on the design challenges of this state of the art circuit. Afterwards, the difficulties and experience related to the circuit manufacturing and assembly are presented. The description of quality inspection methods with comprehensive test results will lead to the conclusion.

Summary

Components for the Compact Muon Solenoid (CMS) Tracker Phase Two Upgrade for the High Luminosity Large Hadron Collider (HL-LHC) are currently under development. Modern HDI circuits are essential to address the requirements imposed by HL-LHC. The upgraded CMS Tracker will use two main types of modules: the Pixel-Strip (PS) modules for the inner tracker and the Strip-Strip (2S) modules for the outer tracker. Both types of modules are based on flexible hybrid circuits folded and wire-bonded to the strip sensors and the Macro Pixel Asics (MPA). The front-end hybrid circuits host the binary readout ASICs and provide the interconnect to the sensors and other system elements.

A PS front-end hybrid circuit prototype was designed to exercise and test the flip-chip soldering technology, carbon fibre stiffener lamination, assembly procedures, production testing and module construction. The first part of the presentation will focus on the design practices, such as: HDI circuit design, design for testability and design for producibility. The circuit integration into the module and the tracker will be described.

Three manufacturer consortia produced the PS prototype hybrid circuits using different manufacturing processes and different assembly routines. Each manufacturer had various difficulties during the production (insufficient surface flatness, open and short circuits, thermal expansion coefficient difference). We will present the cause of difficulties and explain the available solutions in the design and production phases.

The quality of the produced hybrid circuits was inspected by X-ray, visual microscopy and cross section analysis. The electrical functionality was tested with a narrow pitch needle probe tester or a test connector interconnecting the hybrid circuits to the test system. A test interface printed circuit board (PCB) was designed to aid the measurements and host the needle probe tester and the test connectors. The feasibility of production testing was studied based on the test system designed for the PS hybrid circuit prototypes. The properties of the test interfaces (contact resistance, frequency response, cross talk between contacts, high-speed performance) were characterized in room temperature and in the cold. In addition, the hybrid electrical properties were measured (impedance characterization, via resistance). The reliability of the flip-chip bonding and the via structures were tested. We will present the various test results and show their relationship with the applied manufacturing and design techniques.
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Presenter: KOVACS, Mark Istvan (CERN)

Session Classification: Packaging and Interconnects

Track Classification: Packaging and Interconnects
Characterization of a 9-Decade Femtoampere ASIC Front-End for Radiation Monitoring

Monday, 11 September 2017 17:20 (25 minutes)

An ultra-low current sensing digitizer circuit for radiation monitoring for personnel and environmental safety was designed. The ASIC includes some key functionalities like on-chip active leakage current compensation and multi-range charge balancing. The calibration procedure and the measurements of the Ultralow Picoammeter 2 (Utopia 2) ASIC are presented. This chip can measure input current over a wide dynamic range of 9 decades starting from a few femtoampere. The ASIC has been characterized for its ultra-low current performance in the Swiss Federal Institute of Metrology. Radiation measurements when the front-end was connected to the ionization chambers used at CERN are presented.

Summary

The existing detectors used at CERN for background environmental radiation monitoring and radiation protection, provide an output current that varies from a few femtoampere up to the microampere range. A demonstrator ASIC named Utopia 1 [1], gave us the possibility to investigate the effect of the different leakage current sources present at the input of the front-end. This front-end is based on the current to frequency converter architecture and is designed for ultra-low leakage current behavior. The dominant leakage current in the input of the ASIC proved to be the leakage related to the ESD protection diodes.

The Utopia 2 ASIC is based on a two-channel compensating principle and charge balancing. The compensating channel whose input structures are matched to the measuring channel can subtract the leakage current that it is measuring from the first channel’s input. Thus, by active on-chip leakage current compensation, channel 1 can measure the input current that is related only to the radiation detector’s output.

This approach offers many advantages for ultra-low current measurements, since the leakage current of the ESD diodes is susceptible to temperature variations. Provided an initial calibration has been performed, the Utopia 2 ASIC is able to measure current over a wide dynamic range of 9 decades. Due to the current to frequency architecture, sufficient time has to be allocated for the sub-picoampere current measurements. This is compatible with the application since lower radiation can be accompanied by slower measuring time.

This article presents the characterization of the Utopia 2 ASIC. The testbench and the calibration procedure of the most important parameters of the ASIC are discussed. The measurement results, when various currents were injected using standard laboratory current sources are presented. The characterization in the ultralow currents range was performed in the Swiss Federal Institute of Metrology (METAS), where an accurate calibrated current source was used to inject current as low as 1 fA [2].

The Utopia 2 ASIC is able to digitize currents from 1 fA up to 5 μA and fulfills the specifications that are required for the new radiation monitoring system for personnel safety at CERN. Finally, the background radiation measurements when the front-end was connected to the detector and measurements with sources are shown.

References:
front-end ASIC for ionising radiation monitoring with femto-amp capabilities. Journal of Instrumentation, 11(02), C02071.


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**Session Classification:** ASIC

**Track Classification:** ASIC
Design and Implementation of Custom DMA Controller for the ALICE CRU, to Optimize Data Transfer Reducing the CPU Utilization

Wednesday, 13 September 2017 17:45 (15 minutes)

The CRU (Common Readout Unit) is the new readout card that will be used in ALICE during Run 3. The card will receive detector data and it will store the information in the memory of the PC through DMA. To handle the high data throughput an Altera Arria 10 FPGA has been installed on the CRU. A custom DMA controller has been developed to optimize the DMA data transfer reducing the CPU utilization. The paper describes the details of implementation and the communication between software and firmware. It also shows the results obtained during the test concerning data throughput and PCIe usage.

Summary

ALICE (A Large Ion Collider Experiment) is preparing a major upgrade and starting from 2021, it will collect data with several upgraded sub-detectors. The ALICE readout system will be upgraded as well, with a new detector data link called GBT (Giga Bit Transceiver) and new PCIe (Peripheral Component Interconnect) gen.3 x16 interface card called CRU. The card will receive several GBT links in input, up to a maximum of 36 and it will store the data in the memory of the PC through two PCIe gen.3 x8 performing DMA (Direct Memory Access). The raw data bandwidth of PCIe in gen3.x16 mode is 128 Gb/s. The CRU is equipped with an Altera Arria 10 FPGA that provides two PCIe endpoints gen.3 x8 to accommodate the high incoming data throughput. DMA is used to transfer data to the main memory of the server hosting the CRU. In Run 3, the readout servers will use the CRU to collect data from the detectors and store it in the memory.

The DMA engine works based on descriptor that contains two types of information, page size and location of the transfer. The page size of each descriptor supported by the DMA engine is of the order of Kbytes. One single DMA transaction belongs to one single descriptor. The DMA controller pulls descriptor one after another from host memory and push them towards the DMA engine to produce pipelined DMA transfers in order to achieve high performance (85% of the raw data bandwidth). The controller also updates the host side status memory associated with each descriptor when single descriptor gets executed i.e. successful transfer of one page. Software checks the status memory continuously and makes another page available for next DMA transaction upon arrival of status for the previous one. So, in principle, the status memory is updated after every page transfer and software has to react at that pace to maintain the pipeline. This high interaction rate due to small page size leads to high CPU utilization. The ALICE readout software running on the server that hosts the CRU can’t be dedicated entirely to the DMA transfer as there are many other tasks that must run in parallel such as data online processing and data transport over the network. For this reason, the new readout software will allocate multiple big buffers (size ~ few Mbytes to Gbytes), called super pages and share the source addresses and availability of each one with the CRU. Based on that the custom DMA controller will generate descriptors page wise and fill those super pages as per the availability. The firmware provides the number of successful DMA transfers done to the software who decides which super page can be re-allocated and used again by the CRU. In this way, the CPU utilization is reduced to the minimum without reducing the DMA performance. This approach will also reduce the logic and memory used for managing descriptor.
and status memory, reducing the PCIe transaction rate considerably.

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**Session Classification:** POSTER Session

**Track Classification:** Programmable Logic, Design Tools and Methods
ATLAS ITk Short-Strip Stave Prototype Module with Integrated DCDC Powering and Control

Tuesday, 12 September 2017 16:45 (15 minutes)

The prototype Barrel module design, for the Phase II upgrade of the of the new Inner Tracker (ITk) detector at the LHC, has adopted an integrated low mass assembly featuring single-sided flexible circuits, with readout ASICs, glued to the silicon strip sensor. Further integration has been achieved by the attachment of module DCDC powering, HV sensor biasing switch and autonomous monitoring and control to the sensor. This low mass, integrated module approach benefits further in a reduced width stave structure to which the modules are attached. The results of preliminary electrical tests of such an integrated module will be presented.

Summary

The Phase II upgrade of the ITk detector at the LHC requires the modules to have high density channel counts whilst also maintaining minimal material to ensure their optimum performance within a tracking environment. For the ATLAS ITk Short-Strip Stave Module, material reduction has been achieved by a multifaceted approach. The front-end readout ASIC count has been reduced by a factor of two, compared to previous prototype versions, by the scaling up of the number of channels from 128 to 256; this has been realised in the ABC130 ASIC fabricated in 130nm CMOS technology. The readout ASICs are then attached to a low mass single-sided flexible circuit, of minimal width, whose layer count has been reduced by adopting an asymmetric circuit stack-up; with the power supply Ground plane on the bottom (which is referenced to the sensor), removing the requirement for a dedicated shield layer. Test results showing that digital pickup into the sensor is only evident at front-end comparator thresholds well below the nominal setting for normal operation.

Due to geometrical constraints, the module powering, HV sensor switching and control have also been attached to the silicon strip sensor. The integration of front-end readout ASICs and their carriers plus powering, switchable sensor biasing and autonomous monitoring and control results in a compact, self-contained module topology. This is beneficial for the stave structure, to which the modules are attached, as the stave width can be further reduced due to the module powering and control being no longer required to reside on the stave as initially proposed. The integration of module powering, HV sensor switching and control ASIC has been realised by the development of a separate power board. A novel feature of the powering block is the use of a DCDC buck converter, based on the CERN FEAST2 ASIC. Due to the nature of their operation, buck converters can have large EMI emissions which can produce induced noise into both the silicon strip sensor and front-end readout ASIC. Limitations in both height and width make it non-trivial to fit a toroidal coil of the nominal inductance, this would be the preferred choice of coil due to its low EMI; instead a solenoid type was chosen. The adoption of a low mass, mixed material (Al/Cu), shielding solution has been shown to work very well in the attenuation of EMI whilst still maintaining a target efficiency of 75% at the nominal load of 2A.

Prototype modules and power boards have been constructed and shown to work very well, with the integrated module performance meeting the module design specification.

The work is relevant to the power topic. The conclusion is that with correct design it is possible to obtain good low noise performance of silicon detector modules using DCDC converters even when located in close proximity to both silicon sensor and sensitive front-end electronics.
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Session Classification: POSTER Session

Track Classification: Power, Grounding and Shielding
Multi-Gigabit Wireless Data Transfer for High Energy Physics Applications

Tuesday, 12 September 2017 17:20 (15 minutes)

The future of connectivity is wireless, and the HEP community is not an exception. The demand for high capacity data transfer continues to increase every year at a significant rate. For example, the tracking detectors require readout systems with several thousand links that has to handle a data transfer of multiple-gigabit/s each. We propose to use the millimeter-wave band between (57-66 GHz). This 9 GHz band is very attractive in order to achieve high data transfer rate. This talk present current development of the 60 GHz transceiver chip for HEP applications. Studies of antenna and data transmission will be shown.

Summary

The future of connectivity is wireless, and the HEP community is not an exception. The demand for high capacity data transfer continues to increase year over year at a significant rate. This is a continuously race where technology and applications developers push into higher and higher bandwidths. For example, the tracking detectors require readout systems with several thousand links that has to handle a data transfer of multiple-gigabit/s each. Also, due to the high granularity of these links, stringent requirements are also specified on space, material and power consumption. Wireless technique have also developed extremely fast the last decade and are now mature for being considered as a promising alternative to cables and optical links that would revolutionize the detector design. In this context has the WADAPT (Wireless Allowing Data and Power Transmission) consortium been formed to identify the specific needs of different projects that might benefit from wireless readout techniques. The millimeter-wave band (mmw) is defined where the wavelength varies from ten millimeters (30 GHz) down to 1 millimeter (300GHz). In this consortium we will concentrate on data transfer communication in the 60 GHz band (57 GHZ - 66 GHz). This license free 9 GHz band is very attractive in order to achieve a high data rate transfer. In addition it provides a small form factor, material reduction, high material penetration loss, narrow beam width and high path loss. These features, and due to the operation in a very well controlled environment with line-of-sight operation, makes the 60 GHz band optimal for short range operation as in a detector environment. This talk present current developments of the 60 GHz transceiver chip for HEP applications. Studies of antenna and data transmission will also be shown. An International collaboration for an R&D on wireless readout is sent to CERN, and is now under evaluation.

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Session Classification: POSTER Session

Track Classification: ASIC
Irradiation Test Results of the ALICE SAMPA ASIC

Wednesday, 13 September 2017 17:45 (15 minutes)

This paper will present the irradiation test results performed on the first two prototypes (MPW1 and V2) for the new readout ASIC (SAMPA). The SAMPA chip is aimed to be used in the ALICE Time Projection Chamber detector (TPC) and ALICE Muon Chamber (MCH) detector during RUN3 starting in 2021. The irradiation tests have been performed using proton beams of 180 MeV.

Summary

During RUN3 at LHC, the expected interaction rate of the lead ions for the ALICE experiment will be increased from 10 kHz to 50 kHz. The present readout electronics does not cope with the higher collision rates for the TPC and MCH detectors. Thus a new custom-made, trigger-less and continuous readout chip SAMPA is currently being developed to replace the current readout electronics in both detectors.

The SAMPA chip is designed in a 130 nm TSMC technology with a nominal supply voltage of 1.25 V. SAMPA includes 32 data processing channels, each containing a charge-sensitive pre-amplifier, a shaper, a 10-bit 10 MHz SAR ADC followed by a Digital Signal Processor (DSP). The data readout takes place, either in continuous or triggered mode, by enabling up to eleven 320 Mbps SLVS serial links, allowing a data throughput of up to 3.2 Gbps.

With the increased interaction rate expected during RUN3, the radiation load on the new SAMPA chip will consequently also increase. SAMPA needs to withstand a dose up to 2.1 krad and High Energy Hadron (HEH) flux of 3.4 kHz/(cm²*2). HEH is the primary source of radiation induced Single Event Effects (SEE) in the ALICE readout electronics. SEE can be expected mainly in clock distribution elements, memories and registers in the DSP part of the SAMPA, which covers more than 60 % of the chip area. Irradiation campaigns are therefore necessary to investigate the radiation tolerance of the SAMPA.

This paper will focus on the irradiation qualification of the SAMPA chip with respect to the relevant radiation environment. Two proton beam irradiation campaigns were conducted for SAMPA MPW1 and V2 prototypes at The Svedberg Laboratory (TSL) in Uppsala and Center of Advanced Radiation Technology (KVI) in Groningen respectively. The results from both campaigns will be compared and presented.

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Presenter: MAHMOOD, Sohail Musa (University of Oslo (NO))
Session Classification: POSTER Session
Track Classification: Radiation Tolerant Components and Systems
CBC3: a CMS Micro-Strip Readout ASIC with Logic for Track-Trigger Modules at HL-LHC

Monday, 11 September 2017 16:30 (25 minutes)

The CBC3 is the latest version of the CMS Binary Chip for readout of the outer radial region of the upgraded CMS Tracker at HL-LHC. This 254-channel, 130nm CMOS ASIC is designed to be bump-bonded to a substrate to which sensors will be wire-bonded. It will instrument double-layer 2S-modules, consisting of two overlaid silicon micro-strip sensors with aligned micro-strips. On-chip logic identifies L1 trigger primitives from high transverse-momentum tracks by selecting correlated hits in the sensors. Delivered in late 2016, the CBC3 has been under test for several months, including x-ray irradiations and SEU testing. Results and performance are reported.

Summary

The CBC3 is the latest version of the CMS Binary Chip ASIC for readout of the outer radial region of the upgraded CMS Tracker at HL-LHC. It advances the technique of identifying L1 trigger primitives (“stubs”) first demonstrated by its forerunner the CBC2, and introduces many new features, such as stub bend calculation, fast data output, and e-fuses for trimming of the new band-gap and chip identification. In addition to these new features, the performance of the analogue channel has been fine-tuned and the programmable analogue biasing improved.

Designed in 130nm CMOS, the CBC3 is a 254 channel binary readout ASIC with each channel comprised of a pre-amplifier, shaper and comparator. Channel outputs are stored in a 512-deep digital pipeline to accommodate trigger latencies of up to 12.8 microseconds. In addition to doubling capacity, the CBC3 pipeline has been redesigned to eliminate radiation induced leakage effects present on the CBC2 design. The L1-triggered data from the pipeline is now combined into a serial data packet along with a 9-bit L1 count, and output at 320 Mb/s via a differential SLVS output driver to meet the requirement of a 1 MHz average trigger rate.

Like its predecessor, the CBC3 is designed to instrument double-layer 2S-modules and includes coincidence logic for identifying potential stubs, along with programmable cluster-width discrimination and programmable geometric-offset correction. The CBC3 improves on the original stub recognition logic by increasing the resolution to half-strip and providing bend information associated with the stub’s direction. Additional logic is included to assign an 8-bit address to each identified stub and assemble a data packet containing up to three stub addresses per bunch-crossing, along with their corresponding 4-bit bend information and status flags. This data packet is divided into five bytes and output from the ASIC via five differential SLVS output drivers operating at 320 Mb/s, thus allowing the complete data packet to be sent in one bunch crossing.

The CBC3 retains the I2C compatible slow control interface for programming the configuration registers of biases and other functions, but adopts a 320 Mb/s serial command interface for fast commands such as the L1 Trigger. These commands are now received in the form of a serial 8-bit word via a differential SLVS input.

Whereas the CBC2 was able to operate off a single 40 MHz clock, the CBC3 required an additional 320 MHz clock domain for the fast I/O. To simplify module design, the CBC3 derives its own 40 MHz clock from a synchronisation pattern contained within the fast command-word data stream. This derived clock can be phase shifted by a programmable Delay-Locked-Loop in order to optimise timing relative to the bunch-crossing.

The CBC3 was delivered in late 2016, and wire-bonded prototypes were evaluated for performance. We will present results from electrical characterization including x-ray irradiations and SEU testing.
Probe testing of the remaining wafers was carried out before they were sent to be processed with bumps in readiness for mounting on a dual-chip hybrid.

Our plans for future developments will be outlined.

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**Presenter:** PRYDDERCH, Mark (STFC Rutherford Appleton Laboratory)

**Session Classification:** ASIC

**Track Classification:** ASIC
The ATLAS Muon-to-Central Trigger Processor Interface for the Phase-I Muon Trigger Upgrade

The Muon-to-Central Trigger Processor Interface (MUCTPI) of the ATLAS experiment at CERN will be upgraded for run 3 of the LHC. The current system, a full 9U VME crate, will be replaced by a single AdvancedTCA blade, based on state-of-the-art FPGA technology and high-density ribbon fibre-optic transmitters and receivers. The module uses a System-on-Chip (SoC) with a processor running an embedded Linux operating system to communicate with the experiment run control system. We present the hardware design and implementation of the module, the communication model used in the SoC as well as results from the validation of the first prototype.

Summary

The Muon-to-Central Trigger Processor Interface (MUCTPI) is part of the Level-1 trigger system of the ATLAS experiment at CERN. It receives and combines information on muon candidates from the 208 trigger sector logic modules in the barrel and endcap regions of the detector and calculates the candidate multiplicity, taking into account the possible double counting between trigger sectors due to the geometrical overlap of the muon chambers and the trajectory of the muons in the magnetic field, and sends the result to the Central Trigger Processor (CTP).

The existing MUCTPI will be upgraded for run 3 of the Large Hadron Collider (LHC), in order to interface with the new muon endcap trigger sector logic modules which will be deployed as part of the muon new small wheel upgrade. The upgraded MUCTPI will also be able to send full precision information on the muon candidates identified by the muon trigger processors at the bunch crossing rate to the topological trigger processor (L1Topo) of the Level-1 trigger system, which will allow combined calorimeter/muon topological trigger algorithms to be implemented.

The MUCTPI upgrade requires a complete redesign of the existing VME based system. The design is based on state-of-the-art FPGA technology (Xilinx 20 nm UltraScale devices), featuring a large number of on-chip high-speed serial transceivers, and high-density ribbon fiber optics receiver and transmitter modules. These technologies allow a much higher integration of the new MUCTPI and enable the implementation of all the required functionality on a single AdvancedTCA (ATCA) blade. In comparison, the existing system requires a full 9U VME shelf with 18 boards. The module features over 270 multi-gigabit optical inputs/outputs operating at line rates between 6.4 and 12.8 Gbit/sec, resulting in an aggregate bandwidth of over 2 Tbit/sec.

Two large Virtex UltraScale FPGAs (sector processors), each covering one side of the detector, are used to receive and process the muon trigger data from the 208 sector logic modules. The sector processor FPGAs also send lists of muon candidates with their full precision information to L1Topo through up to 48 serial optical links.

A third FPGA, a Xilinx Kintex UltraScale device, is used to merge the information from the two sides of the detector, to perform the required trigger calculations and to send the resulting object multiplicities and trigger flags to the CTP. For events accepted by the CTP, it also outputs a list of muon candidates to the DAQ system and sends Region-of-Interest (RoI) information to the high-level trigger (HLT) to seed the muon processing.

Finally a Xilinx Zynq System-on-Chip (SoC) FPGA is used to interface the MUCTPI to the ATLAS run control system through a Gigabit Ethernet connection. It is used to configure and control the
MUCTPI and to read state and monitoring information. The SoC device runs an embedded Linux 
operating system with application-specific software using a remote-procedure-call approach. 
We present the hardware design and implementation of the module as well as results from the 
validation of the first prototype.

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**Presenter:** VICHOUDIS, Paschalis (CERN)

**Session Classification:** Trigger

**Track Classification:** Trigger
Development of the New Trigger Processor Board for the ATLAS Level-1 Endcap Muon Trigger for Run-3

Wednesday, 13 September 2017 17:45 (15 minutes)

The ATLAS first-level Endcap Muon trigger in LHC Run-3 will identify muons by combining data from the Thin-Gap chamber detector (TGC) and a new detector, called the New-Small-Wheel (NSW). In order to handle data from both TGC and NSW, a new trigger processor board has been developed. The board has a modern FPGA to make use of Multi-Gigabit transceiver technology. The readout system for trigger data has also been implemented with TCP/IP instead of a dedicated ASIC. The presentation will focus on the electronics and its firmware of the ATLAS first-level Endcap Muon trigger processor board for LHC Run-3.

Summary

The LHC performance for Run-3 is expected to increase its instantaneous luminosity to $3 \times 10^{33} \text{cm}^{-2}\text{s}^{-1}$ after the Phase-1 upgrade, to take place from 2018-2020. In order to cope with this high luminosity, an upgrade of the ATLAS trigger system will be required.

The ATLAS first-level Endcap Muon trigger system identifies muons with high transverse momentum from 40 MHz bunch crossings, using data from fast muon trigger detectors, TGC. The whole system is implemented on a special trigger circuit, which makes the trigger decision latency as short as 2.2 us. In LHC Run-2, the Endcap Muon trigger requires the coincidence between TGC Big-Wheel (BW) at the middle station and the Small-Wheel at the inner station, in order to reduce the fake triggers of beam-induced backgrounds by slow-particles from the endcap toroid or shields.

In the Phase-1 upgrade, a new detector, called New-Small-Wheel (NSW), will be installed at the small wheel region. NSW provides information of finer position and direction of the track, which can be used for the trigger selection by the trigger processor board. Finer track information from the NSW can be used as part of the trigger logic to enhance performance significantly. We aim to keep the trigger rate for muons with $p_T > 20 \text{ GeV/c}$, at the same level as it is now.

In order to handle data from both TGC and NSW, some new electronics, including a 9U VME board known as the trigger processor, are being developed. The trigger processor board has a modern FPGA to make use of Multi-Gigabit transceiver technology, which will be used to receive data from the NSW. The firmware implemented in a FPGA on the trigger processor board consists of two major parts, trigger and readout. The trigger part does to receive data, to calculate the muon momentum with a fixed latency, and to output the trigger decision to the central trigger system. The readout system for trigger data has also been re-designed, with data transmission implemented with TCP/IP instead of by a dedicated ASIC, by using SiTCP technology. This makes it possible to minimize the use of custom readout electronics and instead use some commercial PCs and network switches to collect, format, and send the data.

This presentation will describe the aforementioned upgrades of the first-level Endcap Muon trigger system. Particular emphasis will be placed on the new Sector Logic electronics and the firmware. The performance of the software readout system, and the latest results of the trigger performance study for LHC Run-3 will be also discussed.
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Presenter: MIZUKAMI, Atsushi (High Energy Accelerator Research Organization (JP))
Session Classification: POSTER Session
Track Classification: Trigger
ASICs and Readout System for a High Resolution UV Single Photon Imagining Detector

Tuesday, 12 September 2017 17:40 (20 minutes)

Large aperture MCP based UV single photon imaging detectors are commonly used in space applications. NASA granted the development of a new detector with a geometrical acceptance up to a 100x100 mm, as well as ASICs for the construction of its readout system. We developed the detector and ASIC chips which enabled the construction of its readout system. The system is composed of fast, low noise and low power 16ch CSA amplifier ASICs, and 16ch waveform sampling GSPS ASICs. The detector and readout system are currently under evaluation, meanwhile a novel and even more compact readout system on chip is undergoing design process.

Summary

The Department of Physics and Astronomy (ID Lab) at University of Hawaiʻi and Space Sciences Laboratory, Berkeley, collaborate on the development of a UV single photon imaging detector with crossed strip readout. The detector uses a photo-cathode to convert single photons into photoelectrons and an MCP stage for charge multiplication. The photon income position is extrapolated by measuring the charge cloud distribution over orthogonal anode strips being 25um wide and 625um apart. Our base line detector has an aperture of 50x50mm, hence the readout system needs to measure 160 channels. Using an older laboratory readout system, a spatial resolution of 17um FWHM was measured [1]. Space grade instruments require to operate at very low power, low noise and enable high count rate.

We developed a 16 channel charge sensitive amplifier (CSA) ASIC [2] in 130 nm TSMC-CMOS technology. It features a linear range up to 50fC, baseline gain of 10mV/fC, noise figure of ~600e-, analog pulse rise time of 25ns, and power consumption of ~5mW per channel. Its partnering ASIC, called Half-Graph, is a 16 channel waveform sampling and digitizing GS/s ASIC. The sampling capacitor array, along with an analog storage array, enables to keep about 8 us of data per channel. An external FPGA is used to access the analog memory array and convert the stored values using the ASIC internal 12 bit slope converter. Converting only the data of interest enables efficient data throughput, hence a high single photon count rate. The HalfGraph was irradiated with 225kRad without observable issues. Both chips have been irradiated with gamma rays. The CSA sustained 850kRad dose without notable degradation. Both could qualify for Jupiter missions with appropriate shielding, where the requirement is to functionally pass a dose of 200kRad.

Both chips are programmable to reduce required external biasing components for operation. Using these ASICs we constructed a scalable self triggered readout system, which is presently under evaluation coupled to the 50x50 mm detector. The 160 channel system constitutes of 10 CSAs and 10 Half-Graphs. The power consumption ranges around 12W, and this number includes as well 2 ARTIX 7 FPGAs required for controlling the system. A new 100x100mm aperture detector along with a scaled readout system are under construction.

To further decrease the power consumption, reduce the system complexity and shrink the package footprint, we design a new ASIC called GRAPH. This ASIC will encapsulate a CSA and a GS/s ADC on a single die using 130nm TSMC technology. We present the ASICs and the readout system for the 50x50 mm detector, obtained results and share details on the GRAPH architecture.

[1] J. Vallerga et al., " Development of a flight qualified 100 x 100 mm MCP UV detector using advanced cross strip anodes and associated ASIC electronics ", Proc. SPIE 9905, Space Telescopes
and Instrumentation 2016

[2] A. Seljak et al., A fast, low power and low noise charge sensitive amplifier ASIC for a UV imaging single photon detector, JINST 2017

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Presenter: Dr SELJAK, Andrej (UH Hawai‘i Manoa)

Session Classification: POSTER Session

Track Classification: ASIC
Development of the jet Feature EXtractor (jFEX) for the ATLAS Level 1 Calorimeter Trigger upgrade at the LHC

Monday, 11 September 2017 15:40 (25 minutes)

To cope with the enhanced luminosity delivered by the Large Hadron Collider in 2021, the ATLAS experiment has planned a major upgrade. The first level trigger based on calorimeter data will be upgraded to exploit fine-granularity readout using a new system of Feature Extractors (FEXs), each optimized to trigger on different physics objects. This presentation is focused on the jet FEX. The main challenges of such a board are the input bandwidth of up to 3 Tb/s, dense routing of high-speed signals and power consumption. We report on design, firmware development and results of integrated tests of a prototype.

Summary

To cope with the increased luminosity after Long Shutdown 2, ATLAS has planned a major upgrade of the sub-detectors. The Level 1 calorimeter trigger system is redesigned taking advantage of the latest technology available to exploit higher granularity data from the calorimeter. It consists of three subsystems, called Feature Extractors (FEXs), each optimized to trigger on different physics objects: eFEX (electromagnetic FEX) identifies electron, gamma and tau signatures; jFEX (jet FEX) identifies jets and large-area taus and calculates energy sums including missing transverse energy; gFEX (global FEX) identifies large-area jets and calculates global variables. This presentation focuses on the jFEX prototype, its design, performance tests and the ongoing firmware development. The board design is based on the ATCA specifications, consists of 24 layers of MEGTRON6 and it hosts four FPGAs from the Xilinx UltraScale family (XCVU190FLGA2577). The selected FPGA model presents one of the largest number of MGT links available within the Virtex UltraScale family. 7 jFEX modules will be produced covering the whole calorimeter with different granularity depending on the detector region.

The jFEX design presented several challenges: The high input bandwidth of up to 3 Tb/s combined with the on-board data duplication results in a dense routing of over 500 differential high-speed signals. This duplication is required due to a limited optical input capacity. The used PMA loopback method allows data duplication without any signal splitting or additional devices at the cost of some latency. 20 opto-electrical receivers feed the incoming data from 240 fibers to the FPGAs and four opto-electrical transmitters send the processed data of the algorithms to the next stage in the trigger system, the Topological Processor (L1Topo), via 48 optical fibers. The worst case estimate for the power consumption of the whole board is about 500 W. This required careful planning of the power planes including simulations of current densities and voltage drops and simulations on signal integrity.

An extension mezzanine is used, where the Xilinx Zynq System on Chip manages board control and FPGA communication via IPBus. After production and assembly of the jFEX prototype the board has been tested in Mainz and during integrated tests at CERN. In parallel there is an ongoing firmware development of algorithms and infrastructure.
Primary author:  STAMEN, Rainer (Ruprecht-Karls-Universitaet Heidelberg (DE))
Presenter:  WEIRICH, Marcel (Johannes Gutenberg Universitaet Mainz (DE))
Session Classification:  Trigger
Track Classification:  Trigger
The Development of the Global Feature eXtractor (gFEX) for the ATLAS Level 1 Calorimeter Trigger at the LHC

Wednesday, 13 September 2017 17:45 (15 minutes)

During the ATLAS Phase-I upgrade, the global feature extractor (gFEX) will be designed to maintain the trigger acceptance against the increasing luminosity for the ATLAS Level-1 calorimeter trigger system. The prototypes v1 and v2 have been designed and tested in 2015 and 2016 respectively. With the lessons learned, a pre-production board with three UltraScale+ FPGAs and one ZYNQ UltraScale+, and 35 MiniPODs is implemented in an ATCA module. This board will receive coarse-granularity information from the entire ATLAS calorimeters on up to 300 optical fibers and each FPGA has 24 links to the L1Topo at the speed up to 12.8Gb/s.

Summary

The Large Hadron Collider (LHC) will undergo a series of upgrades to increase both collision energy and luminosity in next ten years, and the ATLAS experiment will follow the same upgrade schedule. During the Phase-I upgrade, a new component - global feature extractor (gFEX) will be designed to maintain the trigger acceptance against the increasing luminosity for the ATLAS Level-1 calorimeter trigger system. The gFEX is designed to identify patterns of energy associated with the hadronic decays of high momentum Higgs, W, & Z bosons, top quarks, and exotic particles in real time at the LHC crossing rate. The prototype v1 and v2 have been designed and fully tested in 2015 and 2016 respectively. The prototype v1 board is designed with one single system-on-chip processor, ZYNQ, and one Xilinx Vertex-7 FPGA for challenge technologies validation and the prototype v2 board is design with three Vertex UltraScale FPGAs and one ZYNQ for the full functionalities and performance test. Both gFEX prototypes have been developed and evaluated successfully. The gFEX prototype v1 has been used in the LArL1Calo link speed test, to determine the baseline link speed of 11.2Gb/s. The prototype v2 has been designed and tested in the lab. High-speed fiber-optic links are stable at 12.8 Gbps, and on-board electrical links are stable at 25.6 Gbps. Parallel buses operate at 1.12 Gb/s with good margin. The integration test with FELIX has been successful, and now the prototype v2 is being used as firmware development platform.

With the lessons learned from these two prototype boards, a pre-production board with three Xilinx UltraScale+ FPGAs and one MPSOC ZYNQ UltraScale+, and 35 MiniPODs is implemented in an ATCA module. This board will receive coarse-granularity information from the entire ATLAS calorimeters on up to 300 optical fibers at the speed up to 12.8 Gb/s synchronized to 40 MHz LHC clock frequency and each FPGA has 24 links to the L1Topo at 12.8 Gb/s. The ZYNQ UltraScale+ will be the only one to communicate with FELIX for the TTC clock recovery and data transfer. It is also used to control and configure all the three processor FPGAs, monitor board health, and interface to Gigabit Ethernet and UART. Now, the routing of the pre-production board is almost done and will be sent out for fabrication in the May. We will bring it up around July and will present the performance on the meeting.

Primary author: STAMEN, Rainer (Ruprecht-Karls-Universitaet Heidelberg (DE))
Presenter: TANG, Shaochun (Brookhaven National Laboratory (US))

Session Classification: POSTER Session

Track Classification: Trigger
Hardware Trigger Processor for the ATLAS MDT System

We are developing a low-latency hardware trigger processor for the Monitored Drift Tube system in the ATLAS muon spectrometer. The processor will fit candidate muon tracks in the drift tubes in real time, improving significantly the momentum resolution provided by the dedicated trigger chambers. We present a novel pure-FPGA implementation of a Legendre transform segment finder, an associative-memory alternative implementation, an ARM (Zynq) processor-based track fitter, and compact ATCA blade architecture. The ATCA architecture is designed to allow a modular, staged approach to deployment of the system and exploration of alternative technologies.

Summary

The ATLAS Monitored Drift Tube (MDT) trigger system will be implemented as a set of 32 or 64 ATCA blades, each handling one or two sectors of the ATLAS muon system. Each ATCA blade will provide up to 144 optical transceivers capable of operating at 10 Gbps.

MDT hits are received in real time over GBT links from the detector with minimum latency. Simultaneously, regions of interest (ROI or seed tracks) are provided by the ATLAS muon sector logic to the trigger processor.

Matching of MDT hits to regions of interest will be performed in an FPGA on the blade. Tube coordinates are transformed to convenient chamber-local coordinates and drift time converted to a drift radius. The processed MDT hits are then passed to sector processors on mezzanine boards.

Two alternative mezzanine board designs are under consideration. The first uses content-addressable memory devices (also known as Associative Memories or AM). The AM devices store a library of all possible track patterns and compare actual hits against the track library in a massively parallelized way.

The second uses FPGA logic to implement a Legendre transform based segment finder. This logic evaluates in parallel a total of 128 possible track segment angles for each MDT hit, calculating in a fast FPGA pipeline the offset of each track candidate from an arbitrary origin for each angle and hit. The (angle, offset) pairs are used to fill a 2D histogram, with the maximum peak in the histogram representing a likely track where a number of tubes "agree" on the position and angle of a possible track.

Each station (inner, middle, outer) will process hits and identify track segments independently. All hits are then transferred back to the blade, where a Xilinx Zynq FPGA with embedded ARM processor cores will be used to evaluate a final parameterized track fit. We expect the resulting p(T) to be substantially more precise than that provided by the dedicated trigger chambers, and approach the resolution currently achieved by the off-line fitting.

A detailed conceptual design with extensive simulation studies is being prepared now, to be published in the ATLAS TDAQ TDR. A first generation of hardware prototypes is planned for 2018-2019, with a full system ready for installation during LHC Long Shutdown 3.

Primary author: STAMEN, Rainer (Ruprecht-Karls-Universitaet Heidelberg (DE))
**Presenter:** COSTA DE PAIVA, Thiago (Univ. Illinois at Urbana Champaign (US))

**Session Classification:** POSTER Session

**Track Classification:** Trigger
Prototype Chip for a Control System in a Serial Powered Pixel Detector at the ATLAS Phase II Upgrade

Tuesday, 12 September 2017 17:45 (15 minutes)

A new inner tracking detector (ITk) for the Phase-II upgrade of the ATLAS experiment is in development. A serial power scheme is foreseen for the pixel detector. This requires a new detector control system (DCS) to monitor and control the pixel modules in the serial power chain. The Pixel Serial Power Protection (PSPP) chip is an ASIC for this purpose. It operates parallel to the modules and houses an ADC and bypass. This talk presents test results with the PSPPv3 chip. It includes irradiation up to 500 Mrad and investigations of a serial power chain with up to 8 A supply current.

Summary

The upgrade of the LHC to the High-Luminosity LHC requires improved detectors. A completely new full-silicon tracker is in development for the ATLAS Phase-II upgrade. This tracker includes a pixel part with about 10 times more modules than the current version. A serial powering scheme to reduce the number of service lines to the detector is the baseline. A new detector control system (DCS) is required for a safe operation over the planned lifetime of 10 years. The current concept envisions three parallel paths for the DCS. The security path is a hardwired interlock system. This path doesn’t need any software or interaction and acts as last line of defense. The diagnostics path provides information on demand. It is merged with the regular data readout and provides the highest granularity and most detailed information. The control path is used to supervise the entire detector. This path has its own communication lines independent from the regular data readout for reliable operation.

The main elements in the control path are the DCS chip and controller. The DCS chip operates in the serial power chain parallel to the pixel modules. This imposes different operating voltages of each DCS chip in the chain. Additionally, they should be powered independent of the serial supply current. A power scheme is proposed which uses only one additional service line for the operation of the DCS chip. Each chip monitors one module and has capabilities to bypass the module. This guarantees operation of the serial chain if the module fails. The DCS chip communicates through a dedicated communication path with the controller chip. These communication has to operate with each DCS chip on a different voltage. This is realized with single ended AC coupled lines and specially developed I/O drivers. The controller receives commands by CAN from the DCS computers.

In this talk, we explain the pixel serial power protection (PSPP) chip, a prototype for the DCS chip. The third version, called PSPPv3, was designed to respect the updated power requirements and has capabilities to bypass up to 8 A. The other components in the chip are an ADC for measuring the module voltage and temperature, a communication logic implemented in triple modular redundancy (TMR) and comparators for a local module interlock. The bypass is activated automatically if the temperature or voltage go over a fixed threshold. We show results of test in the serial power chain and the operation of the PSPPv3.

The DCS chip will observe the same radiation levels as the pixel modules. Currently they are designed to work with a total ionizing dose (TID) up to 500 Mrad. We present results of irradiation
tests with the PSPPv3 chip.

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**Presenter:**  LEHMANN, Niklaus (Bergische Universitaet Wuppertal (DE))

**Session Classification:**  POSTER Session

**Track Classification:**  ASIC
Characterization of SLVS Driver and Receiver in a 65 nm CMOS Technology for High Energy Physics Applications

Tuesday, 12 September 2017 17:45 (15 minutes)

This work presents the design and characterization of a SLVS transmitter/receiver pair, to be used for I/O links in High Energy Physics applications. The prototype chip was designed and fabricated in the framework of the CHIPIX65 project and was completely characterized. The chip has been also irradiated with X-rays in order to evaluate the effect of the ionizing radiation on the signal integrity. The full characterization of the driver and receiver will be discussed in the conference paper.

Summary

A transmitter/receiver pair designed for a possible integration in the RD53A prototype, and conform to the SLVS protocol, was designed in a 65 nm CMOS technology. The proposed link, that can be operated up to 1.2 Gbps, will be used in a harsh radiation environment, so the design is based on thin gate oxide transistors, using a supply voltage of 1.2 V. The SLVS standard describes a differential current-steering protocol with a voltage swing of ±200 mV on a 100Ω termination resistance and a common mode of 200 mV. The driver architecture is based on a Bridged-Switch Current Source (BSCS) scheme. The 2 mA biasing current is switched through a 100Ω termination resistance, placed at the receiver input, according to the input data stream. The output current of the transmitter can be trimmed, by means of three configuration bits, in a range from 500 μA to 2.5 mA. In order to achieve insensitivity to PVT variations, a low power, common-mode feedback has also been included. The common mode voltage is sensed by two resistors, which are connected to the output nodes and compared with a reference voltage generated by a resistor voltage divider. The CMFB amplifier is based on a two stage Miller OTA. The receiver is based on three different stages: the first one is a fully differential amplifier with a cross-coupled load, rail-to-rail input stage, and with a bandwidth close to 1.2 GHz; the second stage is a differential-to-single ended amplifier with a full swing CMOS output voltage and the last one is a chain of three inverter. The receiver input is AC coupled for a possible use with serial powering. The common mode voltage of the signal at the input of the receiver is restored by resistor voltage divider. The CMFB amplifier is based on a two stage Miller OTA. The receiver is based on three different stages: the first one is a fully differential amplifier with a cross-coupled load, rail-to-rail input stage, and with a bandwidth close to 1.2 GHz; the second stage is a differential-to-single ended amplifier with a full swing CMOS output voltage and the last one is a chain of three inverter. The receiver input is AC coupled for a possible use with serial powering. The common mode voltage of the signal at the input of the receiver is restored by resistor voltage divider. The input of the driver was stimulated with a CMOS Pseudo-Random-Bit Signal (PRBS) and the signal integrity of the driver was evaluated by measuring the eye diagram at the termination resistance. The chip has also been irradiated, up to 550Mrad, with the X-rays machine present at CERN in order to evaluate the effect of the ionizing radiation on the signal integrity. The conference paper will report on the full experimental characterization of the SLVS transmitter and receiver.

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Presenter: DE CANIO, Francesco (Università e INFN, Pavia (IT))
Session Classification: POSTER Session

Track Classification: ASIC
Time-to-Digital Converter with Adjustable Resolution Using a Digital Vernier Ring Oscillator

Tuesday, 12 September 2017 17:45 (15 minutes)

This paper reports the development of a high resolution, low power, and adjustable in frequency Time-to-Digital Converter (TDC), based on two vernier Ring Oscillators (RO) made of standard XOR cells. The TDC is aimed at exploiting the excellent timing performance of the multigap Resistive Plate Chambers (RPC). The frequency of each RO is adjustable thanks to a 9-bit register from 340MHz to 370MHz, allowing theoretically an LSB selection down to one picosecond. The core area measures $35 \times 75 \mu m^2$ in a 130nm CMOS technology. Under 1.2V, the TDC consumes $2.3 mA_{RMS}$ and $260 nA_{RMS}$ with or without signal respectively.

Summary

A high precision time measurement detected in the RPCs of the high eta muon stations of the Compact Muon Solenoid (CMS) experiment at CERN’s LHC is expected to improve the detector performance in the High Luminosity LHC phase. A Time-to-Digital-Converter (TDC) is one of the most crucial building blocks required inside the readout electronics. The exploitation of the TDC performance can be used to reduce the data flow and increase the spatial resolution. High-resolution, better than 10ps, over a nanosecond dynamic range is required. Moreover, the power consumption has to be limited as well as the jitter (less than 5ps).

Other TDC implementation which use inverter delay line or Ring Oscillator (RO) expect a constant delay of each inverter stage. On the contrary, our novel technique take advantage of every delay cell variation. The period of the Fast RO ($T_F$) and the Slow RO ($T_S$) have $2^9$ combinations each, and their values are randomly spread in a gaussian fit around 2.8ns. The resulting LSB often called $\varDelta T$ is equal to $\varDelta T = T_S - T_F$, and could be adjust down to 1ps thanks to this fine tuning. The heart of the RO is made of XOR standard cells, one can thus choose only inverters or buffers as delay elements or a mix of buffers and inverters. A XOR gate delay in the buffer mode is in average 50 ps longer than the inverter mode, the mix of this two families of delay elements can improve the delay time in order to find the best combinaison with the smallest needed delay. This adjustable architecture offers $\frac{512 \times 513}{2}$ possible ways to configure the two ring oscillators with a random Gaussian fit around zero delay. In principle, the resolution can vary down to 10fs. However, choosing a small LSB ($\Delta t$) implies that the deadtime $\frac{\varDelta T}{\Delta t}$ increases. For robustness issue, a custom Conditional Precharge Flip-Flop (CPFF) has been designed as an optional feature. A minimum setup time of 15ps for the CPFF is measured. Consequently, the phase detector block is characterized using such a CPFF resulting in a $3ps_{RMS}$ S-curve.

A prototype of the TDC has been fabricated in 130 nm CMOS technology. The circuit occupies an area of only $35 \times 75 \mu m^2$ and consumes $2.29 mA_{RMS}$ with signal and $260 nA_{RMS}$ of leakage current without signal. The serial shift register of the ASIC is simply configurable with the spi-pins of a Raspberry-pi plateform to provide all the configuration code to the TDC. The simulated TDC performance could ideally achieves better than 1ps resolution, but the effective measured time resolution performance are limited to 60ps in one nanoseconde depth. The circuit limitation are due to noise jitter accumulation, noise coupling from the power supply and the frequency noise of the ring oscillator’s itself. However, the proof of concept of this architecture is a success.
limitation of the architecture had been pinpointed and new design of similar improved architecture are under test.

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**Presenter:** Ms AMINA, ANNAGREBAH (Universite Claude Bernard-Lyon I (FR))

**Session Classification:** POSTER Session

**Track Classification:** ASIC
In the framework of the ALICE experiment upgrade at HL-LHC, the whole electronics of the existing Muon Tracking Chambers (MCH) will be refactored with a new frontend chip and the associated readout electronics. This paper presents the design of the dedicated concentration cards ‘SOLAR’ to ensure the readout of 30,000 frontend chips. Based on the CERN GBTx and FEAST DCDC chips, allowing to work in a radiation and magnetic field environment, each of the 650 SOLAR cards can broadcast configuration, trigger and synchronization signals and gather the data of up to 80 frontend chips through up to 6 meter cables.

Summary

In the frame of the upgrade of the LHC (Large Hadron Collider) at CERN, the existing ALICE (A Large Ion Collider Experiment) prepares a major upgrade of its experiment apparatus, planned for installation in the second long LHC shutdown (LS2) in the years 2019-2020. This will include the upgrade of the Muon Tracking Chambers (MCH), and especially the update of its electronics. This refactor involves the frontend replacement by a dedicated ASIC ‘Sampa’, along with an upgrade of the readout for all the 5 tracking stations. For compatibility with the existing detector and taking into account the detector occupancy, the ~ 30,000 Sampa chips involved are grouped by 2 on a ‘Dual-Sampa’ (DS) board. The configuration and the readout of all the Sampa chips is then ensured by ~ 650 concentration cards ‘SOLAR’, and connected optically to ALICE Common Readout Unit (CRU). Taking into account the radiation (TID < 1 krad, fluence < 4.1011 n 1 MeV equivalent) and magnetic field (0.7 T) environment, the design of the SOLAR concentration board is based on the GBTx (gigabit transceiver), the GBT-SCA (slow control companion chip), VTRX (versatile transceiver) and the FEASTMP (DC/DC converter) devices developed at CERN. With regard to the granularity of the elinks in the GBTx and the integration constraints, especially keep a generic design for SOLAR with the two types of MCH stations (quadrants and slats), each SOLAR board was designed to connect to up to 40 DS cards through up to 6 meter cables. In this design, DS cards are grouped by cluster of up to 5 cards, such that each Sampa ASIC can be configured individually, while the trigger and synchronization signals are shared by up to 10 Sampa chips. Downstream, the 2 Sampa chips on a DS board are daisy chained, each DS board having its dedicated 80 Mbit/s elink toward the SOLAR card. In addition to this, a chip with a unique ID was included onboard the SOLAR board to ensure board identification for traceability at the production step, but also for tracking the SOLAR boards along their life cycle in the MCH detector. With a power consumption below 3 W for a versatile power supply in the range 5 to 12 V, thanks to the FEASTMP DC/DC, first results with the first SOLAR prototype are very encouraging, even with 6 meter flat ribbon cables, allowing a full chain validation including the configuration and the readout of 5 DS cards, in a beam test at CERN. A new design, fitting into a standard 6U format crate, and a dedicated production test bench are developing for the end of 2017.
Primary authors: Dr. FLOUZAT, Christophe (CEA Centre de Saclay); PAUL, Bernard Joseph (CEA/IRFU, Centre d'étude de Saclay Gif-sur-Yvette (FR)); GRABAS, Aude Marie (CEA/IRFU, Centre d'étude de Saclay Gif-sur-Yvette (FR)); Mr. BESIN, Dominique (CEA)

Presenter: GRABAS, Aude Marie (CEA/IRFU, Centre d'étude de Saclay Gif-sur-Yvette (FR))

Session Classification: POSTER Session

Track Classification: Radiation Tolerant Components and Systems
A Data Acquisition System for the CLIC Vertex Detector Readout Chip.

Monday, 11 September 2017 17:20 (25 minutes)

The DAQ of the CLICpix2 readout chip is based on the Control And Readout Inner tracking BOard (CaRIBOu). CaRIBOu is a versatile readout system targeting a multitude of detector prototypes. It profits from the heterogeneous platform of the Zynq System-on-Chip and integrates in a monolithic device front-end FPGA resources with a back-end software running on a hard-core ARM-based processor. The user-friendly Linux terminal with the pre-installed DAQ software is combined with the efficiency and throughput of a system fully implemented in the FPGA fabric. We present the design of the system and show examples of the achieved functionality and performance.

Summary

The development of pixel detectors for future high-energy physics experiments requires flexible high-performance readout systems supporting a wide range of current and future device generations. The versatile readout system of the Control and Readout Inner tracking BOard (CaRIBOu) targets laboratory and high-rate test-beam measurements with a multitude of detector prototypes. Under the project umbrella, application-specific chipboards and a common interface card have been developed for a variety of pixel detector readout ASICs and active sensors. While currently supporting CLICpix2 and ATLAS FE-I4 hybrid pixel detector readout ASICs, it can be easily interfaced to other devices. The boards are hosted by a commercial evaluation kit (ZC706). This talk focuses on the data acquisition system (DAQ) based on a heterogeneous Xilinx Zynq All Programmable System-on-Chip (AP SoC). The device integrates the software programmability of an ARM-based processor with the hardware flexibility of an FPGA, enabling acceleration of the design, verification, test and commissioning processes. The CPU handles the slow control of the system, while the FPGA fabric performs data processing and data encapsulation in UDP datagrams moved by a Direct Memory Access (DMA) device through the High Performance Advanced Extensible Interface (AXI) port directly to the shared Random Access Memory (RAM). Further, data in RAM is accessed by the CPU for prompt analysis (data-quality monitoring, calibration, etc.) or is transferred eventually to a storage server over the 10 Gbps Ethernet link using a standard Linux network stack, the DMA and an offload engine implemented in the FPGA. Thanks to the fully capable dual-core processor running a Linux operating system, the DAQ board provides the unique user experience of a regular fully-functional remote terminal able to execute high level code (such as Python scripts). Moreover, as the code runs locally on the CPU integrated directly or indirectly (through the FPGA fabric) with the given ASIC, operations involving high input/output (I/O) activity (e.g. chip equalization) are not affected by network delays. The logic modules implemented in the FPGA fabric are available to the end user through the open source Linux device drivers maintained by the Xilinx community. In order to facilitate the creation of an embedded Linux distribution, CaRIBOu provides a layer to the Yocto build framework supported by a large community of open-source and industrial developers. The talk presents the design of the SoC-based DAQ system, its building blocks and shows examples of the achieved functionality and performance for the CLICpix2 readout ASIC and the C3PD active CMOS sensor.
Primary author:  FIERGOLSKI, Adrian (CERN)
Presenter:  FIERGOLSKI, Adrian (CERN)
Session Classification:  Systems, Planning, Installation, Commissioning and Running Experience
Track Classification:  Systems, Planning, Installation, Commissioning and Running Experience
A testbeam telescope, based on the ATLAS IBL silicon pixel modules, has been built to investigate the possibility of using the CMOS technology in the HL-LHC upgrade of ITk. The Front-End LInk eXchange (FELIX) system is a new approach to function as the gateway between different front-ends and the commodity switched network in the ATLAS upgrade. A FELIX based readout system has been developed for the testbeam telescope, including a FMC Telescope Readout Card for data transmission. The test results show that it is capable of high-density pixel sensor calibration and readout effectively, and being deployed in the testbeam experiments.

Summary

The ATLAS experiment is planning to build a new all-silicon Inner Tracker (ITk) for the High-Luminosity LHC (HL-LHC). The High Voltage CMOS (HV-CMOS) sensors are extensively investigated for multiple advantages compared to the traditional planar pixel detectors. The FE-I4 telescope has been built to test small HV-CMOS prototypes, which consists of six ATLAS Insertable B-Layer (IBL) double-chip (DC) pixel modules. The Front-End LInk eXchange (FELIX) is a system to interface the front-end electronics and trigger electronics for several detectors in the ATLAS Phase-I and HL-LHC upgrade. The PCIe based FELIX has been verified as a good option for HV-CMOS sensors readout. A new system is being developed for the readout of testbeam telescope sensors, with the goal to have the full testbeam readout upgraded to the FELIX system.

This FELIX based readout system includes a Xilinx ZC706, an interface FMC Telescope Readout Card and a FELIX in the back-end. The Xilinx ZC706 is the main FELIX interface in the front-end. It consists several firmware modules, including the FE-I4 interface module, the low-latency GBT-FPGA, and other control parts. The FE-I4 output data is a 160 Mbps 8b/10b encoded serial signal, which is de-serialized, aligned and decoded in the ZC706. Different data types from FE-I4 will also be extracted and buffered. There are two GBT links between ZC706 and FELIX: one is used to distribute the clock signal from FELIX to ZC706, and the other is for data transmission. The FELIX software is responsible for issuing all the control commands and continuously storing all the pixel data from the front-end for off-line analysis.

An interface board, FMC Telescope Readout Card, has been designed, which will be placed between IBL DC modules and the ZC706 board. This board is connected to the ZC706 through FMC connectors, with single external 12-V power supply. There are 12 RJ45 ports connecting to all the IBL DC modules in the testbeam telescope, and 4 SFP connectors for GBT links. A clock chip of Si5345 is implemented on board in order to improve the quality of recovered clock from the GBT link. This clock chip can be configured from FELIX through the GBT link. The hardware design of the FMC Telescope Readout Card has been verified, including the power rails, I2C bus, Si5345, SFP connectors, LVDS repeaters, etc.

The previous version of this FELIX based readout system has been used to readout Device Under Test (DUT) in the testbeam in August, 2016 at CERN. The configuration and tuning of both CCPD sensor and FE-I4 chip can be fulfilled with a good efficiency. During a more than 13-hours of data taking, the testbeam data can be streamed from the FE-I4 to the disk without any loss. With the new FMC Telescope Readout Card, the readout of telescope sensors will also be realized with FELIX system. It is planned to have the full testbeam readout upgraded to the FELIX system by summer 2017.
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Session Classification: POSTER Session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience
The Development of Front-End Readout Electronics for ProtoDUNE-SP LAr TPC

Tuesday, 12 September 2017 08:30 (25 minutes)

As a prototype of DUNE far detector, ProtoDUNE-SP single phase LAr TPC will sit in H4 beam line at CERN to study detector response to particles. It consists of 6 full-size APAs plus 2 CPAs, with total 15,360 TPC readout channels. The front-end readout electronics is comprised of cold electronics and warm interface electronics. The integral design concept of APA, cold electronics, feed-through, plus warm interface electronics with local diagnostic and strict isolation and grounding rules has been followed and studied at BNL. The production front-end readout electronics are being fabricated and will be installed in ProtoDUNE-SP in fall 2017.

Summary

ProtoDUNE-SP is a 700 ton single phase LAr TPC using full scale components of DUNE far detector module, will sit in H4 beam line at CERN and plans for operation in 2018. Its goals include measuring detector response to known particles, confirming modeling and simulation, and validating mechanical and electrical design and interface. It consists of 6 full-size APAs (Anode Plane Assembly) plus 2 CPAs (Cathode Plane Assembly), which get 2 x 3.6m drift regions and 15,360 TPC readout channels in total. In the DUNE experiment, the total equivalent noise charge (ENC) should be less than 1/9 of the expected worse case instantaneous charge arriving at the APA from a MIP, which requires the ENC for induction wires to be less than 650 electrons. This is enabled by the CMOS cold electronics installed in the cryostat and operating in LAr to achieve the optimal noise performance.

The ProtoDUNE-SP front-end readout electronics is comprised of cold electronics and warm interface electronics. Cold electronics is placed close to the wire electrodes inside the cryostat, which makes the noise independent of fiducial volume (signal cable lengths). It mainly consists of 960 FE ASICs, 960 ADC ASICs and 120 cold FPGAs to form 120 Front End Mother Board (FEMB) assemblies. Each FEMB assembly is made up of an analog mother board (AM) and a FPGA mezzanine (FM). An AM has 128 channels with 8 FE (front-end) ASICs and 8 ADC ASICs designed by BNL for 77K-300K operation and long lifetime with low power consumption. An FE ASIC has 16 channels of charge amplifier with programmable gain and filter time constant. An ADC ASIC has 16 channels of 12-bit ADC at 2MHz sampling rate. FM multiplexes and transmits 128 channels of data through four 1 Gb/s serial links to warm interface electronics. Warm interface electronics with local diagnostic is installed in the crate on the flange, which aggregates all the data with up to 10 Gb/s optical links to DAQ system.

Noise performance of FEMB with 150pF input capacitance has been characterized. ENC is about 1100 electrons at room temperature and about 550 electronics in liquid nitrogen. However, to have a chance to achieve a good performance with ProtoDUNE-SP detector, the integral design concept of APA, cold electronics, feed-through, warm interface electronics, plus strict isolation and grounding rules should be followed. An integration test stand with 40% APA has been built at BNL, which is used to test the full readout chain from APA to WIB at both room and liquid nitrogen temperatures. With proper ground scheme, ENC measurement at room temperature achieves 770 electrons with collection wires (2.8m) and 830 electrons with induction wires (4m), which is consistent with what we expected. We are performing the cold test from April through May, the...
detailed test results will be presented in the meeting. The production front-end readout electronics are being fabricated and will be installed in ProtoDUNE-SP in fall 2017. The experience of the production test of front-end electronics will be presented as well.

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**Session Classification:** Production, Testing and Reliability

**Track Classification:** Production, Testing and Reliability
MATISSE: a Low Power Front-End Electronics for MAPS Characterization

Tuesday, 12 September 2017 17:45 (15 minutes)

Monolithic Active Pixel Sensors are becoming increasingly attractive for the next generation High Energy Physics experiments. For this reason several R&D are ongoing in different laboratories to improve the performance of conventional MAPS.

In this context we present a flexible readout electronics specifically developed for the detailed characterization of MAPS. The prototype ASIC has been fabricated in 0.11 μm CMOS technology with a die area of 2 x 2 mm² and a low voltage operation of 1.2 V.

In the presentation, the front-end electronics will be described and detailed tests obtained on a first submission will be presented.

Summary

The next generation High Energy Physics experiments requires the development of novel radiation silicon sensor technologies adequate to cover large areas. In this context, Monolithic Active Pixel Sensors (MAPS) are becoming increasingly attractive thanks to their properties such as low material budget, high granularity and the much lower cost if compared with hybrid pixel sensors. Several R&D are ongoing in different laboratories to improve the characteristics of conventional MAPS. In particular, achieving a charge collection speed as fast as possible is key to improve the sensor radiation tolerance.

Technologies that allow simultaneous integration of analog and digital electronics in the same pixel are also increasingly exploited.

In the course of an R&D project it is important to compare different sensor designs and different starting materials. In this context we have developed a flexible readout electronics that allows the detailed characterization of MAPS. A prototype ASIC has been fabricated in 0.11 μm CMOS VLSI technology with a die area of 2 x 2 mm² and a low voltage operation of 1.2 V. The test chip consists of a matrix of 24 X 24 pixel units organized in 4 independent sectors and an End of Column logic. Each sector consist of 6 columns of 24 pixels and can be used to test different sensor flavors. Both NMOS and PMOS can be used simultaneously.

The analogue readout is based on a Charge Sensitive Amplifier (CSA) with a feedback transistor for the reset operation, two local memories implemented by using MIM capacitors to optimize the pixel size and four buffers used to send the analogue data off-chip through dedicated data transmission lines. The preamplifier is connected to the sensing node by DC coupling. The digital logic in-pixel allows some features like internal pulse generation, baseline regulation and mask channel operation. Thanks to the baseline regulation and to the wide dynamic range of the buffers, the readout supports signals in excess of 24 ke−. The use of a CSA makes the readout fairly insensitive to the sensor capacitance. An additional large digital buffer, controlled by a dedicated signal have been also implemented to inject substrate noise with the aim of studying the possible noise coupling between the digital and the analogue electronics. The four sub-matrices are readout in parallel in less than 40 us with a maximum measured drop voltage of 0.7 μV. when a clock of 5 MHz is used. For each sector both the baseline and signal are sent off-chip. The design supports snapshot shutter operation with integration times as short as 100 ns and Correlated Double Sampling (CDS) to subtract offsets in common between baseline and signal and to suppress the switching noise. In the present implementation the in-pixel electronics occupies an area of 30 μm X 30 μm and, including the sensor, it allows the implementation of pixels with a total are of 40 μm X 40 μm or larger.
In the presentation, the front-end electronics will be described and detailed tests obtained on a first submission will be presented.

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**Presenter:** Mr OLAVE, Elias Jonhatan (INFN di Torino e Politecnico di Torino)

**Session Classification:** POSTER Session

**Track Classification:** ASIC
A Multi-Channel PCI Express Readout Board Proposal for the Pixel Upgrade at LHC

Tuesday, 12 September 2017 17:45 (15 minutes)

After having commissioned the readout electronics currently implemented in the Insertable B-Layer, Layer 1 and Layer 2 of the ATLAS Pixel Detector (B-Layer and Disk readout electronics in under commissioning), we have designed and fabricated a new readout electronic board looking at the upgrade of the LHC pixel detectors. A couple of PCI_express-based prototype boards, namely PCI-ROD featuring all the minimal I/Os and interfaces to address the future front-end electronics, have already been fabricated and tested. The GBTx and RD53A are the first chips that we are going to interface with: preliminary tests are here presented.

Summary

Over the last years the ATLAS Pixel Detector has been upgraded in terms of sensors and readout electronics. The sensors, the back-of-crate and readout-driver cards have been upgraded for the Insertable B-Layer, while the Layers 1 and 2 have maintained the current sensors and have updated only the readout electronics to stand the on-going increment of luminosity of the collider at CERN. All these layers have already taken data while the readout electronics upgrade for the B-Layer and Disks is under commissioning and it will be completed in the technical stop of 2018. To continue the challenge of upgrading the readout electronics for the LHC pixel detectors we have designed and fabricated a PCI_express 8-channel board (PCI-ROD) with all the necessary I/Os looking at the performance to interface with the current and future front end electronics chains. For example, the intention is to interface with the GBTx and RD53A chips.

In particular the GBTx communication has already been tested via an optical transceiver at a speed of 10 Gb/s in a loopback configuration. In addition, a board designed for the ALICE time-of-flight experiment, mounting a GBTx ASIC, has been physically interfaced with the PCI-ROD through an optical fiber at a speed of 4.8 GB/s.

As far as the RD53A chip interface, we are building a demonstrator tool able to emulate a data-taking of physical streams, using the Aurora protocol, by connecting two PCI-ROD boards. One is used to build the expected RD53A emulated data and the other one is the receiver. This can be run at data rates up to 10 Gb/s on a single channel or in parallel over several links.

The PCI-ROD board features two Xilinx FPGAs: the Kintex7 XC7K325T-2FFG900C and the Zynq XC7Z020-1CLG484C with an embedded physical dual-core ARM Cortex-A9 processor. The Kintex device allows 16 transceivers nominally running at up to 12 Gs/s. These 16 GTx are connected to different types of physical ports: 8 PCI_express, 4 HPC FMC, 1 LPC HMC, 1 SMA, 1 SFP and 1 Gb-Ethernet port. So far we have proved the coaxial link to the SMA, the optical channel to the SFP and the Ethernet links up to 10 Gb/s.

In addition the two Xilinx devices feature DDR3 external memories tested with read-write cycles at 667 MHz.

The PCI-ROD board can be equipped with a firmware derived from the one that is currently working into the BOC and ROD boards of the ATLAS Pixel Detector.

As the PCI-ROD features 16 GTx channels we are proposing the board as a tool to test, qualify and read out the recent chips and/or channels under development to interface the new generation of the Pixel Detectors at LHC. We start working within the ATLAS ITK italian collaboration to help qualifying some the RD53A modules expected by this year. We are also planning extend the use of the board within other CERN-based collaborations.
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Session Classification: POSTER Session

Track Classification: Production, Testing and Reliability
Commissioning of ROD Boards for the Entire ATLAS Pixel Detector

Wednesday, 13 September 2017 17:45 (15 minutes)

ATLAS Experiment has reworked and upgraded some systems during the 2014-2016 LHC shut down and the Pixel Detector has inserted an additional layer: the Insertable B-Layer. The layers 1 and 2 have been also upgraded, using the same BOC and ROD cards designed for IBL, while maintaining the detector unchanged. Now the efforts focus on the upgrade of the B-Layer and the Disks, again leaving the sensors untouched. Time plan is to commission the DAQ installation by the technical stop in 2018 while IBL, Layers 1 and 2 are working and able to take data using the new readout system.

Summary

The strategy for Insertable B-Layer (IBL) Readout-Driver (ROD) firmware development was three-fold: keeping as much of the Pixel ROD datapath firmware logic as possible, employing a complete new scheme of steering and calibration firmware and designing the overall system to prepare for a unified code version integrating IBL and Pixel layers. Essential features such as data formatting, frontend-specific error handling, and calibration are added to the ROD data path.

Along the recent years, after the ATLAS Pixel Detector IBL upgrade (14 ROD boards plus 1 for the Diamond Beam Monitor), also the Layer 2 and 1, which requires 26 plus 38 additional pairs of Back-of-Crate (BOC) and ROD cards, have been upgraded. For these two layers, in contrast with IBL, only the BOC and ROD readout chain has been updated while the sensors have been left unchanged. In fact, the boards originally designed for IBL can easily expand also the bandwidth of Pixel Layer 2 and 1 as long as we provide dedicated firmware to interface with the present detector and, in particular, with the FEI3 chips instead of the IBL FEI4 ASICs. The same approach used for upgrading the Layer 2 and 1 will be used to upgrade the BOC and ROD cards used in the Pixel Detector B-Layer and Disks. The B-Layer and Disks will be read out with the same firmware in use for the Layer 1, sharing the same modularity and clock speed. The additional production of 51 RODs, including the spares, has already been completed and the tests are on going. The plan is to have the readout upgrade of B-Layer and Disks commissioned by the technical stop in 2018. Thus, eventually, the entire Pixel Detector of ATLAS will share the same hardware readout chain, configured differently with specific firmware depending on the front-end sensors and modularity.

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Session Classification: POSTER Session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experi-
ence
Simulations of Busy Probabilities in the ALPIDE Chip and the Upgraded ALICE ITS Detector

Wednesday, 13 September 2017 17:45 (15 minutes)

For the LS2 upgrade of the ITS detector in the ALICE experiment at the LHC, a novel pixel detector chip, the ALPIDE chip, has been developed. In the event of busy ALPIDE chips in the ITS detector, the readout electronics may need to take appropriate action to minimize loss of data. A lightweight, statistical simulation model for the ALPIDE/ITS has been designed using the SystemC framework.

With the simulations we have been able to quantify the probability of busy situations under various conditions, which is crucial knowledge for the further design and development of the readout electronics.

Summary

For the upgrade of the Inner Tracking System (ITS) in the ALICE experiment at the LHC, a novel pixel detector chip called ALPIDE has been developed. The upgraded ITS will consist of over 24,000 ALPIDE chips spread out over 192 detector staves in 7 layers. Each stave is connected to its own Readout Unit (RU), and 8 RUs are connected to a dedicated Common Readout Unit (CRU). The readout electronics is currently under development, and investigations are ongoing to decide if a dedicated system for monitoring and handling busy situations in the ALPIDE chips is required.

Due to the random and unpredictable nature of the collisions at LHC, there will be situations where some of the ALPIDE chips will have their Multi Event Buffer (MEB) slices filled faster than the events can be read out. In this situation, the chips will send busy messages so that the RUs can take appropriate measures. Reducing the trigger rate may be one such measure. Forwarding the information to components later in the chain so that the busy decision is taken on larger parts of the detector may be another.

It will be crucial to have a busy monitoring system. If this system should also take active actions is not clear yet, and this can only be decided once the probability of busy chips is known with a high statistical certainty. None of the existing simulation models have been suitable for this task, as they were either extremely accurate, and comparably slow; did not scale for the whole detector; or they did not model the right parts of the ALPIDE chip required for these simulations. Additionally, no simulation has so far been done of the whole readout chain, including ALPIDE, RU and potentially the CRU.

A simplified simulation model of the ALPIDE has been developed using the SystemC framework. In this simulation model a purely statistical approach to event generation has been used. The events are created with random inter-event times, event multiplicities, and hit coordinates, all following well known statistical distributions that are representable for an LHC experiment. Only the necessary parts of logic in the ALPIDE chip were implemented, using a high level of abstraction in order to reduce simulation time.

The simulation model can easily be adapted for a variety of detector configurations, and currently a model of the RU is being included into the model. The simulations so far have proven to be in line with the expected results from earlier simulations (readout efficiency of up to 99.86% in 100kHz Pb-Pb, triggered mode).
Other possible applications of the simulation model include being used as an accurate ALPIDE data generator. This is useful for RU design or input to other simulations. Additionally, other research projects will be using the ALPIDE chip, to which the simulation model can easily be adapted.

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**Session Classification:** POSTER Session

**Track Classification:** Trigger
First full size 2S module prototypes for the CMS Phase-2 Tracker Upgrade have been assembled. With two sensors with realistic geometries and 16 CBC2 readout chips on two front-end hybrids, the characteristics of these complex objects can be studied. A microTCA based readout system was developed to test multiple front-end hybrids simultaneously. Therefore the concurrent information of the full module can be used for differential and common-mode noise characterization, as well as for signal tests with radioactive sources or cosmic particles. This talk will discuss the readout system and test results obtained with the first full size 2S module prototypes.

Summary

To prepare the CMS experiment for the High Luminosity LHC and its planned instantaneous luminosity of up to $7.5 	imes 10^{34}$ cm$^{-2}$s$^{-1}$ the CMS Silicon Tracker will be replaced in the Long Shutdown 3.

A new tracker will be constructed using about 13000 conceptually new modules: Two vertically spaced silicon micro-strip sensors are integrated into a single module and read out by the same front-end chip. The displacement of the hits between both sensors - caused by the bending of charged particle tracks within the 3.8 T magnetic field - can be used to infer a lower bound on the transverse momentum of the track in the modules themselves. Therefore all hits from high transverse momentum tracks can fit in the available bandwidth between module and back-end, where they are used in the first trigger stage of CMS.

First full size module prototypes for the outer radii of the CMS Tracker have been assembled. These so-called 2S modules feature two identical stacked 10x10 cm$^2$ micro-strip sensors, each with two rows of 1016 strips. The strip length amounts to 5 cm. One row of each sensor is connected to the same front-end hybrid. This allows to process the hit information from one track – hitting both sensors – in one of the eight CMS Binary Chips (CBC2) of each front-end hybrid.

A microTCA based readout system has been used to test these prototypes, since for the first time it is required to read multiple front-end hybrids simultaneously. Multiple GLIB AMCs are connected to the front-end while the fast control signals (clock, reset, trigger) are distributed within the back-plane of a commercial microTCA crate. The readout data is streamed via the IPBUS protocol through the Ethernet fabric in the back-plane as well.

With this system the two front-end hybrids of one module can be operated synchronously and the concurrent hit data of all 4064 channels is available. It allows to study single channel (differential mode) and coherent noise (common mode) in these complex objects. In this context also the susceptibility of the modules to perturbations on low voltage supply rails and electromagnetic emissions are investigated, since each module will be powered by a DC-DC converter pair, placed on the service hybrid in the direct vicinity of the sensors and the front-end hybrids (below 1mm distance).

Readout chip internal test pulses are used for functional tests and charge calibration, which is then cross-checked with X-rays. Beta sources and cosmic muons provide signals with realistic...
pulse heights within the sensors. They are used to access quantities which are defined by the sensor like cluster width and signal height. Due to the binary readout scheme the later one is only measurable on a statistical basis as an integrated charge spectrum. Combining these with the noise measurements, first conclusions on the signal-to-noise characteristics of the 2S prototypes on the scale of a full module can be drawn.

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**Session Classification:** Production, Testing and Reliability

**Track Classification:** Production, Testing and Reliability
Upgrade of the ATLAS Monitored Drift Tube Frontend Electronics for the HL-LHC

Wednesday, 13 September 2017 17:45 (15 minutes)

To cope with large amount of data and high event rate expected from the planned High-Luminosity LHC (HL-LHC) upgrade, the ATLAS monitored drift tube (MDT) readout electronics will be replaced. In addition, the MDT detector will be used at the first-level trigger to improve the muon transverse momentum resolution and reduce the trigger rate. A new trigger and readout system has been proposed. Prototypes for two frontend ASICs and a data transmission board have been tested, and simulation of the latency has been performed. We will present the overall design and focus on latest results obtained for the two ASICs.

Summary

The ATLAS monitored drift tube (MDT) chambers are the main component of the precision tracking system in the ATLAS muon spectrometer. The MDT system is capable of measuring the sagitta of muon tracks to an accuracy of 60 μm, which corresponds to a momentum accuracy of about 10% at pT=1 TeV. To cope with large amount of data and high event rate expected from the High-Luminosity LHC (HL-LHC) upgrade, ATLAS plans to use the MDT detector at the first-trigger level to improve the muon transverse momentum resolution and reduce the trigger rate. The new MDT trigger and readout system will have an output event rate of 1 MHz and a latency of 6 us at the first-level trigger.

The signals from MDT tubes are first processed by an Amplifier/Shaper/Discriminator (ASD) ASIC, and the binary differential signals output by the ASDs are then router to the Time-to-Digital Converter (TDC) ASIC, where the arrival times of leading and trailing edges are digitized in a time bin of 0.78 ns which leads to an RMS timing error of 0.25 ns. The pulse height is encoded as the time interval between the leading and trailing edges of the ASD output pulse. A local processor, Chamber Service Module (CSM), routes all hit signals from up to 432 tubes through optical fibers to the trigger processors located in the ATLAS movable counting house. The trigger processor will extract MDT tube hits corresponding to the right bunch crossing ID, perform segment-finding and track fitting algorithms on these selected hits and determine the muon transverse momentum at the first-level trigger. A system based on Front End Link Interface eXchange (FELIX) will be used to provide time, trigger and control signals and also for readout.

Detailed simulation have been performed for the whole trigger data flow chain to make sure it satisfy the first-level trigger latency requirement. First prototypes for ASD, TDC and CSM have been designed and tested. Integration tests with various prototypes have been performed with test beams at CERN. We will present latest results for these prototype ASICs and boards.

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Presenter: HU, Xueye (Umich)

Session Classification: POSTER Session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experi-
Development of Trigger and Readout Electronics for the ATLAS New Small Wheel Detector Upgrade

Monday, 11 September 2017 16:30 (25 minutes)

The present small wheel muon detector at ATLAS will be replaced with a New Small Wheel (NSW) detector to handle the expected rate at the increase in data rates and harsh radiation environment expected at the LHC. Resistive Micromegas and small-strip Thin Gap Chambers will be used to provide both trigger and tracking primitives. A new trigger and readout system is developed for the NSW detector. The new system has about 2.4 million trigger and readout channels and about 8,000 frontend boards. We will discuss the overall electronics design and studies with various ASIC and board prototypes.

Summary

The planned Phase-I and Phase-II upgrades of the LHC accelerator drastically impacts the ATLAS trigger and trigger rates. A replacement of the ATLAS innermost endcap muon station with a new small wheel (NSW) detector is planned for the second long shutdown period of 2019 - 2020. This upgrade will allow us to maintain a low pT threshold for single muon and excellent tracking capability even after the High-Luminosity LHC upgrade.

The NSW detector will feature two new detector technologies, Resistive Micromegas and small-strip Thin Gap Chambers. Both detector technologies will provide trigger and tracking primitives. The total number of trigger and readout channels is about 2.4 millions, and the overall power consumption is expected to be about 75 kW. The electronics design will be implemented in some 8000 front-end boards including the design of four custom front-end ASICs capable to drive trigger and tracking primitives with high speed sterilizers to drive trigger candidates to the backend trigger processor system. Tasks such as time, trigger and control signal distribution and readout are performed by the GBTx (Gigabit transceiver) ASIC, Slow Control ASIC, and an Front End Link Interface eXchange (FELIX) system. The large number of input channels, short time available to prepare and transmit data, harsh radiation environment, and low power consumption all impose great challenges on the design. The overall design as well as studies with ASIC and board prototypes will be presented.

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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience
Design and Results from a Front-End Board for Micromegas Chambers in the ATLAS New Small Wheel

Monday, 11 September 2017 17:45 (25 minutes)

The design and implementation of demonstrator front-end electronics for Micromegas detectors to be employed in the New Small Wheel, an ATLAS muon spectrometer upgrade, are presented. The demonstrator has 512 Micromegas detector channels as input. Signal processing and digitization utilize a custom ASIC developed by Brookhaven National Lab. Configuration, control and Ethernet readout functions are performed using an Artix-7 FPGA. Design constraints and considerations are discussed. Measurements of noise performance, both off- and on-detector, are presented. Results using an Fe-55 source are also shown. Design considerations for the final front-end electronics to be used in the ATLAS experiment are discussed.

Summary

The design and implementation of demonstrator front-end electronics for Micromegas detectors to be employed in the New Small Wheel (NSW), an ATLAS muon spectrometer upgrade, are presented. In order to improve the performance of the ATLAS end-cap muon system in response to ever-increasing luminosity of the Large Hadron Collider (LHC), the Level-1 trigger capability must be augmented. Adding hit information from the innermost layer of the end-cap muon system will significantly reduce the Level-1 trigger rate associated with combinatoric sources. Small-strip Thin Gap Chambers (sTGC) and Micromegas detectors (MM) will comprise the ATLAS New Small Wheel and provide improved triggering and reconstruction capability.

The MM detectors are constructed using a resistive strip design. The strip pitch for the MM front-end board is 400 um and the NSW system (both end-caps) consists of approximately 2 million strips. The front-end board has inputs for 512 MM channels, hence 4096 front-end boards are required for NSW system. The electrical connections between the front-end board and MM detectors are two elastomeric connectors. The connectors are made of silicon rubber with six rows of gold plated contacts spaced with 50 um pitch. G10 holders are used to hold the two connectors for each front-end board. A compression system that is part of the MM system bar provides the necessary clamping force. Input protection on the front-end board consists of a set of TVS diodes.

Signal processing and digitization utilize a custom ASIC, called the “VMM”, developed by Brookhaven National Lab. Each VMM ASIC has 64 channels. Each channel contains an amplifier with adjustable gain and shaper. Signals passing a sub-hysteresis discriminator have their peak amplitude and times digitized by 10-bit and 8-bit ADC’s respectively. The discriminated signal also provides an address-in-real-time that can be as part of the MM trigger. Digitized data are buffered and subsequently readout using a two-bit serial output. There are eight such VMM ASIC’s on the front-end board.

This demonstrator version of the front-end board utilizes an Artix-7 FPGA for configuration, control and Ethernet readout functions. MicroBlaze is used to communicate with the on-board Ethernet PHY. The final version of the front-end board will utilize two custom ASIC’s for the configuration and control functionality. The demonstrator version also makes use of commercial DC-DC converters and low dropout regulators for power. The final version will utilize a radiation tolerant DC-DC converter developed by CERN.
Noise measurements are made using an oscilloscope connected to a monitor output for the analog signals from the VMM ASIC’s. These measurements are cross-checked by a similar set of measurements using the XADC functionality of the FPGA. Data are also collected and analyzed using a small test MM chamber with 256 readout channels. Using an Fe-55 source, a clear photopeak and Argon escape peak are observed and the energy resolution for this MM detector is approximately 12%.

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**Presenter:** SCOTT, Garrett Joseph (University of Arizona (US))

**Session Classification:** Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Simulation of the ATLAS New Small Wheel Trigger System

Wednesday, 13 September 2017 17:45 (15 minutes)

The instantaneous luminosity of the LHC at CERN will be increased up to a factor of seven with respect to the original design value to explore higher energy scale. The first station of the ATLAS muon end-cap Small Wheel system need to replaced by a New Small Wheel (NSW) detector. The NSW provide precise track segment information to the muon Level-1 trigger to reduce fake triggers. This contribution will summarize a detail simulation of the NSW trigger decision system, track reconstruction algorithm implemented into the trigger processor and results of performance studies on the trigger system.

Summary

The instantaneous luminosity of the LHC will be increased up to a factor of seven with respect to the present design value by undergoing an extensive upgrade program over the coming decade. In order to benefit from the expected high luminosity performance, the first station of the ATLAS muon end-cap Small Wheel system will need to be replaced by a New Small Wheel (NSW) detector, which is used for trigger and precision measurement. The NSW provides precise track segment information to the muon Level-1 trigger to reduce fake triggers arising from particles that are not high pT muons originating from the Interaction Point (IP). The NSW consists of Micromegas (MM) and small-strip Thin Gap Chambers (sTGC). Both systems find a track segment independently and provide a two-dimensional position, (eta, phi), as well as the angle deviation delta theta of the NSW track-segment with respect to an infinite momentum track from IP. Eventually, a coincidence by (eta, phi) between the NSW and outer muon system is required to suppress the fake trigger rate.

A detailed study of the final design and validation of the readout electronics for the trigger system that are able to work at high rates with excellent real-time spatial resolution has been performed. A dedicated parametric digitization model based on the exhaustive standalone MC studies and experimental test beam results has been developed to simulate the response of the NSW trigger system. This contribution will summarize a detail simulation of the NSW trigger decision system, track reconstruction algorithm implemented into the trigger processor and results of performance studies of the DAQ trigger logic.

The NSW simulation has been developed to model the actual response of the detector and its fast electronics. The simulation has been used to get a deep understanding of the trigger logic timing, the tracking-segment finding efficiency, track rate and track-pointing resolutions at the high background hit rate expected during the next phases of operation of ATLAS at the LHC. The results of these performance studies will be presented to show that the NSW trigger system is capable of working with good performance compared to the foreseen requirements.

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Session Classification: POSTER Session
**Track Classification:**  Systems, Planning, Installation, Commissioning and Running Experience
Upgrade of the ATLAS Thin Gap Chamber Electronics for HL-LHC

Tuesday, 12 September 2017 11:55 (25 minutes)

The High-Luminosity LHC (HL-LHC) is planned to start the operation in 2026 with an instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. To cope with the event rate higher than that of LHC, the trigger and readout electronics of ATLAS Thin Gap Chamber will be replaced and an advanced muon trigger with fast tracking will be implemented. A frontend board prototype was developed and the functions for HL-LHC including the data transfer of 256 channels with a 16 Gbps bandwidth have been demonstrated. A study on the fast tracking shows the rate reduction for a first-level single muon trigger by 30%.

Summary

The High-Luminosity LHC (HL-LHC) is planned to start the operation in 2026 with an instantaneous luminosity of $7.5 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$. To cope with the event rate higher than that of LHC, the trigger and readout system of ATLAS will be upgraded based on the first-level trigger with a higher rate of 1 MHz and a longer latency of 6 us. The change in the trigger and readout system requires the replacement of the electronics for the Thin Gap Chamber (TGC), which plays a primary role for the first-level muon trigger in the endcap regions. The new design assumes the transfer of all hit data from the frontend to the backend boards, where only selected data are transferred in the current system. The current coincidence-based trigger will be upgraded by a tracking-based trigger to improve the transverse momentum resolution at the first-level trigger.

We have developed the first prototype frontend board of the TGC for the HL-LHC, which has a transceiver to send all hit data of 256 channels with a 16 Gbps bandwidth based on the optical transceivers. The data transfer was tested with pseudorandom numbers, and the bit error rate was less than $8.9 \times 10^{-15}$. The prototype includes the controller of the threshold voltage for the discriminator, which is also essential for the TGC frontend board. Linear relation between the set and the measured voltages was obtained in a range from -300 mV to 300 mV, which covers the operation range of the current system (from -250 mV to 250 mV). The prototype has been mounted on the spare TGCs for ATLAS, and the data transfer has been demonstrated with the charged particle beam at the CERN SPS beam facility. The single-hit efficiency in the bulk region of the chamber was obtained to be ~99%, which indicates that the data transfer works without serious problems. The investigation of the radiation tolerance for the elements on the prototype, e.g. FPGA, is the next major step.

R&D is also ongoing for the backend board. Segment reconstruction with a software-based minimum chi-square method showed a potential of the TGC to provide the segment angle resolution of 3.5 mrad. As a result, the rate for a single muon trigger with a transverse momentum threshold of 15 GeV may be reduced by 30%. The algorithm of the segment reconstruction for the implementation in the hardware, e.g. pattern matching, is under study.

In summary, the trigger and readout electronics of ATLAS Thin Gap Chamber will need to be replaced to cope with the higher event rate at HL-LHC. First prototype of the frontend board was developed with the functions required for HL-LHC including the data transfer of 256 channels with a 16 Gbps bandwidth, and the functions have been demonstrated with charged particle beam at the CERN SPS beam facility. An initial study on the first-level trigger with fast tracking shows the rate reduction for a single muon trigger with a transverse momentum threshold of 15 GeV by 30%.
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**Session Classification:**  Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:**  Systems, Planning, Installation, Commissioning and Running Experience
A 2.5V Step-Down DC-DC Converter for Two-Stages Power Distribution Systems

A prototype second-stage buck DC-DC converter has been designed in 130nm CMOS and fully characterized. This circuit provides up to 3A at an adjustable output voltage of 0.6-1.5V from an intermediate bus voltage of 2.5V. Hardness by design techniques have been systematically used, and the prototype successfully passed TID irradiation up to more than 200Mrad and Single Event Effects tests with a heavy ion beam. Safe integration on-board requires an optimized PCB design and bump-bonding assembly to reduce parasitic inductances along the input current path. An alternative quasi-resonant topology enabling significant reduction of the inductor size is also described.

Summary

Some detector systems for upgraded LHC experiments require the distribution of different voltage supply levels on the same compact module. The use of two-stages step-down conversion is a convenient and efficient way of doing that. The first conversion stage provides a regulated intermediate bus voltage of 2.5V that can be used on module to power opto-electronics components. This converter, powered via a single 12V line by off-detector supplies, is a modified version of an already qualified circuit (upFEAST2) widely used in LHC detector upgrades. In this work we present the development of a second-stage Point-Of-Load (POL) converter, radiation and magnetic field tolerant, and providing up to 3A at 0.6-1.5V to the load from the intermediate bus voltage. The first prototype converter circuit for this application uses a simple buck topology and has been designed in the mainstream 130nm CMOS technology supported within the CERN Foundry Services. The I/O 2.5V transistors available in this technology have been used in the design of the power portion of the circuit, while all the control benefits from the better performance and radiation tolerance of the core 130nm transistors. One of the main difficulties to overcome originates from the large switching input currents inherent to the functionality of a buck converter: parasitic inductances along the input current path generate large voltage transients at high frequency that challenge the reliability of the device. This has been addressed in the design with reduced slew rates in the commutation of the power transistors. In an effort to reduce the parasitic inductance the circuit is bump-bonded to a PCB whose design has been optimized with the help of ANSYS SIwave, a specialized design platform for power integrity. On-chip voltage transients have been measured on the prototype with a dedicated on-chip track-and-hold circuit, and agree with expectations.

Total Ionizing Dose (TID) tolerance has been achieved with the systematic use of Enclosed Layout Transistors (ELT) and guardrings, and relying on the natural radiation tolerance of the thin gate oxides. Provisions to protect the circuit from Single Event Effects (SEE) include over-sized logic gates, triplication, and the use of a novel Pulse-Width-Modulation generator circuit capable of fast recovery from a possible particle hit. These built-in properties have been confirmed with irradiation at an X-ray system up to more than 200Mrad (TID) and at a heavy ion accelerator (SEEs). The first prototype converter switches at frequencies between 4 and 8MHz using inductors of 47 to 100 nH. Its efficiency, strongly determined by the working conditions, is in the range of 85-89% for an output voltage of 1.2V and 81-86% for 1V. Full electrical characterization shows that most of the...
integrated functions perform correctly, while highlights some issues that are addressed in a second prototype that will be manufactured over the summer. We are also developing an alternative design based on a quasi-resonant topology that promises to yield higher efficiency while drastically reducing the inductor size to 10-20nH, allowing for a considerable mass and size reduction very attractive for tracker detectors.

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**Session Classification:** Power, Grounding and Shielding

**Track Classification:** Power, Grounding and Shielding
The ATLAS ITk is working to deliver a new Inner Tracking detector for use at HL-LHC. The strip tracker community has recently constructed partially loaded, double sided demonstrator staves using the HCC / ABC130 chipset in 130nm CMOS technology. Mindful of the need to maximise power efficiency whilst minimising the cost and material of associated cable plant, the system design includes the integration of a low-mass DC-DC converter and sensor bias (HV) switch within each module. This paper documents the first results from the demonstrator staves. The system concept and the roadmap toward a full system test are also outlined.

Summary

The ATLAS ITk is working to deliver a new Inner Tracking detector for use at HL-LHC. The strip tracker, comprising a series of concentric barrels with endcaps formed of petals, applies a common system architecture to the two geometrically different regions. Each stave or petal comprises a support structure made of carbon fibre and foam, into which a cooling pipe has been integrated. Polyimide flex circuits known as "bus tapes" are co-cured upon them to route electrical services between the End of Substructure (EoS) card, which provides the interface to the off-detector systems, and the detector modules. In order to maximise power efficiency and to minimise the cost and material of associated cable plant, each stave or petal side has a common low voltage power bus at 11V. As such, low mass DC-DC converters form an integral part of the strip module design: these are used to deliver the 1.5V needed to power the front end chipset. The detailed module design and standalone performance is presented elsewhere in this conference. This year our community has constructed partially loaded, double sided demonstrator staves using the HCC / ABC130 chipset in 130nm CMOS technology. The system architecture of these staves differs slightly from that proposed for production units with the ABCstar/ HCCstar chipset in the same technology, but is sufficiently representative so as to make this an important test. Key differences include the use of EoS cards which connect to the DAQ hardware by means of parallel electrical links provide a buffered, parallel connection instead of the lpGBT chips to be used in the experiment, and the use of early bus tape designs with a common multi-drop bus to supply Trigger, Timing and Control (TTC) signals to the 13 short strip modules on each side. Signal propagation tests with these tapes had noted a marked deterioration of TTC quality when more than 4 modules are loaded, so these early demonstrators shall not be fully loaded. The design was shown to work very well and results shall be presented.

The next generation of staves will use segmented TTC links to deliver high quality signals to 14 modules, hence they may be fully loaded, and their EoS cards will use the GBTx chip in order to facilitate optical readout of the modules. The way forward to a system test using such staves shall be outlined.
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Presenter: PHILLIPS, Peter (STFC - Rutherford Appleton Lab. (GB))

Session Classification: Production, Testing and Reliability

Track Classification: Production, Testing and Reliability
Radiation Hardness Studies and Evaluation on SRAM-Based FPGA for High Energy Physics Experiments

Monday, 11 September 2017 14:50 (25 minutes)

Being a proposed solution for the digital boards of the upgraded LHCb RICH sub-detectors, SRAM-based FPGA devices have become widely used in high energy physics experiments. These studies aim to present the radiation hardness measurements done on the KINTEX-7 FPGA during irradiation with protons, X-rays and ions beams. For multiple values of the total ionising dose, linear energy transfer and proton energy, the cross sections of single-event-effects are estimated. We also give separate results for specific resources type: configuration RAM, block RAM, I/O banks and logic. Conclusions are reached on the radiation tolerance of this chip family in LHC environment.

Summary

The KINTEX-7 FPGA, considered the mid-range class of the 7 Series from Xilinx, is a commercial 28 nm high-K metal gate SRAM-based device which was proposed to be included in the design of the digital boards of the upgraded LHCb RICH detectors because of its price-performance ratio. An irradiation campaign was organized to test and qualify this FPGA for the radiation environment expected at 50 fb-1 integrated LHC luminosity. The test campaign includes irradiation sessions with: high penetration and high stopping power ion beams at the Legnaro National Laboratories in Italy and at the Cyclotron Resource Centre in Louvain Belgium; proton beams with different energies at the Paul Scherrer Institute from Switzerland and at the Nuclear Physics Institute in Jülich Germany; and an X-ray test at a facility from the University of Padova.

A custom test bench along with a DAQ system was specially designed for this kind of tests allowing us to run the FPGA in JTAG mode without any additional components like external configuration memory in order to have a realistic minimal setup which decreases the probability that the test board and monitoring system ensemble fails under radiation. Since the FPGA is designed using flip-chip technology and in order to allow the heavier ions to penetrate the dice to the bottom active layer the wafer was thinned from 250 to about 60 µm. During irradiation, the electrical parameters of the FPGA, voltages and currents, were monitored and saved for later analyses along with the CRAM mitigation report provided by the Soft Error Mitigation IP Core.

With ion beams providing Linear Energy Transfer (LET) values ranging from 1.3 to 32.4 MeV·cm²/mg the FPGA was tested for single-event effects, especially the single-event latch-ups and single-event upsets, hence the calculated cross sections for both effects will be provided. With several dedicated firmwares calling specific resources like configuration RAM, block RAM, flip-flops chains, I/O banks, we have measured individually each corresponding cross-section.

Using 35 MeV and 200 MeV protons the FPGA was tested to get a maximum tolerance value for total ionizing dose and displacement damage. For single-event-effects, dedicated firmware was used to test logic with flip-flop chains, configuration RAM, block RAM and I/O blocks. The results of the device testing and its electrical characteristics during and after irradiation will be provided in this talk. A special attention was given to the I/O block ring oscillators which were tested, and I/O bank reliability will be discussed.

The X-ray tests helped us to confirm and tag the effects seen during proton tests, with most of
them dependent on the total ionizing dose only.

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**Session Classification:** Radiation Tolerant Components and Systems

**Track Classification:** Radiation Tolerant Components and Systems
An 8-Channel ASD in 130 nm CMOS with Superior Performance of Rise Time, Noise and Threshold Uniformity for ATLAS Drift Tube Readout at the HL-LHC

Monday, 11 September 2017 17:45 (25 minutes)

ATLAS Muon-Drift-Tubes spatial resolution- &- efficiency depend on drift-time resolution, noise levels, and accurate threshold setting. A new 130nm read-out device is developed and optimized, for the required time resolution, to guarantee rise-times below 10ns, with acceptable time-slewing effects. Moreover, the large chain-amplification results in increased sensitivity to any disturbance (mainly from supply). To avoid additional costs to clean up the set-up from such disturbs, the read-out chain adopts innovative techniques (at system, circuit, and design levels) minimizing read-out chain disturb sensitivity. This paper details the design strategy, compares post-layout simulation with measurements and presents resolution studies in CERN high-energy testbeam.

Summary

ATLAS MDT of HL-LHC (High-Luminosity Large-Hadron-Collider) interface with 8xASD (Amplifier-Shaper-Discriminator) ASIC. The new electronics in IBM 130nm CMOS 8RF-DM technology must be able to detect charged particles in 5fC – 100fC range with <15ns rising time in challenging operative conditions. These arise out peak luminosity increment of a factor 5 – 7.5 beyond the nominal value of 1034 cm-2 s-1.

The 8xASD includes eight channels designed to comply with rising time, signal-to-noise and threshold uniformity specifications. Each channel includes an input stage (a Charge Sensitive Preamplifier, CSPreamp) able to convert the input charge signal into a voltage one. This analog signal provides information about charge arrival time and charge amount. The 8xASD can also operate in ToT (Time-over-Threshold) mode.

This paper presents the second ASD ASIC prototype for ATLAS MDT (the first ASIC was presented in [1]. It occupies an area of 7.64mm2 performing about 14mV/fC of sensitivity and 12ns of rising time at discriminator input with 10mA/channel current consumption and 3.3V supply voltage. The first front-end element of previous ASD chain[1] is the CSPreamp. It is built-up by a single-ended (i.e. a common source) analog gain stage with a feedback capacitor (and a resistor for operating point). Unfortunately, this solution is very sensitive to voltage supply and ground references. These situations are further stressed by the large amplification gain in ASD chain (after the CSPreamp) and by common substrate layout, featuring very poor noise/disturbs rejection. This definitely degrades whole analog chain PSRR.

The main consequences are higher false positive events rate (scanning along the threshold voltage codes, i.e. about three orders of magnitude higher than specifications) and inaccurate Time-over-Threshold for low input charge (i.e. 5fC – 25fC).

In previous design, the noise signal coming from supply and ground references reaches the CSPreamp output with 6.5dB (2.11 factor) gain and, then, it is further amplified by three amplification stages causing false detections.

In this scenario, the 8xASD has been modified in terms of CSPreamp circuital topology, preferring a fully differential structure.

Post-layout simulations validate this choice demonstrating that the unwanted supply noise signal
is attenuated of -7dB (0.44 factor) at first stage output. The reduction of 13.5dB (4.7 factor) of this parameter makes it a valid choice without analog performance degradation like rising time, sensitivity, etc. The channel power consumption is the same whereas there is a total area increment of about 14%. This is due to the better isolation of analog parts from digital ones creating regions of high resistive path (named BFMOAT and provided by foundry) and Guard Rings. Area increment from 6.73mm2 to 7.64mm2 has been allowed to divide different supplies and to manage them externally by user.

An improved version of 8xASD chip for ATLAS MDT Chamber has been designed and integrated with the final target to replace the actual mounted ASICs [1].


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**Session Classification:** ASIC

**Track Classification:** ASIC
Validation of the Front-End Electronics and Firmware for LHCb Vertex Locator.

Tuesday, 12 September 2017 11:30 (25 minutes)

The LHCb Experiment will be upgraded to a trigger-less system reading out the full detector at 40 MHz event rate with all selection algorithms executed in a CPU farm. The upgraded Vertex Locator (VELO) will be a hybrid pixel detector read out by the "VeloPix" ASIC with on-chip zero-suppression. This talk will present the systems overview and design of the VELO on-detector electronics and readout firmware. Results will show the evaluation of the prototypes boards and readout firmware.

Summary

The upgrade of the LHCb experiment will be installed during the shut-down of LHC operations in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The Vertex Locator (VELO) surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. It will be a hybrid pixel detector read out by the VeloPix ASIC. The highest occupancy ASICs will have pixel hit rates of 900 Mhit/s and produce an output data rate of over 15 Gbit/s, adding up to 1.6 Tbit/s of data for the 40 Mpixels of the whole VELO.

This talk will present the architecture and the design of the VELO electronics, describing each component and how they interface to each other and to the LHCb common frame. Its main components are the VeloPix ASIC at 5 mm from the beam in a secondary vacuum tank and extremely high and inhomogeneous radiation environment, the Opto- and Power Board (OPB) outside of the vacuum, but still in a high radiation environment. The LHCb readout (TELL40) and front-end control (SOL40) boards are placed in a radiation free environment on the surface. The front-end hybrid hosts the VeloPix ASIC as well as the GBTx ASIC which provides the control signals and clocks for the VeloPix. The VeloPix transmits data packets with binary hit information and a time-stamp of 25 ns over serial highspeed electrical links at 5Gbit/s. This data is converted to optical in the OPB and sent to the TELL40 board over 300m optical links. The OPB also supplies the front end voltages using DC/DC conversion. Each of the 52 TELL40 boards handles all 20 data links from a single module. All control of the front-
end electronics is handled by 4 SOL40 boards. The firmware of VELO TELL40 boards is based on
the
LHCb common framework. However,
due to the non time ordered data stream from the VeloPix ASIC
and the specific data transfer protocol (GWT) about 80% of the code has to be customised for VELO.
Prototypes for all components of the whole readout chain,
including firmware,
have been integrated
and tested. The results and experience gained from these test will be presented.

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Session Classification:  Systems, Planning, Installation, Commissioning and Running Experience

Track Classification:  Systems, Planning, Installation, Commissioning and Running Experience
CACTµS: High-Voltage CMOS Monolithic Active Pixel Sensor for Tracking and Time Tagging of Charged Particles

Tuesday, 12 September 2017 17:45 (15 minutes)

The increase of luminosity foreseen for the Phase-II HL-LHC upgrades will lead to an unprecedented occupancy of the detectors. A solution proposed to fight against the resulting pile-up effect is to measure very accurately the time of arrival of the particles with a resolution of a few tens of picoseconds. This allows to reject by the time of flight technique the tracks associated with random pile-up vertices spread longitudinally along the protons bunches collisions. In addition, a spatial granularity better than a few millimeter will be needed to obtain a fake jet rejection rate that is acceptable for the physics analyses. Such performances should be obtained with a sensor also able to cope with the very important radiation levels expected by HL-LHC (up to 6×10^{15} 1 MeV equivalent n/cm² and 6.5 MGy).

These goals could be reached using the intrinsic benefits of the High-Voltage (HV) CMOS technology. This technology achieves in a standard process a high electric field by isolating the transistor devices -working with standard power supplies- into the collecting diodes. The technology supports high-resistivity (HR) wafers (about 2 kΩ·cm) leading to a complete depletion of the charge sensitive area (> 100 µm depth) of thinned sensors, enhancing the tolerance to neutrons damages.

Proofs of the detection capability and radiation hardness have already been produced for HV-HR technology. We will present here the architecture and simulation results of a 100 mm² pixel sensor, called CACTµS, dedicated to timing measurements. Device (TCAD) simulations and electrical simulations studies based on the HV-HR CMOS LFOUNDRY 150 nm technology design kit have been made to prepare a submission of the Cactus chip. These simulations have shown that a resolution of the order of 50 to 80 ps per MIP impact point can in principle be reached for a HV-CMOS MAPS pixels sensor with 1 mm pixel pitch.

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Session Classification: POSTER Session

Track Classification: ASIC
An FPGA-Based Track Finder for the L1 Trigger of the CMS Experiment at HL-LHC

A new tracking detector is under development for use by the CMS experiment at the High-Luminosity LHC. This upgrade will allow to reconstruct within a few microseconds charged particle tracks with transverse momentum above 3 GeV, for use in the Level-1 trigger. A concept for an FPGA-based track finder using a fully time-multiplexed architecture is presented, reconstructing tracks using an Hough Transform based algorithm. A hardware demonstrator using MP7 boards has been assembled. It operates on 1/8 of tracker solid angle at a time, processing events taken at 40 MHz with up to 200 superimposed proton-proton interactions, satisfying latency constraints.

Summary

A new tracking detector is under development for use by the CMS experiment at the High-Luminosity LHC (HL-LHC). A crucial component of this upgrade will be the ability to reconstruct within a few microseconds all charged particle tracks with transverse momentum above 3 GeV, so they can be used in the Level-1 trigger decision. A concept for an FPGA-based track finder using a fully time-multiplexed architecture is presented, where track candidates are reconstructed using a projective binning algorithm based on the Hough Transform. A hardware demonstrator using MP7 processing boards has been assembled to prove the entire system, from the output of the tracker readout boards to the reconstruction of tracks with fitted helix parameters. It successfully operates on one eighth of the tracker solid angle at a time, processing events taken at 40 MHz, each with up to 200 superimposed proton-proton interactions, whilst satisfying latency constraints. The demonstrated track-reconstruction system, the chosen architecture, the achievements to date and future options for such a system will be discussed.

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Session Classification: Trigger
Track Classification: Trigger
ALTIROC0 is an 8-channel ASIC prototype designed to readout 1x1 or 2x2 mm$^2$ 50 µm thick Low Gain Avalanche Diodes (LGAD) of the ATLAS HGTD detector. The targeted combined time resolution of the sensor and the readout electronics is 30 ps/MIP. Each analog channel of the ASIC must exhibit an extremely low jitter noise to ensure this challenging time resolution, while keeping a low power consumption of 2 mW/channel. A “Time Over Threshold” and a “Constant Fraction Discriminator” architecture are integrated to correct for the time walk.

The ASIC was received in April 2017 and testbench measurements will be presented.

Summary

The expected increase of the pile-up at the high luminosity phase of the LHC due to the 200 interactions per bunch crossing will have a severe impact on the physics. A High Granularity Timing Detector (HGTD) is proposed in front of the Liquid Argon End-Cap calorimeters for pile-up mitigation at Level-0 trigger level and in the offline reconstruction. Four layers of very thin Low Gain Avalanche Diodes (LGAD), with a transverse size of 1-2 mm$^2$, are foreseen to provide precise timing information for charged and neutral particles with a time resolution of about 30 pico-seconds per MIP. The readout FE electronics is designed to cope with the high radiation and time resolution requirements while keeping a power dissipation lower than 2 mW/cell.

To preserve the excellent intrinsic time resolution of LGAD sensors (25 ps before irradiation for gain larger than 20), the front-end ASIC must exhibit an electronics jitter smaller than 20 ps for a MIP signal (10 fC for a LGAD with a gain of 20).

ALTIROC0 is a first ASIC prototype designed in TSMC 130 nm. It integrates 8 analog channels. Each one is made of a preamplifier followed by a discriminator, which are both determinant for the overall electronics time performance. The time resolution depends on the “electronics jitter” and the “Time Walk” effect. In the final version, a 20 ps-bin Time to Digital Convertor (TDC), a digital memory and a serializer will follow the discriminator to deliver real time digital data.

The input preamplifier is the cornerstone of the design to minimize the electronics jitter. The preamplifier must be very fast (Gain Bandwidth Product larger than 10 GHz) while exhibiting a noise smaller than 0.5 fC to ensure a Signal over Noise ratio of 10. Besides, the available power dissipation for the preamplifier must be smaller than 400 µW.

The discriminator is also crucial as it determines the time accuracy measurement. The Time Walk can be corrected using Time over Threshold (TOT) architecture or Constant Fraction Discriminator (CFD) architecture.

The TOT technique requires calibration and offline correction, which prevents real time results and their use in the trigger path. The Constant Fraction Discrimination option has also been integrated to compensate for the Time Walk effect as it eliminates the shortcomings of the classical TOT technique. The position of the discriminator pulse is independent of the original pulse amplitude, compensating naturally the Time Walk. Best CFDs integrated in ASICs so far have shown time walk limitations around 1 ns, making this 20 ps requirement more than an order of magnitude beyond the state of the art. Simulation results show a time resolution better than 30 ps for input signals varying from 1 to 10 MIP. The actual time performance of the chip and the sensitivity of the integrated CFD to the pulse shape variation must be studied in real conditions.
The ALTIROC0 ASIC was received in April 2017. Its overall performance on test bench and with LGAD sensors will be presented in this presentation.

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**Presenter:** DE LA TAILLE, Christophe (OMEGA (FR))

**Session Classification:** ASIC

**Track Classification:** ASIC
Clock and Trigger Distribution for ALICE Using the CRU FPGA Card

Tuesday, 12 September 2017 08:50 (20 minutes)

ALICE is preparing a major upgrade for 2021.

Subdetectors upgrading their counting room DAQ electronics will use a common hardware to receive physics data: the Common Readout Unit (CRU).

The same CRU will also distribute the LHC clock and trigger to many of the upgrading subdetectors (~7800 front end cards).

Requirements are strict: for the clock the allowed jitter (RMS) is typically <300ps, and <30ps for timing critical subdetectors; the allowed skew is typically <1ns, and <100ps for timing critical subdetectors. A constant latency for distributing the trigger is a must.

Techniques used to meet these requirements will be presented.

Summary

In the upgraded system the CRUs will sit in the data acquisition computers in the counting room.

In the upstream direction (front end to DAQ) they will receive physics measurement data on up to 36 optical links (mostly using GBT protocol, but in some cases using detector specific custom protocols), then pre-process, and finally forward data to the host PC’s memory.

In the downstream direction (DAQ to front end) the CRUs will receive from the trigger system the LHC clock, trigger decisions, and flow control messages over a custom Passive Optical Network (PON).

The LHC Clock will be recovered, and used as a reference clock for the downstream GBT links towards front ends, thus implementing the clock forwarding.

In typical FPGA applications the high speed transceivers are used for source synchronous data transmission: clock accompanying the data is combined with and embedded into the serial data stream.

As a characteristic of these source synchronous designs, users typically do not care about the phase relation of the reference clock and the transceivers’ RX/TX clocks, or the latency for crossing between these clock domains, or about the minute variation of all these.

In our application these variations are critical, hence we are using FPGAs in an unusual way, for which these devices are not optimized. All Process, Voltage, and Temperature (PVT) variations must be controlled, to be able to meet our strict system requirements.

This is not only true for the FPGA and the design running in it, but also for all external components making up the full clock and trigger distribution chain: optical transceiver modules, external fanout buffers, multiplexers, and jitter cleaners for the clock.

This requires special attention to component selection, clocking architecture, PCB design, and clock domain crossing techniques inside the FPGA.

These considerations, the actual design decisions made, and characterization measurement results will be presented.
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Presenter:  IMREK, Jozsef (Hungarian Academy of Sciences (HU))

Session Classification:  Programmable Logic, Design Tools and Methods

Track Classification:  Programmable Logic, Design Tools and Methods
Data Analysis at Level-1 Trigger Level

Wednesday, 13 September 2017 17:45 (15 minutes)

With ever-increasing luminosity at the LHC, optimum online data selection is getting more and more important. While in the case of some experiments (LHCb/ALICE) this task is being completely transferred to computer farms, the others - ATLAS/CMS - will not be able to do this in the medium-term future for technological, detector-related reasons. Therefore, these experiments pursue the complementary approach of migrating more of the offline and high-level trigger intelligence into the trigger electronics. The presentation will illustrate how the Level-1 Trigger of the CMS experiment and in particular its concluding stage, the so-called "Global Trigger", take up this challenge.

Summary

While during the early years of LHC operation the Level-1 trigger selection was dominated by single-object triggers whose thresholds (in particular, thresholds on transverse momentum or transverse energy) were gradually raised to limit trigger rates to manageable levels, this approach would now result in significant loss of good physics data and is not viable any more. So, while silicon-tracker information will still be available only at the high-level trigger for a number of years to come, the Level-1 trigger relies increasingly on topological combinations of trigger objects from calorimeters and muon systems and on physics quantities such as invariant mass or transverse mass. This requires using particle flight directions correctly extrapolated to the vertex rather than raw detector data distorted by the bending of charged-particle tracks in the magnetic field. The enormous progress in digital electronics, in particular with regard to the computing power of Field-Programmable Gate Arrays (FPGAs) makes it possible to use input data of higher resolution and to perform complex calculations (using Digital Signal Processors (DSPs) as well as large lookup tables) for large numbers of candidate objects resulting in challenging combinatorics. The available resources also allow us to calculate in parallel certain quantities such as missing transverse energy in different ways (including or excluding the electromagnetic or hadronic calorimeter, varying the angular range with regard to the beam direction (pseudorapidity range) etc.) and use for each physics channel the most adequate version of this quantity. As jets, electron/photon candidates and "tau jets" (narrow jets from hadronic tau lepton decays) can be discriminated in the calorimeters only to a limited extent, attention must be paid to avoid double counting of such objects ("overlap removal"). By better reflecting high-level trigger resolution and algorithms in the Level-1 trigger electronics, data losses can be reduced and more useful physics events can be obtained within the available bandwidth.

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Session Classification: POSTER Session
Track Classification: Trigger
CMS DAQ Current and Future Hardware Upgrades up to Post Long Shutdown 3 (LS3) Times

Tuesday, 12 September 2017 12:20 (25 minutes)

Following the first LHC collisions seen and recorded by CMS in 2009, the DAQ hardware went through a major upgrade during LS1 (2013-2014) and new detectors have been connected during the 2016-2017 winter shutdown. Now, LS2 (2019-2020) and LS3 (2024-mid 2026) are actively prepared. This paper shows how CMS DAQ hardware has evolved from the beginning and will continue to evolve in order to meet the future challenges posed by High Luminosity LHC (HL-LHC) and the CMS detector evolution. In particular, post LS3 DAQ architectures are focused upon.

Summary

The initial requirement on the central CMS DAQ was to readout ~1MB of data at 100 kHz level-1 trigger rate (1Tb/s). The main peculiarity of its architecture was to profit from the rapid evolution of the networking technologies in order to build complete events at 100 kHz directly into computers memory without requiring a Level 2 trigger. This unique feature remains to this day.

Initially, DAQ1 was interfaced to the detector front-end via custom modular electronic (FRL) receiving the data over copper cables at 200MB/s average. The event builder (EVB) was implemented in stages with different technologies with 640 servers acting as a bridge. The assembled events were analyzed and classified by the High Level Trigger (HLT) running on ~1000 multicore servers.

During LS1, all commercial parts in the EVB and analysis farm were replaced due to their obsolescence. Moreover, part of the FRL has been upgraded to accommodate new front end systems with optical only data interfaces. The FRL produces now a TCP/IP compliant output at 10 Gb/s. The new single stage event builder is based on Infiniband FDR technology (56 Gb/s). The analysis farm has been replaced with state of the art multicore servers. With these changes, the post LS1 DAQ is now able to readout up to ~2MB of data per trigger.

For LS2, the baseline plan is a box to box replacement, no change in the hardware architecture is foreseen. However we will take profit of faster network technologies like Omni-Path or InfiniBand EDR, both running at 100 Gb/s, and more powerful analysis machines.

For LS3, due to HL-LHC design parameters, all detector readout systems must be upgraded, leading to a completely new central DAQ design, while maintaining the initial architecture supporting a single level of hardware trigger.

The upgrade of the LHC will result in a factor ~50 increase in the total data throughput and a factor ~20 increase in the requirements on the on-line computing power.

After an overview of the new readout requirements per sub-detector, we are reviewing, in detail, the possible hardware topologies for the data to surface (D2S) funneling into the event builder. The key element of the D2S will be the future DAQ and Trigger Hub (DTH) in charge of the translation and agglomeration of many custom sub-detector data streams into standard network streams. It will also provide the timing and trigger signals to sub-systems.

As of today, the DTH will be an ATCA form factor card sitting in the hub slots of the sub-system shelves. Its architecture will allow an optimal data collection within its shelf, taking into account the specific data volumes and throughput of each sub-system that can be very different from one sub-system to another.
A full program of prototyping and development is presented with a view to making available functional DTHs along with a companion software stack very early before LS3 and eventually, when we get closer to LS3, definitive full performance DTHs.

**Primary author:** RACZ, Attila (CERN)

**Presenter:** RACZ, Attila (CERN)

**Session Classification:** Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
The New Version of the LHCb SOL40_SCA Core to Drive Front-End GBT-SCAs for the LHCb Upgrade

Wednesday, 13 September 2017 17:45 (15 minutes)

The LHCb experiment is currently engaged in an upgrade effort that will implement a trigger-less 40 MHz readout system. The upgraded Front-End Electronics profits from the GBT chipset functionalities and bidirectional optical fibers for readout, control and synchronization. This paper describes the new and final version of the firmware core that transmits slow control information from the Control System to thousands of Front-End chips, discussing the implementation that expedites and makes the operation more versatile. The detailed architecture, original interaction with the software control system and integration within the LHCb upgraded architecture are described. First tests in FPGAs are shown.

Summary

The LHCb experiment is one of four experiments operating at the Large Hadron Collider and it consists of a high precision detector that focuses in the detection of decays of particles containing B mesons.

LHCb is currently involved in an Upgrade effort that will happen between 2019 and 2020. During this upgrade, most of the on-detector and back-end electronics will be replaced. In order to relay the event information from all bunch crossings to the Software Trigger, the readout electronics will have to cope with the full 40MHz bunch crossing rate without performing first-level event triggering. In view of this requirement, the experiment is using the GBT chipset and its related components developed by the EP-ESE group at CERN, for data readout as well as for fast control and slow control tasks. In particular, to aid the slow control tasks, the GBT-SCA ASIC is specifically used to configure and monitor the Front-End electronics (FE) via a set of protocols such as JTAG, I2C and SPI, among others. In LHCb, these are controlled via FPGA-based electronics boards -commonly referred to as SOL40 – interfaced to the software control system via a PCIe bus.

It is estimated that the LHCb experiment will contain around 2500 Master GBTs and GBT-SCAs and around 10000 FE chips. To be able to drive the numerous GBT-SCA chips in the FE, a specific firmware core was initially developed. It consists of a technology agnostic firmware VHDL core, developed in a generic way to support all buses and protocols of the GBT-SCA chips. Such core is driven by a bus such as the Altera Avalon bus and drives the GBT-SCA chip through optical links via GBTs. However, the first implementation employed too many FPGA logical resources and it lacked the necessary speed to configure and monitor the FE electronics in a fast way.

This document discusses the improvements and solutions in the firmware core so that it can handle the configuration and constant monitoring of the FE chips during the operation of the LHCb experiment. These improvements aim at increasing the amount of GBT-SCAs that can be reached by each core instantiation in order to save resource utilisation. They also aim at shortening the execution time of the most taxing control operations through the use of protocol accelerators and memories, reducing the interaction between software and hardware. The most immediate use cases are the mass configuration of GBTx chips dedicated to the transmission of data and the remote configuration of FPGAs located at the FE. At LHCb, this design was implemented for both an Arria X FPGA that is mounted on the LHCb PCIe40 board, and a Stratix V FPGA that is mounted on the LHCb MiniDAQ prototype board. The architecture of this core will be discussed in detail.
as well as its integration in the global readout control architecture and its interaction with the software control system. Tests using real Front-End hardware were performed for all GBT-SCA protocols, including remote FPGA configuration of Kintex7 and IGLOO2 FPGAs.

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**Co-authors:** ALESSIO, Federico (CERN); GASPAR, Clara (CERN)

**Presenter:** VIANA BARBOSA, Joao Vitor (CERN)

**Session Classification:** POSTER Session

**Track Classification:** Programmable Logic, Design Tools and Methods
MuTRiG: A Silicon Photomultiplier Readout ASIC with High Timing Precision and High Event Rate Capability

The MuTRiG chip, which is dedicated to the Mu3e experiment, is a 32 channel mixed-signal Silicon Photomultiplier readout ASIC with high timing precision and high event rate capability designed and fabricated in UMC 180 nm CMOS technology. It combines the excellent timing performance of the fully differential analog front-ends and the 50 ps time binning TDCs with a high event rate capability from a dedicated on-chip digital logic circuit and a gigabit LVDS serial data link. The design of the chip and the results from the characterization measurements will be presented.

Summary

The Mu3e experiment is designed to probe new physics by searching for the lepton flavour violating decay of \( \mu^+ \rightarrow e^+e^-e^- \) at a sensitivity level of \( 10^{-16} \). A high timing resolution of 100 ps (\( \sigma \)) and 500 ps (\( \sigma \)) is required for the Mu3e Tile Detector and the Mu3e Fibre Detector, respectively, in order to suppress the combinatorial background below the signal level as well as to facilitate the event reconstruction. The event rate of the Fibre Detector will be at the level of 700 kHz/channel to 1.3 Mhz/channel, posing extra challenges to the detector system and the readout electronics.

MuTRiG is a mixed-signal Silicon Photomultiplier (SiPM) readout ASIC with high timing precision and high data rate capability. It is dedicated to the readout of the Mu3e Tile Detector and the Mu3e Fibre Detector. MuTRiG consists of 32 SiPM readout channels, each of which comprises an analog front-end and a Time-to-Digital Converter (TDC), as well as an integrated digital logic circuitry for event processing and data transmission to an external Data Acquisition system (DAQ). The analog front-end is designed in a fully differential structure to suppress the common mode noise from both the on-chip digital circuit and the external sources. The TDC has a binning of 50 ps, ensuring a precise time digitization. The analog front-end and the TDC have been extensively characterized with the STiCv3 chip and have proven an excellent timing performance. The digital logic circuitry has been upgraded to sustain the high input event rate as well as to provide additional functionalities such as external trigger function, channel event counters and CRC for data transmission error detection. A gigabit serial data link consisting of a Double Date Rate (DDR) serializer and a customized LVDS transmitter has been implemented in the MuTRiG chip to tackle the high event rate challenge from the Mu3e Fibre Detector.

Characterization measurements have shown an analog front-end jitter of less then 20 ps when injecting charge via a 33 pF capacitor, a Single Photon Time Resolution (SPTR) of 150 ps obtained with Hamamatsu S13360-1350CS MPCCs and reliable 8b/10b encoded data transmission at a data rate of 1.28 Gbps. In this paper we will present both the design and the characterization measurement results of the MuTRiG chip.

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MuTRiG: A Silicon Photomultiplier Tracker

Presenter: SCHIMANSKY, David (Heidelberg University)

Session Classification: ASIC

Track Classification: ASIC
Rad-Hard Fibre Optics Cabling Design for LHC Detectors Upgrades

Wednesday, 13 September 2017 17:45 (15 minutes)

Upgrades over the next decades will enable LHC to operate at a higher luminosity (HL-LHC). Accordingly, the optical links designed to transmit collision data should be hardened against increased radiation levels, allowing for a reliable communication. This paper studies fibre cabling design of a generic link between the in-detector optical front-end and the counting room. The proposed solution concatenates radiation-resistant and conventional fibres using multi-fibre interconnections. The radiation penalty calculation considers a temperature of \(-30^\circ\text{C}\) inside the detector innermost part. The maximum link loss during HL-LHC lifetime is estimated to be 3.16dB, complying with predefined margins of Versatile Link system.

Summary

High speed optical links are critical building blocks of LHC detectors as they transmit particle collision data to the counting room immediately after detection. In this respect, the CERN Versatile Link (VL) project has been active since 2008 to provide point-to-point bi-directional links for upgrades of LHC experiments. The high radiation dose in proximity to these links necessitates special design and/or selection criteria for active and passive components to ensure their performance during the accelerator runtime. With the foreseen upgrades in HL-LHC the Versatile Link Plus (VL+) project was launched to target higher speed links and to provide the stringent design parameters for operating in a higher radiation dose. This paper studies the design of VL+ optical passive components including optical fibres and connectors to achieve the lowest possible link loss. The analysis considers a variable Radiation Induced Attenuation (RIA) model adapted to the dose map and variations of temperature along the designed fibre path.

A critical design criterion for the link loss is minimizing the aggregated RIA which is a function of accumulated dose, irradiation dose-rate, fibre temperature and transmitted power over the link path. The path studied in this work is designed to route the optical fibre inside the detector front-end to the intermediate patch panels through an existing cabling track. The path continues afterwards to the counting room passing through the standard cable trays. Once the link path is determined, the radiation penalty \(P\) is examined for three candidate multi-mode fibres by integrating the incremental RIA element \(dP = f(\Gamma, T)dr\) over the fibre path \(r\). The \(f\) function (in dB/Km) approximates piecewise RIA given the accumulated dose \(\Gamma\) and fibre temperature \(T\) as the arguments. We evaluated this function experimentally for tested fibres at accumulated dose \(\Gamma \leq 1\ \text{MGy}\) and for the temperatures set \(T = \{ -30, 25 \}^\circ\text{C}\) corresponding to the inner and outer detector ambient temperatures.

The RIA was evaluated for candidate fibres using the temperature and accumulated dose maps simulated for HL-LHC lifetime. Results show that a specific Radiation-Resistant (RR) fibre outperformed other tested fibres by more than 4.5dB in radiation penalty. Yet, inspecting the RIA distribution over the link path identifies high and low RIA zones respectively inside and outside the detector area for all tested fibres. Therefore as a cost efficient solution, the final design concatenates a RR fibre at the detector side to a conventional fibre at the counting room side with interconnection close to the detector outer volume. Given the new design the maximum RIA for a generic LHC cable path was calculated to be 1.4dB during the HL-LHC lifetime. Assuming a
maximum 0.36dB propagation loss and an insertion loss of 1.4dB including four optical interconnections by 24-fibre MT and MPO ferrules, the resulting end-to-end link loss is strictly lower than 3.16dB which is below the predefined link margin at 3.9dB. It is worth noting that optical connectors using multi-fibre MT and MPO ferrules are shown to have a negligible radiation penalty at the expected radiation levels.

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**Presenter:** BLANC, Jeremy (CERN)

**Session Classification:** POSTER Session

**Track Classification:** Radiation Tolerant Components and Systems
Electro-Migration Driven Failures on Miniature Silver Fuses at the Large Hadron Collider

Tuesday, 12 September 2017 17:45 (15 minutes)

In the Large Hadron Collider (LHC), the cryogenics instrumentation infrastructure uses fuse-protected high-voltage isolated temperature transducer cards. Spurious faults were observed at their miniature silver fuses during the periods 2008-2010 and 2014-2016 and a study was launched to understand the underlying failure mechanism.

The study uses data from Scanning Electron Microscopy (SEM), spectrometry, Weibull reliability calculations, operating temperature profiles and existing data logging tools. For the period 2014-2016, the fuse failures followed a Weibull distribution of $\beta = 3.91$ and $\eta = 2323$ days. The leading failure mechanism was attributed to electro-migration phenomena.

Summary

In the Large Hadron Collider (LHC), the cryogenics instrumentation infrastructure uses fuse-protected high-voltage isolated temperature transducer cards. Approximately 1200 such cards are installed and each of them is protected by a miniature fuse based on a thin silver wire. The typical current consumption per electronic card is 0.5A.

Fuse failures were observed during periods 2008-2010 and 2014-2016. Those failures resulted in loss of instrumentation signals, occasional loss of cryogenic conditions and required multiple in-situ interventions. Every failure was a “sudden” event. After the failures of the first period, the fuse current rating was increased as a corrective measure, all fuses were replaced and no further failures were observed until 2014. After the failures of the second period, a study was launched to understand the underlying failure mechanism.

The study uses data from Scanning Electron Microscopy (SEM), spectrometry, Weibull reliability calculations, ambient data and data logging tools. The paper presents the difficulties of preparing the data for a Weibull reliability analysis; exact knowledge of electronic cards installation time, operating temperatures, replacements due to other failures and periods during which they could have been unpowered.

During the first period, the rating of the operating fuse was 1 A. 1202 cards were installed at 19 different locations and the failures started occurring at 3 locations having the highest fuse temperatures. At those 3 locations, 150 cards were installed and the failures of those 150 cards followed a Weibull distribution of $\beta = 2.8$ and $\eta = 2215$ days. After 2010, the fuses were replaced with others having a higher rating of 1.25 A. Furthermore, 764 out of the 1202 cards were upgraded to another version consuming less current. Therefore only 438 cards of the “original” failing type remained in operation. For this second period of 2014-2016, failures were observed at 2 locations and for a total population of 46 cards. Due to the upgrade of the cards, there were no cards of the “original” failing type at the third location. The failures of the second period followed a Weibull distribution of $\beta = 3.91$ and $\eta = 2323$ days. When using failure data of only the same 2 locations for the period 2008-2010, the failures followed a Weibull distribution of $\beta = 3.43$ and $\eta = 1687$ days for a total of 102 cards. The leading failure mechanism was attributed to Electro-migration phenomena.

It is therefore concluded that the upgrade of the fuses from 1 A to 1.25 A led to an increase of the MTTF but the underlying failure mechanism remained the same. The temperature and electrical current through the fusing wire were the leading factors of the aging mechanism. A component considered as “lifetime” had much lower than expected Mean Time to Failure (MTTF) based on its operating conditions.
During the last technical shutdown, this problem has been addressed by using a fuse with a higher stated reliability and by increasing the electronic cabinet separation to improve the natural convection resulting in a lower fuse temperature.

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**Presenter:** TRIKOUPIIS, Nikolaos (CERN)

**Session Classification:** POSTER Session

**Track Classification:** Production, Testing and Reliability
Commissioning and First Running Experiences with the TOP Barrel PID Detector in the Belle II Experiment

Tuesday, 12 September 2017 11:05 (25 minutes)

The Time of Propagation (TOP) detector is a novel Cherenkov barrel particle identification system built for the Belle II detector upgrade based on quartz radiator bars read out by Micro-Channel Plate PMTs. The readout electronics of the TOP system are built around a switched capacitor array waveform sampling ASIC operating at 2.7GSa/s. Acquired waveforms are processed in real time in the front end electronics, extracting the individual timing of detected photons to better than 100ps.

This talk presents the current status of commissioning, calibration and operation of the Belle II TOP detector.

Summary

During the upgrade of the Belle detector to accommodate the increased instantaneous luminosity of up to $8 \times 10^{35}$cm$^{-2}$s$^{-1}$ delivered by the SuperKEKB accelerator, its barrel particle identification system was completely replaced by the novel Time of Propagation (TOP) detector. The Cherenkov photons generated in its 16 250x44x2cm$^3$ quartz radiator bars are detected by arrays of Micro-Channel Plate PMTs (MCPs). The traversing particle type is determined from its time of propagation and Cherenkov angle, which are reconstructed from the spatial and temporal distribution of photons detected in the MCPs.

In order to fulfill the performance requirements of separating kaons from pions in the momentum range of 1GeV/c to 4GeV/c with an efficiency of 90% in the challenging environment of high event rates and machine backgrounds, custom readout front end electronics (FEE) were developed for TOP. The signals of all 8192 MCP channels in the system are acquired by custom Ice Ray Sampler ver. X (IRSX) ASICs, which are continuously sampling into a switched capacitor array at 2.7GSa/s. The buffer depth of 10us allows the digitisation and data transfer of dynamically determined groups of samples upon arrival of an external trigger without incurring deadtime in the acquisition.

The TOP FEE is organised into 64 subdetector readout modules (SRMs). One SRM is assembled as a board stack of one Standard Control Readout Data (SCROD) controller board and four ASIC carrier boards hosting four ASICs each, for a total of 128 readout channels corresponding to eight MCPs per SRM.

As the data bandwidth going out of each SRM is limited during physics running, all signal analysis and data processing of the MCP waveforms is handled online on the carrier and SCROD boards. Photon pulses in the digitised waveforms are extracted using constant fraction discrimination and template fitting techniques implemented into the Xilinx Zynq SoCs integrated into the SRMs. Only the parameters of extracted photon pulses are transferred into the Belle II datastream to be used in the offline reconstruction.

The TOP detector has been fully assembled into the Belle II enclosure and the whole detector has been successfully rolled into its final position in the beamline. Each TOP module has been commissioned and tested with laser pulses and cosmic rays before and after its installation into the TOP enclosure. Combined calibration runs taken with the completed TOP system with laser pulses and direct charge injection have been taken continuously since the completion of the installation. A first global cosmic ray run including the whole outer detector of Belle II is planned to start in early Summer.
This talk will present the current status of commissioning, calibration and operation of the Belle II TOP barrel particle identification system, an overview of the online data processing as well as first look into global cosmic ray runs data, current performance figures and lessons learned up to now.

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**Presenter:**  HARTBRICH, Oskar (University of Hawaii at Manoa)

**Session Classification:**  Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:**  Systems, Planning, Installation, Commissioning and Running Experience
Development of a Waveform Sampling ASIC with Femtosecond Timing for a Low Occupancy Vertex Detector

Tuesday, 12 September 2017 17:45 (15 minutes)

One of the crucial parts of the proposed low occupancy Timing Vertex Detector (TVD) is a waveform sampling ASIC denoted the RFpix. It is being developed to sample and digitize voltage pulses and enable measurements of their arrival times with a timing resolution of 100fs or less. To achieve this, the RFpix needs to have an analog bandwidth of 3GHz and a sampling speed of 20GS/s. In this paper, we present the architecture of the RFpix and discuss the challenges of designing and implementing the various subcircuits necessary to achieve the required performance.

Summary

Increasing luminosities of particle colliders result in ever higher hit rates of the innermost vertex detectors, thus increasing their occupancies. The TVD sensor architecture relies on using an asynchronous digital pixel matrix for detection and a high-precision timing readout technique, where the pixel position is encoded in the time of flight of voltage pulses on a micro-strip line. The arrival times of the pulses are measured by a waveform sampling ASIC called the RFpix, the architecture of which is based on differential switched capacitor (SCA) arrays. The prototype has 32 channels. Each channel has two unity gain amplifier buffers to decouple the capacitive loading of the SCA arrays from the inputs, thus providing the necessary analog bandwidth of 3GHz in a wire bonded package. The differential configuration of the SCA helps in terms of crosstalk mitigation and noise coupling. At the same time, it turns the amplitude dependent voltage error, due to charge injection, into a virtual gain of the sampling cell. The strobe signals are generated by a two-level delay locked loop (TLDLL), which ensures a worst case added jitter of 41fs. Two adjacent channels share one TLDLL, which has several advantages: avoiding loading on the strobe lines and thus providing with fast strobe rise times (app. 30ps), lowering of the power consumption, and providing with the possibility of interleaving. With the TLDLL tap delay of 50ps, the 20GS/s sampling speed is achieved. Every SCA block has a trigger logic that issues a transfer cycle, which latches the SCA block for 3.2ns (64 cells x 50ps) upon signal detection. Within this time, the SCA cell values are transferred in parallel to an analog storage array. Each storage array has a depth of 32 storage cells. Each storage cell has an integrated comparator, which is a part of a parallel slope ADC, which runs at a speed of 128MS/s/channel due to its parallel configuration. The digitized data is transmitted off-chip by a serializer logic through a dedicated LVDS driver per channel. With a 12-bit ADC, buffer depth of 5µs, and the system trigger of 30kHz, the overall data throughput is around 2Mbits/s/channel. The average power consumption without the input buffers is estimated at 25mW per channel. The input buffers are not planned in the final detector version (flip-chip mounting directly on the sensor). The prototype is being designed in the TSMC 130nm technology node, which has proved to have good performance in radiation-hard environments. In addition, working in this technology provides the necessary transistor speeds, dynamic range, and level of integration. The RFpix is to be the first low-power, multi-channel waveform digitizer with timing resolution in the range of 100fs.
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Session Classification: POSTER Session

Track Classification: ASIC
Readout Electronics System of the CASCA Front-End Chip for the TPC Based X-Ray Polarimeter

Wednesday, 13 September 2017 17:45 (15 minutes)

The CASCA is a 32-channal readout ASIC designed for the TPC based X-ray Polarimeter (XTP). We propose a prototype Readout system of the CASCA chip for the XTP. The system mainly consists of three kinds of modules. The ASIC cards, mounted with CASCA chip, are designed for sampling XTP signals. The Adapter card, edged-mounted with the ASIC card, is in charge of digitizing the output from ASIC card. The Master card provides 8 channels for 8 Adapter cards based Serial-Rapid-IO protocol at 6.25Gbps bandwidth, and transfers data through 10 Gigabit Ethernet, therefore 256 electronics channels are achieved.

Summary

Micro-pattern TPC (Time Project Chamber) based X-ray polarimeter has been demonstrated in recent years for its main advantage of releasing the competition between absorption depth and drift distance. It measures two dimensional photoelectron tracks generated by the incident X-ray photons with one dimensional strip readout. The other dimension is calculated by the drift time from the signal waveform. The polarimeter focuses on the X-ray energy of 2-10 keV whose track length is only several millimeters, and 100 um track resolution, fast sampling rate (~20MSPS) is required.

The CASCA (Charge amplifier and switched capacitor array) chip designed for XTP is a 32-channal readout front-end ASIC integrated with the front-end part and the SCA (Switched Capacitor Array), the former for amplifying and shaping and the latter for sampling. The sampling rate of the ASIC is designed for 40Msps and the valid readout frequency is 5MHz. The ASIC card named CASCA_FE is designed for driving the CASCA chip. A high performance differential amplifier is adopted in the CASCA_FE to provide the rail-to-rail output for the ADC (Analog to Digital Converter) in the Adapter card.

The Adapter card named CASCA_AD, edged-mounted with the CASCA_FE, is in charge of digitizing the output from the CASCA_FE. A Xilinx Artix-7 FPGA chip, a 12-bit ADC and a multi-output clock generating chip are mounted on the CASCA_AD. The FPGA chip provides logic signals to make the CASCA_FE working properly, and is responsible for packaging the digital data from the ADC. The ADC provides 10Mps sampling rate and 12-bit accuracy in parallel output, which is able to digitalize the output of the ASIC efficiently. The clock generator is configured to meet the requirement of the sampling clock and readout clock.

The CASCA_AD edged-mounted with CASCA_FE is near to the detector for sampling waveform. And a HDMI cable is adopted to connect the CASCA_AD and the Master card. The initial voltage were supplied via the HDMI cable from Master card, as the same way that the packaged digitalized data, source clock and trigger signal were transferred.

With the help of the Serial Rapid-IO Technology and HDMI2.0 cable, the bandwidth of Dataflow could achieve the maximum of 6.25Gbps. The data transfers through the Serial Rapid-IO protocol realized by the Logic IP Serial Rapid-IO Gen2 Endpoint Solution in the FPGA chip.

The Master card named HPDAQ as a FMC-Based card with two FMC connectors, which is responsible for digital data acquiring and processing, connects to the CASCA_AD through a Mezzanine card. In a way of "Several-in-One", 8 CASCA_AD cards are connected to one Master card with
8 HDMI cables. And the Master card transmits data to Server over 10 Gigabit Ethernet. A high-performance FPGA and DDR4 are adopted to provide the logic resource, I/O interfaces and data buffer.

This readout electronics system is flexible to apply in the XTP. One Master card is able to support 256 electronics channels, and a large number of the Master card could be assembled in parallel to meet the requirement of the large XTP.

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**Presenter:** Mr HENGSHUANG, Liu

**Session Classification:** POSTER Session

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Development of a Large Pixel Chip Demonstrator in RD53 for ATLAS and CMS Pixel Upgrades

Tuesday, 12 September 2017 11:05 (25 minutes)

The development of a large scale 65nm CMOS pixel demonstrator chip for very high rate (3GHz/cm²) and very high radiation levels (1Grad) for ATLAS and CMS phase 2 pixel upgrades has taken place within the RD53 collaboration. The development and testing of radiation test structures, building blocks and small scale pixel array demonstrators are summarized together with test and radiation characterization results. The design and verification of a large scale (20mm x 12mm) pixel chip demonstrator, RD53A is described together with an outline of the plans to develop final pixel chips for the two experiments.

Summary

The presentation summarizes the work that has been made within the RD53 collaboration during the last 3-4 years to arrive to the design of a large scale RD53A pixel demonstrator chip, that will be submitted for prototype production in June 2017. The RD53A chip is expected back from prototype production in August and an extensive testing and qualification program will take place during the following months.

The architecture of the RD53A chip will be described together with results from extensive architectural simulations and verifications. The chosen design and verification approach for this complex high rate and high radiation level design will be outlined.

The development and test of a large number of different building blocks (analog front-ends, calibration circuit, Bandgap, DACs, ADC, PLL, serializer, cable driver, serial IO, serial power Shunt-LDO regulator, on-chip monitoring of temperature/radiation/current/voltages, etc.) will be summarized. All building blocks have been prototyped and extensively tested, including radiation testing, to arrive at final building blocks as integrated in the RD53A demonstrator.

The results of several years of radiation characterization of the 65nm technology at both transistor level and circuit level will be summarized to justify key design choices of the RD53A to demonstrate the capability to make pixel chips that can sustain and survive the extremely challenging operating conditions of a HL-LHC era pixel detector.

Finally an outline of how the design and test of the RD53A demonstrator will be used to drive the design of final pixel chips, within RD53, for the phase 2 pixel upgrades of both ATLAS and CMS.

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Presenter: CONTI, Elia (CERN)

Session Classification: ASIC

Track Classification: ASIC
Low Voltage Powering of On-Detector Electronics for HL-LHC Experiments Upgrades

Tuesday, 12 September 2017 16:30 (15 minutes)

All LHC experiments will be upgraded during the next LHC long shutdowns (LS2 and LS3). The use of more advanced CMOS technology nodes typically implies higher current consumption of the on-detector electronics. In this context, and in view of limiting the cable voltage drop, point-of-load DC-DC converters will be used on detector. This will have a direct impact on the existing powering scheme, implying new AC-DC and/or DC-DC stages as well as changes in the power cabling infrastructure. This paper will present the first results obtained while evaluating different LV powering schemes and distribution layouts for HL-LHC trackers.

Summary

Currently, most LHC systems use relatively complex very low voltage power supplies to power their on-detector electronics directly or through radiation tolerant linear regulators. This existing infrastructure is based on radiation and magnetic field tolerant power converter systems generally consisting of remote bulk AC-DC converters and control systems linked to local DC-DC converters qualified for harsh environment. At HL-LHC, the use of POL (point-of-load) DC-DC converters and the expected overall power consumption increase will impose to change the existing powering chain and infrastructure.

POL DC-DC converters require higher input voltages than currently available. Besides reducing the voltage drop induced by the cabling, they present the advantage of potentially relaxing certain power supply requirements such as noise and ripple as well as the voltage regulation precision and stability.

Different solutions are being explored, simulated and qualified to supply POL DC-DC converters. The precise low voltage power source requirements are being assessed and understood using the CMS tracker upgrade as a use-case. In particular, the control granularity as well as the dynamic behaviour of the entire powering chain is being carefully evaluated and simulated. For this study, the power chain is subdivided in three parts, the power source, the monitoring and control and the cabling.

Once well qualified, the explored solutions will serve as a baseline for drafting a detailed technical specification towards the next generation of power supply systems to be proposed to experiments. The studied powering chain will hopefully also serve as conceptual baseline for the detector groups from various experiments to implement their own solutions.

This paper presents the results obtained from the different powering schemes evaluated so far. Focus is given on the first studied use-case consisting of the CMS tracker upgrade. However, some conclusions are surely common to other systems. A first set of key requirement parameters for the power source to be used with the POL DC-DC converter will also be drafted.

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**Presenter:** BOBILLIER, Vincent (CERN)

**Session Classification:** POSTER Session

**Track Classification:** Power, Grounding and Shielding
Currently there is a lot of activity in R&D for future colliders. Multiple detector prototypes are being tested, each with different requirements for data acquisition and monitoring, which has generated different ad-hoc software solutions. We present DQM4HEP, a generic C++11 framework for online monitoring for particle physics experiments, and results obtained at several testbeams with detector prototypes using the framework as it was developed. We also present the currently ongoing work to integrate DQM4HEP and EUDAQ, which will allow these to work together as a complete and generic DAQ and monitoring system for any detector test, as part of AIDA-2020.

Summary

There is currently a lot of activity in R&D for future collider experiments. Multiple detector prototypes are being tested, each one with slightly different requirements regarding the format of the data to be analysed. This has generated a variety of ad-hoc solutions for data acquisition and online data monitoring. We present a generic C++11 online monitoring framework called DQM4HEP, which is designed for use as a generic online monitor for particle physics experiments, ranging from small tabletop experiments to large multi-detector testbeams, such as those currently ongoing/planned at the DESY2 or CERN SPS beamlines. We present results obtained using DQM4HEP at several testbeams where the CALICE AHCAL, SDHCAL and SiWECAL detector prototypes have been tested. During these testbeams, online analysis using DQM4HEP’s framework has been developed and used. We also present the currently ongoing work to integrate DQM4HEP within the EUDAQ tool. EUDAQ is a tool for common and generic data acquisition within the AIDA-2020 collaboration. This will allow these two frameworks to work together as a generic and complete DAQ and monitoring system for any type of detector prototype tested on beam tests, which is one of the goals of the AIDA-2020 project.

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Presenter: COATES, Tom (University of Sussex (GB))

Session Classification: POSTER Session

Track Classification: Other
The project of the LHCb upgrade foresees a replacement of the whole acquisition system of the detector to allow a full readout at 40 MHz. The development of a new control board, called the 3CU for the electromagnetic and hadronic calorimeters was proposed. This board receives commands from the main LHCb control system and sends them through the backplane to the front-end boards. Each calorimeter crate is equipped with one unique 3CU plugged in the central slot which also provides the clock, slow controls, and Fast Control command to all the boards inside the same crate.

Summary

LHCb, one of the four particle physics experiments at the Large Hadron Collider at CERN (Geneva), is aiming at studying CP violation and rare decays using B-hadrons. Its results contribute to complete the understanding of quark flavor physics in the framework of the Standard Model, and may reveal sign of the physics beyond the Standard Model. The LHCb experiment started data taking in 2009 and an upgrade of the detector is planned for 2019.

For the purpose of the LHCb upgrade, it is foreseen to replace the electronics of the calorimeter. The calorimeter front-end crate is a standard 9U VME-like frame. Inside each crate, 16 front-end boards and a single control board (in the central position of the crate) are plugged. The calorimeter new acquisition system will be controlled by the so called 3CU board. It is responsible for sending and processing the information received through optical fibres from the main LHCb system to the front-end boards.

The S-ODIN system receives directly the clock from the RF-system of the LHC via an LHC Interface card located on the S-ODIN card. The S-ODIN card distributes the clock and the Fast Control commands to the SOL40 and TELL40 board, and the SOL40 board distribute the Clock and the Fast Control command to the 3CU board.

The main role of the 3CU is to receive the GBT frame through the optical link and to extract the information which is needed by the FEBs inside a same crate: the 40 MHz clock, the Time Fast Control (TFC) commands and Experiment Control System (ECS).

The various parts of the board are:
- A Versatile Link Transceiver / Receiver (VTRx), for the reception and transmission to the SOL40 board.
- A radiation tolerant chip that can be used to implement multipurpose high speed (3.2-4.48 Gb/s user bandwidth) bidirectional optical links (GBTX).
- GBT-SCA ASIC, part of the GBT chip-set, to distribute control and monitoring signals to the on-detector front-end electronics and perform monitoring operation of detector environmental parameters.
- A Microsemi FPGA (IGLOO2 family) who is in charge of the processing on the 3CU.

First the 3CU receives the clock and the TFC commands through the optical transmitter (VTRx) and decoding inside the GBTX. After processing (inside IGLOO2), the board transmits through the 3U backplane these signals to all the FEB inside the same crate. The FEB are protected by delatchers which detect any current increase that could be due for example, to a Single Event Latchup (SEL). The 3CU board is in charge to monitor the delaching status of all FEBs inside the same crate.

The greater part of the 3CU components have been tested in proton and heavy ions beams in order to test the radiation tolerance of the board and its immunity to accumulated dose and single event
latch-up effects. The FPGA are ACTEL flash technology component and cope the radiation level expected. A mitigation technique (triple voting) will be implemented in the firmware of the FPGAs to prevent single event upsets.

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**Session Classification:**  POSTER Session

**Track Classification:**  Other
The VTRx+, an Optical Link Module for Data Transmission at HL-LHC

Wednesday, 13 September 2017 08:30 (20 minutes)

Optical data transmission will remain a key enabling technology for the upgrading detectors at HL-LHC. In particular, the inner tracking detectors will require low-mass, radiation tolerant optical transmit- and receive modules for tight integration in the detector front-ends. We describe the development of such a module, giving details of the design, functional and environmental performance and showing the feasibility of achieving small size, low-mass, and low-power operation.

Summary

During the phase II upgrades of the ATLAS and CMS experiments at the Large Hadron Collider (LHC) several detectors will be replaced to improve their physics performance. In particular, these upgrades aim to replace the innermost detectors that are exposed to the harshest radiation environments. To cope with the increasing data volume and the higher trigger rate, high-speed optical links will be deployed in large quantities as part of the upgrade programme. The tight space constraints and the high channel count of the on-detector electronics will require to develop a low-profile (20mm x 10mm x 2.5mm target), multi-channel front-end component. During their expected lifetime these components will have to withstand the on-detector radiation levels (1MGy total dose, 1x10^15 n/cm2 and 1x10^15 hadrons/cm2 total fluence) and they have to operate over a wide temperature range (-35 °C to +60 °C). The Versatile Link PLUS (VL+) project is developing custom front-end modules that fulfill these requirements. The front-end module (VTRx+) will be based on radiation-hard laser diode driver (LDD) and transimpedance amplifier (TIA) ASICs, and commercial VCSEL and PIN photodiode (PD) components. The initial project phase of demonstrating the feasibility of the VTRx+ design has now been completed. Components have been evaluated and shown to meet the required performance targets during both functional and environmental testing. We will show an overview of the static and dynamic performance of VCSELs and PDs operating over the full required temperature range. These tests allow us to select devices that perform best for further investigation. Radiation testing has also been carried out for candidate VCSELs and PDs and the results will be shown, along with the impact of the observed degradation on system performance and margins.

The module design is being carried out in two parallel paths: the first being to carry out a full-custom design based on commercially-available optical coupling blocks; the second to carry out minimal customisation of an existing commercially-available module. The former path allows us to learn about the difficulties of the design and inform the requirements of the second path. We will outline the various procedures put in place to enable the parallel developments to be carried out in a robust commercial framework with the clear path to volume production. The measured performance of the various module types will also be reported.

Finally, we will give an overview of the work being done to integrate the modules in various user systems, highlighting the challenges brought to the overall common design by different use-cases. This will be accompanied by the overall project timeline leading up to production starting in 2019 so as to be aligned with the production and assembly timescales of the HL-LHC experiments.
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**Presenter:** TROSKA, Jan (CERN)

**Session Classification:** Optoelectronics and Links

**Track Classification:** Optoelectronics and Links
ATLAS Phase-II-Upgrade Pixel Data Transmission Development

Wednesday, 13 September 2017 17:45 (15 minutes)

The ATLAS tracking system will be replaced by an all-silicon detector (ITk) in the course of the planned HL-LHC accelerator upgrade around 2025. The readout of the ITk pixel system will be most challenging in terms of data rate and readout speed. Simulation of the on-detector electronics based on the currently foreseen trigger rate of 1 MHz indicate that a readout speed of up to 5 Gbps per data link is necessary. Due to radiation levels, the first part of transmission has to be implemented electrically. System simulation and test results of cable candidates will be presented.

Summary

ATLAS is preparing for an extensive modification of its detector in the course of the planned HL-LHC accelerator upgrade around 2025 which includes a replacement of the entire tracking system by an all-silicon detector (Inner Tracker, ITk) and a revised trigger and data taking system with triggers expected at lowest level at an average rate of 1 MHz. The five innermost layers of ITk will comprise of a pixel detector. The readout of the pixel layers will be most challenging in terms of data rate and readout speed. A new on-detector readout chip is designed in the context of the RD53 collaboration. The performance of the readout system was simulated based on hit rates from detector simulation combined with behaviour expected from the proposed chip design, assuming different buffer sizes to store data until trigger arrival with proposed trigger parameters. This simulation indicates that the expected maximum readout speed of 5 Gb/s of the chip LVDS drivers will be over-consumed in the innermost layers, making on-chip data compression necessary. The readout speed per chip is going down to values well below 1 Gb/s in the outermost layers. A latency well below that imposed by the ATLAS trigger system is added. Up- and downlink communication to the on-detector electronics is foreseen to be largely optical. However, radiation levels close to the beam pipe prevent the placement of optical components close to the readout chips such that the first part of transmission has to be implemented electrically with signals to be converted for optical transmission at larger radii. Options to group data links of outer layers are considered in order to make use of the bandwidth to be made available for innermost layers and thus reduce needed material. Consequently, cables are being developed for electrical data transmission at rates of up to 5 Gb/s over several metres. Designs cover solutions such as twin-axial, twisted pair or flex cables and hybrids of these. Prototype cable performance was inspected with dedicated bit error rate testers based on FPGA boards or commercial types. Error rate measurements are complemented by attenuation behaviour derived from S-parameter analysis and eye-diagram inspection in addition to according simulations. Some of the cables under test demonstrated maximum payload rates above the desired data rate and thus provide good candidates for the ITk-Pixel readout, however also indicate the need for driver pre-emphasis and equalization to reduce loss over the envisaged cable length.

Primary author: MACCHIOLO, Anna (Max-Planck-Institut fur Physik (DE))
Presenter: NIELSEN, Jason (University of California, Santa Cruz (US))

Session Classification: POSTER Session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience
A 2 Gsps Waveform Digitizer ASIC in CMOS 180 nm Technology

Tuesday, 12 September 2017 11:55 (25 minutes)

The design and measurement results of a waveform digitizer based on the Switched Capacitor Array (SCA) architecture, fabricated in CMOS 180 nm technology, are presented. The prototype ASIC containing two channels inside is fully functional at a sampling rate of 2 Gsps with an analogue -3 dB bandwidth of more than 400 MHz. Each channel integrates 128 sampling cells and a ramp-compare ADC. With this ASIC, sine waveform and reconstructed PMT waveform recording tests were conducted. We also evaluated its performance on fast pulse timing, and the timing precision is proved to be better than 20 ps RMS after a series of correction strategies.

Summary

In modern particle physics experiments, waveform digitization offers maximum possible information, such as arrival time, charge, waveform shape, and so on. As for fast detectors used for precise timing, e.g. Multi-gap Resistive Plate Chamber (MPRC), a high sampling rate up to Gsps (Giga-samples per second) is required. The traditional solution employing fast Analog-to-Digital Converters (ADCs) in the Gsps level suffers from power dissipation, and especially high cost. The above disadvantages preclude it from application in modern particle physics experiments, in which a huge volume of channels are often employed. An alternative approach to tackle these requirements is Switched Capacitor Arrays (SCAs). SCAs use a series of capacitors, connected via switches to an input bus to sample an analogue signal, and this architecture has the advantage that they can operate at several Gsps with low power consumption.

This paper presents a two-channel SCA ASIC prototype, and each channel has a depth of 128 sampling cells. The shared sampling clock is generated by an on-chip Delay-Locked Loop (DLL), in which the time delay of each stage is made from a CMOS current-starved inverter and the adjustable range is between 0.5 ~ 2 ns. Because of the feedback operation mode, the sampling rate is determined completely by the external input reference clock, almost independent of temperature, power supply and process. In the sampling circuit, to obtain a high input bandwidth and to reduce the distortion cause by switch’s on-resistance, a careful tradeoff is made. Finally, a dual CMOS switch and a 110 fF MOS capacitor are used. After waveform capture, parallel digital conversion of all sampled signals is done on-chip with a ramp-compare ADC which consists of a global ramping voltage, a comparator for each cell and a 12-bit Gray-code counter. The digitized data is serially read out using a shift register ‘token’ architecture.

The proposed prototype was fabricated in CMOS 180 nm technology, and it can be fully functional at the sampling rate of 2 Gsps. Results in terms on DC offset, noise, frequency response, sampling intervals correction and fast pulse timing are presented. The input voltage range is 0~1.1 V with an uncorrected Integral Non-Linearity (INL) 1% over a 900 mV dynamic range, and the offset among each cell varies between -15.62 to 25 mV because of process. Noise, after on-chip digitization, is equivalent to ~1.5 mV RMS. The frequency response result indicates that the analogue -3 dB bandwidth of the chip is above 400 MHz. For precision waveform timing extraction, the sampling interval variations must be calibrated and corrected. The ‘zero-crossing’ method is used to get the real sampling intervals. Finally, the effective timing resolution with a fast Gaussian input pulse is calculated by waveform feature extraction after linearity and sampling intervals correction as well as leading-edge fitting, and the timing precision of this ASIC is proved to be better than 20 ps RMS. Power consumption of the chip is about 48 mW at a 2 Gsps sampling rate.
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**Session Classification:** ASIC

**Track Classification:** ASIC
Integration of the CMS Phase 1 Pixel Detector

Wednesday, 13 September 2017 11:55 (25 minutes)

During the extended year-end technical stop 2016/17 the CMS Pixel Detector has been replaced. The new Phase 1 Pixel Detector is designed for a luminosity that could exceed \( L = 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1} \). With one additional layer in the barrel and the forward region of the new detector, combined with the higher hit rates as the LHC luminosity increases, these conditions called for an upgrade of the data acquisition system, which was realised based on the microTCA standard. This contribution focuses on the experiences with integration of the new detector readout and control system and reports on the operational performance of the CMS Pixel detector.

Summary

During the second running period of the LHC (RUN2) it is anticipated that the instantaneous luminosity will reach and exceed \( L = 2 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1} \). The Compact Muon Solenoid (CMS) Phase 0 Pixel Detector and its front-end readout chip were designed for half of this value resulting in increased dead times and random data loss at the expected hit rates. During the extended year-end technical stop 2016/17 the entire CMS Pixel Detector has been replaced. Compared to the old detector the Phase 1 Pixel Detector has one additional layer in the barrel and the forward region. It is built from four layers in the barrel part and three disks at each end.

A new powering layout using DC/DC converters positioned at a high eta value and the switch to a CO2 based cooling system greatly reduced the material budget of the detector in its sensitive region.

The front-end readout chips (ROCs) have either undergone an evolutionary upgrade like the PSI46dig chip used in layer two to four and the forward disks, or have been completely redesigned like the PROC600 used in the first layer of the barrel part.

The switch to a 400Mb/s digital data transmission scheme coming from each of the 2368 optical front-end readout links also called for a complete redesign of the data acquisition system (DAQ). In the new microTCA based DAQ system the front-end controllers and front-end drivers are implemented on the custom made FC7 card equipped with special receiver or transceiver mezzanine cards.

This contribution will give an overview over the design of the Phase 1 CMS Pixel Detector and its new DAQ system, focusing on the integration of the readout system in the scope of the CMS experiment and report on first operational experiences and the overall performance of the new detector.

Primary author:  KORNMAYER, Andreas (CERN)

Presenter:  KORNMAYER, Andreas (CERN)

Session Classification:  Systems, Planning, Installation, Commissioning and Running Experience
Track Classification:  Systems, Planning, Installation, Commissioning and Running Experience
Studies on the Readout of the ATLAS Inner Tracker Using Commercial Networking Hardware

Wednesday, 13 September 2017 17:15 (15 minutes)

In the context of the ATLAS Phase-II upgrade, new front-end electronics is developed, which reads out the detector at higher bandwidth due to finer granularity and higher occupancy. Because of the high bandwidth requirements, new concepts are needed for the ATLAS ITk readout system. A new scalable approach based on many rather simple nodes is proposed to support lab setups, testing sites as well as the readout of large detector parts. This study is focused on the use of COTS networking components to reduce the costs and increase the flexibility of such a system. Results from first studies are presented.

Summary

For the ATLAS Phase-II upgrade, a complete new all-silicon inner tracker is planned, the ITk. ITk will consist of an outer strip-detector and an inner pixel-detector. The pixel detector on its own will consist of around 10,000 detector modules. In combination with a reduced pixel size and at least 10 times higher trigger rate, the needed readout bandwidth is increasing a lot to the order of 100Tbps. Therefore, a new readout system has to be established for ITk.

Also, in preparation for the construction of the new subdetector, smaller systems are needed being able to handle only a handful of modules. To meet all these requirements in a single solution, a new more flexible approach is proposed being based of rather simple nodes in some crate architecture. Our group is working on a concept using ATCA carrier boards equipped with mezzanine cards. These mezzanine cards are planned to be the fundamental building blocks of the system. The detector links are connected to these cards and all the signals to and from the detector are dealt with by a powerful FPGA. Also, the trigger information will be fed through these mezzanine boards. The connection to further off-detector electronics or computers will be realized by network connections. One of the main topics to study will be the throughput of the system from many detector links to the network. There are some fixed latency paths or signals needed in order to trigger and calibrate the detector, these paths need to be implemented and studies as well. To provide a scalable system, small units should be operational stand-alone. This shall be realized by table top setup solutions which do not need any crate infrastructure. The very modular way of construction offers the possibility of very small and rather large system by simply adding mezzanine boards and carrier boards.

As this concept uses commercial network components, development and purchase costs can be reduced and the integration into the readout chain is simplified.

Finally, the system follows the ATLAS TDAQ approach using interface cards between the detector and the network (FELIX). Therefore, the system can provide a beneficial input for developing the final ITk readout system. As the strategy of detector connection is the same, critical topics can be studied and development of firmware and software which is needed for the detector specific operation tasks, as they are calibration and data taking, can be started.

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**Presenter:**  DÜLSEN, Carsten (Bergische Universitaet Wuppertal (DE))

**Session Classification:**  POSTER Session

**Track Classification:**  Programmable Logic, Design Tools and Methods
DRM2: the Readout Board for the ALICE TOF Upgrade

Tuesday, 12 September 2017 09:10 (20 minutes)

For the upgrade of the ALICE TOF electronics, we have designed a new version of the readout board, named DRM2, a card able to read the data coming from the TDC Readout Module boards via VME. A Microsemi Igloo2 FPGA acts as the VME master and interfaces the GBTx link for transmitting data and receiving triggers and a low-jitter clock. Compared to the old board, the DRM2 is able to cope with faster trigger rates and provides a larger data bandwidth towards the DAQ. The measurements on the received clock jitter and data transmission performances in a full crate are given.

Summary

The ALICE Time Of Flight (TOF) detector is a large array of Multi-gap Resistive-Plate Chamber (MRPC) strip detectors for particle identification in the intermediate momentum range at the ALICE experiment (CERN). Each of the 18 sectors is read out by four VME electronic crates, each hosting 9 or 10 TDC Readout Module (TRM) boards and one Data Readout Module (DRM) card. In order to cope with an increase in the trigger rate up to 200 kHz in proton-proton collisions and 50 kHz in lead-lead collisions, we have designed a newer board, named Digital Readout Module 2 (DRM2). The card features a faster link towards the data acquisition system using the GBTx ASIC and VTRx optical transceiver from CERN, which allow a user bandwidth towards the Data Acquisition system (DAQ) of 3.2 Gb/s. The readout will be implemented with synchronous triggers at fixed bunch crossing at 100 KHz, setting a matching window of 10 microseconds in the TDC ASIC installed in the TRMs, the HPTDC. This solution will mimic a full-fledged continuous readout as the one implemented in the new ALICE TPC and ITS readout. The same link is also used for receiving triggers and a low-jitter clock, which is distributed to the front-end electronics. For the TOF detector the quality of this clock is crucial and a campaign of measurements on the clock received from the ALICE data acquisition card named CRU (Common Readout Unit) has been done: we measured a RMS clock jitter as low as O(10) ps, which is compatible with the requirements.

The heart of the board is a Microsemi Igloo2 FPGA, which is a Flash-based device. This device has been chosen since the expected TID (Total Ionizing Dose) for the board (4 meters far from the beam pipe) is 0.13 krad in 10 years, which is acceptable for such a device. The advantage is that the FPGA configuration memory is SEU (Single Event Upset) immune, so that scrubbing is not needed. Upon reception of a trigger, the Igloo2 FPGA drives the VME interface using the VME64x 2eSST feature for reading out the TRM boards at 160 MB/s and packs events towards the GBTx link, which are then sent to the CRU.

The FPGA implements a proprietary 1.25 Gbps serial link from CAEN, named CONET2, which is used for reading temperatures, voltages and for monitoring physics data. The DRM2 board also hosts an Atmel ARM processor running Linux on a commercial piggy-back mezzanine (named A1500 from CAEN), whose purpose is to remotely re-program the Igloo2 FPGA via an Ethernet link when a new firmware revision is released and some other slow-control functionalities.

The paper will present the design details of the DRM2 board, together with the measurement results of the performances obtained working with DAQ cards (CRU and C-RORC), for what concerns
both the received clock quality and the data transmission bandwidth towards the DAQ.

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**Session Classification:**  Programmable Logic, Design Tools and Methods

**Track Classification:**  Programmable Logic, Design Tools and Methods
A 4-channel parallel 56 Gb/s optical receiver for VCSEL-based optical links is presented. The receiver has been manufactured in a standard 65nm-CMOS process. Simulation results with layout parasites and a model of a wire-bonded photo diode demonstrate that the single channel works at bit rate of 14 Gb/s and has an input sensitivity of better than 20 uApp, an input-referred noise of 2.3 uArms and a differential output amplitude across an external 50 ohm load of larger than 400 mVpp. The power consumption is 84 mW/channel for a power supply of 1.2 V. Test results will also be presented in the conference.

Summary

A 4-channel parallel 56 Gbit/s optical receiver is developed in a 65 nm CMOS process because the high data rate is demanded in the particle physics experiments. The receiver is designed for Vertical-Cavity Surface Emitting Laser (VCSEL) based optical links operating at 850 nm wavelength. Each channel consists of a pseudo-differential Transimpedance Amplifier (TIA), a Limiting Amplifier (LA), double Low Pass Filters (LPFs) and an output buffer. A 250 um pitch between channels is designed with the same as an off-chip photo diode array. The receiver modulation current is programmable through an I2C controller with Triple Modular Redundancy (TMR).

The TIA adopts a pseudo-differential structure to improve the power supply rejection ratio and common mode rejection ratio. A pair of CMOS inverters with resistive feedback, one active and one a replica, are used in the TIA. The TIA gain is 200 ohm. With a photo diode DC coupled to the TIA, a 2.47 uArms input-referred noise and a 25 GHz bandwidth is measured in the post-layout simulations. The power consumption of the TIA is around 7.2 mW for a power supply of 1.2 V.

The LA is a 12-stage fully differential amplifier. Interleaving active-feedback structure is adopted in the LA to extend the bandwidth for each stage. The shunt inductive peaking technique is used to extend bandwidth in the last three-stage differential amplifiers of LA at the expense of area. The simulation demonstrates that the LA has a gain of 51 dB and a bandwidth of 13.3 GHz. The LA consumes 57 mW in total for a power supply of 1.2 V.

To compensate the DC offset, double LPFs are used in each channel. The LPFs are single pole RC filters using double 210 kohm resistors and double 4.8 pF miller capacitors. Three-stage differential amplifiers with a 2.4 pF capacitor for the frequency compensation are adopted in the LPFs. The LPFs amplify the difference between the DC levels at the LA output nodes and feed back to a current mirror which generates the current source of the pseudo-differential inverted TIA to compensate the DC offset.

The output buffer driving off-chip transmission line is a differential amplifier with a load resistance of 60 ohm. The bandwidth of the output buffer is 17 GHz with a power consumption of 14.4 mW for a power supply of 1.2 V.

The 4-channel parallel 56 Gbit/s optical receiver for VCSEL-based optical links has been manufactured in a standard 65nm-CMOS process in April 2017. The receiver occupies 1.23 mm × 2 mm chip area. The simulation demonstrates that the single channel works at bit rate of 14 Gb/s, has an input sensitivity of better than 20 uApp, an input-referred noise of 2.3 uArms and a differential output amplitude across an external 50 ohm load of larger than 400 mVpp, and consumes 84 mW/channel.
for a power supply of 1.2 V. We expect to present the measurements in the conference in September 2017.

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**Session Classification:** POSTER Session

**Track Classification:** ASIC
Test Vehicles for CMS HGCAL Readout ASIC

Tuesday, 12 September 2017 15:15 (25 minutes)

For the HGCAL calorimeter upgrade of CMS, two test vehicles were submitted in 2016. They provide the main building blocks of the future ASIC that will read out 50 pF Si-sensors over 10 pC dynamic range. The first test-vehicle features several variants of low-noise, dual-input-polarity current-sensitive preamplifiers. The second test vehicle has eight channels of the full analog-chain: preamplifiers, single-to-differential 25 ns shapers and 11-bit 40MHz SAR-ADC for charge measurement up to 100 fC. A fast discriminator and 50 ps TDC provide Time Over Threshold measurement up to 10 pC as well as Time of Arrival.

Design and measurements of both chips realized in CMOS 130nm will be presented.

Summary

The high granularity silicon tungsten calorimeter (HGCAL) chosen by the CMS collaboration to replace its endcaps for the phase 2 upgrade will provide unprecedented 5D images of electromagnetic showers. The sensors are made of ~1cm² PIN diodes of 100-300 um thickness providing a MIP signal around 1-4 fC. With 6 million channels of low noise, high speed and large dynamic range readout electronics embedded on detector, the front-end ASICs are very challenging and innovative. In particular, the low noise and high gain preamplifier followed by a single-to-differential shaper will provide charge information by being sampled each 25 ns bunch crossing by a 11 bits SAR-ADC. A Time Over Threshold technique (TOT) will provide the charge information for large signals, above 100 fC, when the preamplifier is saturating, using a TDC over 200 ns dynamic range with 50 ps accuracy. The charge data from ADC and TOT will be linearized and stored in a 512 deep-RAM waiting for being selected or not by the L1 trigger. A trigger path will send charge information of summed four channels over 8 bits. The readout electronics will also provide timing information by measuring the Time Of Arrival (TOA) to 25 ps accuracy. The analog power dissipation is below 10 mW/ch and the radiation hardness up to 200 Mrad.

In order to decouple system issues from limitation of each blocks, it has been decided to submit some buildings blocks into test vehicles. Several flavours of DC coupled, low noise, high gain preamplifiers, able to read both polarities input signals, were designed, fabricated in TSMC 130 nm and tested in winter 2016. Then, the full analog channel was also fabricated in an 8-channel test vehicle received in april 2017. The noise performances will be discussed as well as the linearity and stability constrained to input detector capacitance variation. Measurements in charge sensitive and current sensitive modes will be shown as well as the full ADC/TOT performance.

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Session Classification: ASIC
Track Classification: ASIC
The TrainBuilder Data Acquisition System for the European-XFEL

Wednesday, 13 September 2017 17:45 (15 minutes)

The TrainBuilder is an ATCA based data acquisition system developed at the STFC Rutherford Appleton Laboratory to provide readout for each of three Mega-pixel detectors at the European-XFEL Hamburg. Each Train Builder system constructs over 5,000 detector images per second using FPGAs with DDR2 data buffering and an analogue crosspoint switch architecture; thereby processing 10 GBytes/sec of raw image data. The TrainBuilder I/O links operate with 10 Gigabit Ethernet protocols implemented in FPGA logic. The first TrainBuilder was delivered to Eu-XFEL in August 2016 and three are now being used to commission detectors for first X-Ray beams later this year.

Summary

The TrainBuilder is an Advanced Telecom ATCA based custom data acquisition system developed at the STFC Rutherford Appleton Laboratory. It provides a common readout system for Mega-pixel detectors at the European-XFEL (X-Ray Free Electron Laser) facility in Hamburg. Each detector outputs up to 10 GBytes/sec of raw data distributed over multiple 10 Gbps SFP+ optical links. The TrainBuilder system merges detector link image fragments from up to 500 X-ray pulses in each XFEL bunch train every 100 msec using an analogue crosspoint switch and sends the complete detector movies of images to a farm of PCs. The TrainBuilder data links operate with 10GbE IP based protocols implemented in FPGA logic.

The TrainBuilder exploits the regular time structure of the data flow from the XFEL detectors by using a time switched multiplexing architecture to build complete sequences of images from each detector for each bunch train. This is achieved with an input stage comprising of FPGAs receiving data fragments from the detector links which then feed an analogue cross-point switch operating in a barrel shifter pattern at the train repetition rate of 10Hz. The data streams emerging from the switch are collected in an output stage of FPGAs which accumulate the completed movies of images to a farm of PCs. In order to implement the barrel shift architecture deep data buffers are required at the input and output stages. This is achieved in DDR2 memory modules attached to the FPGAs.

Each ATCA crate instruments one Megapixel detector and contains four TrainBuilder I/O boards together with a central TrainBuilder Switch board. Each I/O board has eight 10G SFP+ optical links housed on VITA57 standard pluggable FMC mezzanine cards. The board has four Virtex-5 FPGAs for data processing each of which are attached to dual 2 GByte DDR2 SODIMMs providing the deep data buffering. Dual PowerPC 440 micro-controllers, embedded in the FPGA, are used to manage the DDR2 memory controller DMA engines. An additional static ram QDRII on each FPGA provides off chip memory for image processing.

The Switch board contains a 160x160 way analogue cross-point switch device which can operate at up to 6.5 Gbps. The I/O boards are connected to the Switch via Rear Transition modules using Infiniband standard cables using the Xilinx Aurora serial protocol.

The fast data transmission from the detectors and outputs to the PC farm employs 10GbE UDP/IP based protocols implemented in the FPGA logic. Half the links are configured as inputs receiving image fragments from sub-modules of the detectors and half as outputs sending complete trains of assembled images to the PC farm.
The first complete TrainBuilder crate system was delivered to the European-XFEL in Hamburg in August 2016 and three are now being used to commission detectors before the first X-Ray beams for experiments expected later this year.

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**Session Classification:** POSTER Session

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Results from CHIPIX-FE0, a Small Scale Prototype of a New Generation Pixel Readout ASIC in 65nm CMOS for HL-LHC

Tuesday, 12 September 2017 15:40 (25 minutes)

CHIPIX65-FE0 is a readout ASIC in CMOS 65nm designed by the CHIPIX65 project for a pixel detector at the HL-LHC, consisting of a matrix of 64x64 pixels of dimension 50x50 \(\mu\)m\(^2\). It is fully functional, can work at low thresholds down to 250e\(^-\) and satisfies all the specifications. Results confirm low-noise, fast performance of both the synchronous and asynchronous front-end in a complex digital chip. CHIPIX65-FE0 has been irradiated up to 600 Mrad and is only marginally affected on analog performance. Further irradiation to 1 Grad will be performed. Bump bonding to silicon sensors is now on going and detailed measurements will be presented.

Summary

The HL-LHC accelerator will constitute a new frontier for particle physics after year 2024. One major experimental challenge resides in the inner tracking detectors, measuring particle position: here the dimension of the sensitive area (pixel) has to be scaled down with respect to LHC detectors.

This paper describes the results obtained by CHIPIX65-FE0, a readout ASIC in CMOS 65nm designed by the CHIPIX65 project as small-scale demonstrator for a pixel detector at the HL-LHC. It consists of a matrix of 64x64 pixels of dimension 50x50 \(\mu\)m\(^2\) pixels and contains several pieces that are included in RD53A, a large scale ASIC designed by the RD53 Collaboration: two out of three front-ends (a synchronous and an asynchronous architecture); several building blocks; a (4x4) pixel region digital architecture with central local buffer storage, complying with a 3 GHz/cm\(^2\) hit rate and a 1 MHz trigger rate maintaining a very high efficiency (above 99%). The chip is 100% functional, either running in triggered or trigger-less mode. All building-blocks (DAC, ADC, Band Gap, SER, sLVS-TX/RX) and very front ends are working as expected.

Analog performance shows a remarkably low ENC of 90e\(^-\), a fast-rise time below 25ns and low-power consumption (about 4\(\mu\)A/pixel) in both synchronous and asynchronous front-ends; a very linear behavior of CSA and discriminator. No significant cross talk from digital electronics has been measured, achieving a low threshold of 250e\(^-\). Signal digitization is obtained with a 5b-Time over Threshold technique and is shown to be fairly linear, working well either at 80 MHz or with higher frequencies of 300 MHz obtained with a tunable local oscillator.

Irradiation results up to 600 Mrad at low temperature (-20\(^\circ\)C) show that the chip is still fully functional and analog performance is only marginally degraded. Further irradiation will be performed up to 1 Grad either at low or room temperature, to further understand the level of radiation hardness of CHIPIX65-FE0.

We are now in the process of bump bonding CHIPIX65-FE0 to 3D and possibly planar silicon sensors during spring. Detailed results will be presented in the conference paper.

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**Session Classification:** ASIC

**Track Classification:** ASIC
A Digital Processing Unit of a Highly Integrated Receiver Chip for PMTs in JUNO

Tuesday, 12 September 2017 17:45 (15 minutes)

The Jiangmen Underground Neutrino Observatory (JUNO) is a multi-purpose underground experiment based on a 20,000 ton liquid scintillator with the one main objective to determine the neutrino mass hierarchy. The signal detection is performed by photomultipliers with directly attached readout electronics. The central component for the digitization process is a receiver chip with a low power analog to digital conversion unit and a large dynamic range. The design and prototype measurements of the included data processing unit and regulation circuits are presented. Additionally, the current status of a model of the receiver chain including future regulation possibilities are shown.

Summary

The Jiangmen Underground Neutrino Observatory (JUNO) is an upcoming neutrino detection experiment located in China that aims to determine the neutrino mass hierarchy by detecting reactor antineutrinos from two nearby nuclear power plants. The central detector is a liquid scintillator with a mass of 20,000 ton and is situated with 700 meters rock overburden. It is surrounded by 18,000 20-inch photomultipliers (PMTs) that are designed to detect the produced light with high timing and energy resolutions while being submerged in water. In order to preserve signal quality and reduce the number of cables in the detector, the receiver chain is integrated into the PMT housing.

A highly integrated analog to digital conversion unit (ADU) is developed in 65 nm TSMC CMOS technology with three high performance 8-bit ADCs that have a programmable gain and run in parallel to achieve a large linear voltage input range of more than 80 dB. After digitization and signal processing, the signal is forwarded above water through a 100 meter Ethernet cable. Besides the control of the configuration, data processing is a major task in the receiver chip to reduce subsequent processing efforts. This central data processing unit is included in the receiver chip to judiciously select data from one of the three ADCs and to generate metadata to identify the gain of the ADC during data reconstruction amongst other system events like counter overflows. Parallel processing of four samples reduces the effective clock rate from 1 GHz to 250 MHz resulting in a reduction of the power consumption.

Due to the generated metadata, a certain overhead is created that increases the amount of data above the feasible transmission rate. This is countered by a noise data format used during the absence of a signal, achieving a compression factor of two. The resulting difference is covered by an internal buffer which is designed to cover even the most extreme scenarios of increased data rates that occur during galactic supernova events.

A chip prototype adhering to above said specification was designed and fabricated. The data processor was measured by feeding programmed waveforms through an internal waveform generator in the chip. By this, different possible scenarios were fed to the processor and the functionality was successfully verified. The measurement results of the main data processor show the desired data selection scheme and noise compression and will be presented.

To minimize the error due to baseline drifts caused by inter-symbol interference and biasing fluctuations a digital sigma-delta-based ADC baseline regulator is included in the chip. Due to complex-
ity of the analog blocks there are limitations on the possible simulations to verify the regulator, hence a receiver chain model in a high level description platform (MATLAB) is developed. From this system model, the required parameters are extracted and the ADC baseline offset correction is demonstrated. The system model, the regulator design and the measurement results with the first prototype will be shown.

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**Session Classification:** POSTER Session

**Track Classification:** ASIC
BDTs in the Level 1 Muon Endcap Trigger at CMS

Wednesday, 13 September 2017 17:15 (15 minutes)

The first implementation of Machine Learning inside a Level 1 trigger system at the LHC is presented. The Endcap Muon Track Finder at CMS uses Boosted Decision Trees to infer the momentum of muons based on 25 variables. All combinations of variables represented by $2^{30}$ distinct patterns are evaluated using regression BDTs, whose output is stored in 2 GB look-up tables. These BDTs take advantage of complex correlations between variables, the inhomogeneous magnetic field, and non-linear effects to distinguish high momentum signal muons from the overwhelming low-momentum background. The new algorithm reduced the background rate by a factor of two compared to the previous analytic algorithm, with further improvements foreseen.

Summary

First implementation of Machine Learning in the L1 Trigger at the LHC.

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Session Classification:  POSTER Session

Track Classification:  Trigger
The FEROL40, a MicroTCA Card Interfacing Custom Point-To-Point Links and Standard TCP/IP.

Wednesday, 13 September 2017 16:45 (15 minutes)

In order to accommodate new back-end electronics of upgraded CMS sub-detectors, a new FEROL40 card in the microTCA standard has been developed. The main function of the FEROL40 is to acquire event data over multiple point-to-point serial optical links, provide buffering, perform protocol conversion, and transmit multiple TCP/IP streams (4x 10Gbps) to the Ethernet network of the aggregation layer of the CMS DAQ event builder. The design of the FEROL40 and experience from operation will be discussed.

Summary

The CMS experiment has installed a new Pixel detector during the end of year technical stop 2016-2017. A new custom card (FEROL40) card has been developed to be able to readout the 112 10Gbps links of the new Pixel back-end electronics.

This new microTCA based card is an evolution of the FEROL card developed in 2013 which interfaces the back-end electronics of the sub-detectors to Ethernet networking technology of switches and computing nodes. The input links connecting to the sub-detector back-end electronics are point-to-point serial links using the CMS custom SlinkExpress protocol. The FEROL40 card is based on the microTCA environment with an architecture aimed to achieve a high number of links per card. It is able to aggregate 4 SlinkExpress data streams (up to 10 Gbps), buffer, and transmit the data to the DAQ Ethernet network with an on chip reduced TCP/IP implementation using 4 x 10Gbps Ethernet links. The memory used for TCP socket buffer is based on DDR3 modules with a bandwidth of 100 Gb/s. The FEROL40 can also receive the TCDS (Trigger Control and Distribution System) information (triggers, command) enabling to check the synchronisation of the event fragments coming from each link and to emulate event fragment to test the complete DAQ infrastructure. The software for configuration, control and monitoring can access the FEROL40 on-board resources via a commercial memory mapped PCIe link from the microTCA MCH and a control PC. Experience from operation will be discussed.

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Presenter:  GIGI, Dominique (CERN)

Session Classification:  POSTER Session

Track Classification:  Programmable Logic, Design Tools and Methods
A Combined Versatile Platform for Silicon Strip Hybrids Reliability Assessment

Wednesday, 13 September 2017 09:20 (25 minutes)

A unified platform combining a low noise 64-channel power supply with environmental monitoring and a high data rate transmission system, rated up to 1.2 Gbps/sec, has been developed for commissioning of the ATLAS ITk silicon strip hybrids. The power supply with 10mV peak-to-peak noise, implements 3kV isolation and software control. Humidity, temperature, voltage and current are monitored for all channels through I2C interface. Data paths are organized in a pyramid-like, fully programmable layout, enabling use of 8 LVDS lines for accessing all 64 data inputs. The system has been optimized to fit in a single 6U VME type C crate.

Summary

ATLAS ITk features strip system with 100 million readout channels and several custom ASICs. Burn-in tests are envisioned as a part of hybrid testing procedure in order to catch “infant mortality” of the ASICs. Implementing such tests requires a system providing all available services for DUTs. A multichannel compact architecture is presented, embedding precise low voltage powering, environmental control and data read-out transmission for 64 modules.

An autonomous 1.5V, 10mV peak-to-peak noise power supply is implemented for each channel. The 1.5A max current output in combination with the 3kV isolation provides 50% margin in respect or required power and medical grate protection for the sensitive equipment. Voltage and current are monitored at the receiving end while a passive humidity sensor in combination with a double channel ADC are included. Temperature is monitored through an NTC in conjunction with a precision current source and a configurable gain high precision amplifier directed to the second ADC input. Configuration, remote enable and data readout tough I2C interface is instrumented for each channel individually.

Data transmission is organized in three layers of high speed differential octal switches. Using a pyramidal fully user programmable architecture, the 64 differential inputs can be probed by 8 DAQ lines. The I2C structure configurability, enables any of the inputs to be connected to any of the available output lines while internal use of CML signaling ensures high bandwidth. While internal switching can be achieved up to 2.5Gbps/s, elements related to the LVDS standard limit data rates to 1.2Gbps/s. A universal clock is distributed to all channels while 32 direct differential lines are made available for specific functions. Pre-emphasis and equalization is implemented in all differential switching stages while SLVS to LVDS transceivers are introduced in the final stage of the control lines output. An intricate attention was devoted to noise reduction and signal referencing with single ground paths and high frequency filtering elements.

The system is organized in a single 6U VME crate and comprises of three distant autonomous elements: the individual channel power and environmental boards, power and data transmission mother-boards combining 8 power boards and the backplane, implementing high rate data switching and transmission. To accommodate higher powering requirements, the possibility of combining powering boards is implemented via I2C programming. Although this technique reduces the number of available channels by half, it allows a maximum 3A current per channel. The compactness of the system is enhanced by the single common 12V supply voltage for all elements allowing use of a commercial high power VME power supply. Finally, the integrated FMC connector on the backplane enables the addition of an FPGA daughter board of user choice simplifying integration, upgradability and compatibility with different platforms.

Overall, the high versatility of this combined powering, data transition and monitoring system, in
combination with low electronic noise, precision power supplies and reconfigurable data switching architecture, makes it a characterization platform compatible with any multichannel detector setup. The compact nature and upgradability facilitates integration and provides enhanced design freedom to the end user.

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**Session Classification:** Production, Testing and Reliability

**Track Classification:** Production, Testing and Reliability
**FELIX: the New Detector Readout System for the ATLAS Experiment**

*Tuesday, 12 September 2017 14:50 (25 minutes)*

Starting during the upcoming major LHC shutdown (2019-2021), the ATLAS experiment at CERN will move to the Front-End Link eXchange (FELIX) system as the interface between the data acquisition system and the trigger and detector front-end electronics. FELIX will function as a router between custom serial links and a commodity switch network, which will use industry standard technologies to communicate with data collection and processing components. This presentation will describe the FELIX system design as well as reporting on results of the ongoing development program.

**Summary**

The upcoming ATLAS upgrade program, to be implemented in the next major LHC shutdown (2019-2021), requires a Trigger and Data Acquisition (TDAQ) system able to trigger and record data at luminosities up to three times the original LHC design value. At the same time new on detector electronics technologies will be introduced to ATLAS readout for the new Muon Small Wheel detector, as well as the Liquid Argon (LAr) Calorimeter and Calorimeter Trigger upgrades. These new systems will make use of newer readout link technologies, including high bandwidth FPGA-to-FPGA protocols and radiation-hard Giga Bit Transceivers (GBT), providing up to 42 logical links within one fibre. In order to connect these new systems and handle the significantly increased data volumes in a detector agnostic and easily scalable way a new readout architecture, named the Front-End LInk eXchange (FELIX), has been designed.

FELIX receives and identifies different information streams on its incoming links and routes packets to client processing applications via a commercial switched network. In the opposite direction, FELIX receives packets from the network and forwards them to specific on-detector modules. Another task for FELIX is to handle input from the Time, Trigger and Control (TTC) system to recover the LHC clock and to forward synchronous trigger information to on-detector electronics over low-and-fixed-latency GBT links.

All functions described above are implemented in FPGAs hosted on PCIe interface cards, which are hosted within commodity server PCs. Feature design and subdetector interface testing is taking place using a Xilinx VC-709 development card. The VC-709 is equipped with an 8 lane PCIe Gen3 (64 Gb/s) interface and four SFP+ transceivers for optical connectivity. A custom FMC mezzanine has been designed to receive and decode the TTC clock and information stream and provide clock jitter cleaning. Drivers and software tools have been developed to test and configure these boards both for internal development purposes and use in subdetector test systems. Data routing and connectivity to a COTS (Commercial Off-The-Shelf) network is implemented in a software pipeline running on the FELIX host PC. It has been verified the packet processing performance of the design satisfies ATLAS readout requirements for 2021.

The final implementation of FELIX will make use of a custom built PCIe board with a Xilinx Kintex UltraScale FPGA, a 16 lane Gen3 PCIe interface and 48 bidirectional optical interfaces in the form of eight Mini-POD transceivers (max. link speed 14 Gb/s). The optical links, PCIe interface, and TTC decoding circuits of the prototypes of this board have been verified to function well. Integration testing with the complete FELIX firmware and software is ongoing. In this presentation the FELIX system will first be introduced, before further details are given of ongoing development and performance testing.
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Session Classification:  Trigger
Track Classification:  Trigger
Development of the Readout System for Triple-GEM Detectors for the CMS Forward Muon Upgrade

Wednesday, 13 September 2017 11:30 (25 minutes)

We present the readout system being designed for triple-GEM detectors to be installed in 2019-2020 in the CMS muon endcap for HL-LHC. Beginning of 2017, 10 triple-GEMs have been installed in CMS. These detectors are read-out with the VFAT2 chip while its next version, the VFAT3, is under characterization. The rest of the readout system is very similar between the 2017 and the final version: on-detector FPGA board with GBTx and SCA, Versatile link and microTCA backend (CTP7). We will report on the first experience in CMS with VFAT2s as well as the status of the final system design.

Summary

In this contribution we will present the readout system being designed for triple-GEM detectors that should be installed in 2019-2020 in the CMS muon endcap system for the LHC high luminosity phase. Beginning of 2017, 10 triple-GEM detectors have been for the first time installed in CMS. These detectors are read-out with the VFAT2 chip while the next version of the chip, the VFAT3, is under characterization. The rest of the readout system is very similar between the 2017 and the final version: GEM Electronic Board (GEB), Opto-Hybrid board with on-detector FPGA, GBTx, SCA, Versatile link and micro-TCA backend (AMC13 and CTP7). We will report on the first experience in CMS with VFAT2s as well as the status of the final system design around the VFAT3.

The CMS triple-GEM has a trapezoidal shape, equipped with 1D readout, with dimensions 990 x 440-220 mm2. The readout strips are segmented in 24 sectors: 3 sectors along the azimuthal coordinate spanning 10° in φ x 8 sectors along the pseudo-rapidity (1.5<|η|<2.2). Each sector consists of 128 anode strips read-out by a new front-end chip being designed, the VFAT3. The readout system being designed takes full advantage of current generic developments introduced for the LHC upgrades; it is based on the use of CTP7 AMC boards host in micro-TCA crates for the off-detector electronics and the Versatile Link with the GBT chipset to link the front-end electronics to the micro-TCA boards. In addition the CMS AMC13 micro-TCA board will be used to interface the back-end electronics to the central CMS DAQ system. Finally the FEAST DC-DC converters are used to power the on-detector electronics.

In addition a few hardware components have to be developed specifically for this project: the GEM Electronic Board (GEB) and the Opto-Hybrid board. The GEB consists in a large multi-layer PCB board, matching the size of the Triple-GEM detector. The Opto-Hybrid is a small (typically 10 x 20 cm2) mezzanine, mounted on the center of the GEB, equipped with a Xilinx Virtex6 FPGA and the GBT chipsets. The Opto-Hybrid will collect the trigger and tracking data from the 24 VFAT3 chips and ensure the sparcification and the formatting of these data for the optical links. The data are transmitted from the VFAT3s to the Opto-hybrid through the GEB PCB at 320 MHz.

In January 2017 10 triple-GEM detectors equipped with the VFAT2 FE chips have been installed in CMS. In this contribution we will report on the lessons learned and on the first results gathered with this new system in CMS. Together with the characterization of the new VFAT3 chip, which started in March 2017, these results are very valuable to finalize the design for the final system. First results from the VFAT3 characterization and the status of the final CMS Triple-GEM readout system design will also be reported.
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Session Classification: Systems, Planning, Installation, Commissioning and Running Experience

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience
Demonstrating TTC-PON Robustness and Flexibility

Wednesday, 13 September 2017 11:05 (25 minutes)

In 2016, a TTC-PON (Timing, Trigger and Control system based on Passive Optical Networks) demonstrator was presented at TWEPP as an alternative to replace the TTC system, currently responsible for delivering timing, trigger and control commands in the LHC experiments. Towards a deployment foreseen for ALICE phase-1 upgrade, the system has been consolidated through flexible software implementation providing full configuration, complete calibration and extended monitoring and diagnostic tools. A scaled-up setup was built with various FPGA platforms to stress the system in realistic conditions. The system and its features will be demonstrated together with a discussion on its robustness.

Summary

The TTC-PON system (Timing, Trigger and Control system based in Passive Optical Networks) was first envisaged in 2010 as an alternative to the current TTC system, responsible for timing distribution, and for sending level-1 trigger accept and control commands from the central trigger unit to the detector sub-partitions of the CERN LHC (Large Hadron Collider) experiments. TTC-PON is a bidirectional point-to-multipoint optical communication system in which a master node can communicate with slave nodes over the same fiber using WDM (Wavelength Division Multiplexing) and TDMA (Time Division Multiplexing Access). Compared to the current TTC system, TTC-PON has a much higher bandwidth and allows bidirectional optical communication between the master and slaves. In addition, TTC-PON masters can serve more slave nodes (up to 64) when compared to the current system (up to 32).

Since the TTC-PON will be installed in the back-end of the experiments, COTS (commercial off-the-self) optical components and FPGAs (Field Programmable Gate Arrays) are used for the system implementation. In 2016, a demonstrator based on the XGPON1 technology was presented overcoming major limitations of past solutions. The system can handle up to 64 slave nodes per master with a comfortable optical margin and the TDMA is based on 125 ns timing slots allocated to each slave. This demonstrator was based on a single manufacturer for the optical components and all the nodes of the system were implemented using Kintex7 FPGAs by means of KC705 evaluation boards (Xilinx).

Since then, the FPGA firmware has been consolidated and is being prepared for a full deployment in the framework of ALICE phase-1 upgrade. The proposed system is now fully software configurable with a very flexible design based on Python; several features have been made available to the users in order to have full configuration and calibration procedures and extended online and offline monitoring tools of the system. An improved setup consisting of one master and eight slaves has been built. Based on Kintex Ultrascale and Arria 10 development platforms, as well as on PON transceivers from several vendors, this new test bench allowed to perform stress tests (extended bit error ratio tests, temperature, long fibers, dynamic range...) in order to better understand system limitations and to improve its robustness.

This paper will focus on the current core design and a demonstration of its features will be performed. The system stress tests results and the robustness of the current setup will also be discussed.
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**Session Classification:** Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Effect of Gamma Irradiation on Leakage Current in CMOS Readout Chips for the ATLAS Upgrade Silicon Strip Tracker at the HL-LHC

Monday, 11 September 2017 15:15 (25 minutes)

As part of the program for the upgrade of the ATLAS inner tracker for the High Luminosity LHC, irradiations have been carried out with 60Co gamma source. The measurements characterize the increase in the leakage current in the 130 nm-technology readout chips. The current as a function of total ionizing dose has been studied under different conditions: dose rate, temperature, power applied to the chip and pre-irradiation. The results show unique features that provide valuable information for the understanding of the mechanisms responsible for radiation damage in transistors. Models that attempt to parameterize the leakage current will also be presented.

Summary

The increase of the leakage current of NMOS transistors in certain 130 nm CMOS technologies during exposure to ionizing radiation needs special consideration in the design of detector systems, as this can result in large increases in current and power dissipation. As part of the R&D program for the upgrade of the ATLAS inner tracker for the High Luminosity upgrade of the LHC at the CERN laboratory, a dedicated set of irradiations has been carried out with the 60Co gamma source at the Brookhaven National Laboratory. Measurements will be presented that characterize the increase in the digital leakage current in the 130 nm-technology ABC130 readout chips, as observed by other experiments. The variations of the current as a function of time and total ionizing dose have been studied under different conditions, such as dose rate, temperature and power applied to the chip. The ranges of variation of dose rates and temperatures have been set to be as close as possible to those expected at the High Luminosity LHC, i.e. in the range 0.6 krad/h - 2.5 krad/h and between -10 ℃ and +10 ℃. Some of the chips under test were pre-irradiated with high doses of X-rays at Rutherford Appleton Laboratory, i.e. at a total dose of 8.5 Mrad and dose rate of 0.85 Mrad/h, in order to study the different effect of radiation on un- and pre-irradiated devices.

The results of this irradiation campaign reproduce the general observations by other experiments, however some unique features have been observed. Specifically, it has been observed an increase of the digital leakage current that peaks at values that are 1.2 - 2.7 times the baseline value (i.e. before irradiation), and both current peak value and current peak time depend on the dose rate. In order to study the dependence of the leakage current on temperature, temperature conditions were changed during operations. No changes in current have been observed when the temperature is raised from -10 ℃ to +10 ℃ after the current peak is reached. In order to study the effect of voltage bias on transistors, the chip power was turned off during irradiation. It has been observed that the current slowly resumes to the expected general trend once the power is applied again after a few days of interruption. Furthermore, It has also been found that pre-irradiated chips show no increase in digital leakage current up to a few Mrad of total ionizing dose, differently from chips that were not pre-irradiated. These results can provide valuable information for the understanding of the underlying mechanisms responsible for radiation damage in transistors and detector readout chips.

Models that attempt to parameterize the leakage current under different environmental conditions and how they fit to experimental data will also be presented.
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Session Classification:  Radiation Tolerant Components and Systems

Track Classification:  Radiation Tolerant Components and Systems
Integration of Intelligence and Redundancy Elements into the FPGA-Based DAQ of the COMPASS Experiment

Wednesday, 13 September 2017 12:20 (25 minutes)

Using FPGA technology for event building tasks in high-energy physics experiments reduces costs and increases reliability of DAQ systems. In 2014, the COMPASS experiment at CERN’s SPS commissioned a novel, intelligent, FPGA-based DAQ (iFDAQ) in which event building is entirely performed by FPGA cards. The highly scalable system is designed to cope with an on-spill data rate of 1.5 GB/s and a sustained data rate of 500 MB/s. Its intelligent and highly reliable hardware event builder is able to handle and detect front-end errors and automatically take corrective action. The contribution will give an overview of system details, performance, and running experience.

Summary

Driven by the need of a highly scalable and high-performance computing architecture for data acquisition, the COMPASS experiment at CERN’s Super Proton Synchrotron (SPS) developed a new Data Acquisition System (DAQ) from scratch using a novel approach to the event building network. The new system and its event builder exploit the application-optimized computation technology of Field Programmable Gate Arrays (FPGAs). In contrast to traditional event builders which base on distributed online computers interconnected via an Ethernet Gigabit network, the event building task is solely executed in hardware. Recent developments in FPGA technology, such as increased I/O bandwidth (> 3 Gbps) and support for high-performance SDRAMs even on low-cost chips, made FPGAs suitable for event building purposes. Reduced costs, higher reliability, and increased compactness are the arguments to move from traditional to FPGA-based event builders in future.

COMPASS commissioned its intelligent, FPGA-based DAQ (iFDAQ) in 2014, when a reduced spectrometer required only a reduced event builder. During the following years, the system was extended and features were added. In 2017, the system will be deployed in its full scale and it will be able to cope with the expected on-spill data rate of 1.5 GB/s.

By buffering data on different levels, the iFDAQ exploits the spill structure of the SPS beam and averages the on-spill data rate over the whole SPS duty cycle to a sustained rate of 500 MB/s. The system uses a hybrid FPGA-software approach. The event building task is entirely performed by FPGAs, whereas the software is responsible for system control, user interfaces, configuration, and monitoring. The hardware event builder consists of multipurpose, custom designed FPGA-cards. These cards are equipped with 4 GB of DDR3 memory and 16 high-speed links. The event builder receives data from the front-end electronics via approximately 100 optical serial interfaces. It buffers and multiplexes data, combines event fragments to complete events, and finally distributes them to eight readout computers via FPGA PCIe cards. All hardware nodes are synchronized by the Trigger Control System (TCS). Monitoring and control of the hardware nodes is possible via a dedicated Ethernet network using IPbus protocol. Using three independent interfaces for slow control (IPbus), synchronization (TCS), and data flow (SLINK) increases the robustness of the system.

Built-in intelligence allows to dynamically react on faulty front-end modules. In order to ensure system stability and data integrity, too high data rate is throttled and wrongly formatted or missing data is replaced by empty but correct frames. Moreover, a steady data stream enables the
system to continuously check the status of frontend modules and automatically point the user to problematic equipment.

From 2017, all involved point-to-point high-speed links between front-end electronics, the hardware event builder, and the readout computers are wired via a fully programmable crosspoint switch. This allows the user to remotely customize the network and hence simplifies compensation for hardware failure and optimization for load balancing. In a second step, the intelligent hardware will recognize load imbalance and malfunctioning hardware nodes by itself and will automatically take appropriate actions.

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**Session Classification:** Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
A SEU Tolerant Latches Study for the RD53A Chip

Abstract:
The RD53 collaboration was established to develop the next generation of pixel readout chips needed by ATLAS and CMS at the HL-LHC and requiring extreme rate and radiation tolerance. The 65 nm CMOS process is adopted in order to satisfy the high level of integration requirement. The SEU immunity for this highly scaled process should be carefully considered because the device dimensions are small and the capacitance of the storage nodes becomes very low. A chip prototype including different SEU tolerant structures was designed in the TSMC 65nm technology and proton irradiation tests were done in order to estimate the SEU tolerance of the proposed structures.

Summary
The 65 nm CMOS process is a promising technology for the pixel readout chips at HL-LHC in terms of high integration density and a first 65 nm demonstrator chip containing 76 800 pixels of 50µm × 50 µm will be submitted during the summer 2017. Simulations show that the innermost parts of the new pixel detector will integrate a fluence of about 2.1016 n/cm² (1 MeV neutron equivalent) corresponding to a Total Ionizing Dose (TID) of 1Grad equivalent of 10 years of exploitation. Irradiation studies were done in order to estimate the TID tolerance of the 65nm process and design rules were followed for digital and analog blocks to ensure good functionality in these aggressive operating conditions. The flux of particles producing Single Event Upset (SEU) in the pixel barrel layer 0 (at approximately 3.7 cm) is estimated to be 0.5 10⁹/cm²/s. The cross section of the foundry latches is estimated by measurements to 3.10⁻¹⁴ cm²/bit which indicates that the mean time between 2 errors for the pixel configuration in each readout chip is around 50 ms. In order to optimize the immunity of the latches against SEU, a chip prototype integrating 2 different main flavors of SEU tolerant cells have been designed in 65nm technology and have been tested using a 24 GeV proton beam.

The first studied structure is the DICE latch (Dual Interlocked CEll) based on the redundancy of the storage node. The main drawback of this structure concerns the sensitivity of the charge sharing effect which appears on 2 nodes identified like critical. These nodes can be isolated and separated spatially by using an interleaved layout technic. Measurements show an improvement of SEU tolerance by a factor of 10 with respect to the single latch. A layout of 8 bits configuration memory block was done to be implemented as a pixel configuration memory inside the readout chip. The size of such a block represents only 4% of the whole pixel area.

The second type of latch is a Triple Redundant Latch (TRL) cell including a self correction error. Particular attention has been paid to the combinatorial logic controlling each single latch of the TRL and the global nodes were triplicated in order to prevent the transient errors occurring in the control logic to be propagated to the latches. Measurements of this structure show that the TRL latch allows an improvement of the SEU tolerance by a factor 3600 with respect to the single latch. However, it consumes a rather large area and can not be implemented inside the pixel. It can nevertheless be used in the chip periphery where it increases the SEU-hardness quite drastically.

In the pixel chip prototype, the TRL is used in the digital chip bottom and the synthesis tool is constrained to separate sufficiently sensitive nodes. Recently, a new 65nm SEU prototype has been submitted in order to study the effect of the Deep
NWell, used in this process, on the SEU tolerance.

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**Session Classification:** Radiation Tolerant Components and Systems

**Track Classification:** Radiation Tolerant Components and Systems
Functionality and Performance of the ALFA_CTPIN Module

Wednesday, 13 September 2017 17:00 (15 minutes)

During first long stoppage (LS1) of the LHC, the Central Trigger Processor (CTP) of the ATLAS experiment has been upgraded. In addition to enriched functionality, it resulted in increasing the CTP input-output latency by 75 ns (3 cycles@40 MHz). The ALFA triggers were no longer early enough to contribute to the global ATLAS triggering. A dedicated input board, speeding up the ALFA signal processing and providing advanced monitoring of the ALFA trigger signals, has been therefore required.

The ALFA_CTPIN module has been designed to deliver requested functionality. In this text, we will give description of it and present achieved performance.

Summary

The ALFA_CTPIN module has been designed in VME standard. To its inputs it receives the LHC clock and orbit synchronising signals from the CTP (40 MHz and 11 kHz, respectively) and up to 16 trigger signals from ALFA detector stations. From its outputs it drives ALFA triggers to the CTP.

The whole functionality of the ALFA_CTPIN has been implemented in two FPGA chips present on the motherboard. The module’s logic consists of the following functional blocks: Trigger-Decoder, Trigger-Processing Unit, Rate-Counters Unit, Test-Pattern Generator, Phase-Measurement Unit and VME Interface.

The Trigger-Decoder processes trigger signals coming from ALFA detector stations. Each detector station sends to the ALFA_CTPIN module encoded trigger signals coming either from the Main-Detector (MD) or the Overlap-Detector (OD). The Trigger-Decoder detects the trigger type and produces on its MD or OD outputs unique trigger pulses driven directly to the ATLAS CTP module. The latency of trigger detection is 50 ns (4 cycles@80 MHz) while the introduced dead-time is 75 ns which is still inside 100 ns dead-time of the ALFA detector itself.

The MD and OD triggers are also made available internally to the Trigger-Processing Unit for further processing. The MD and OD outputs from the Trigger-Decoder form four 8-bit wide vectors used for addressing individual Look-Up-Tables (LUTs) which produce 128-bit wide data on their outputs. This output data then passes through a combinatorial stage were bit-masking, AND or OR operations are applied to produce final values of 128 trigger items. Bit-masking contents as well as combinatorial function selection is pre-settable individually to each trigger item via VME. The latency of trigger processing is 25 ns (1 cycle@40 MHz).

Such processed trigger items feed the Scalers Unit to measure their rates. There are two type of scalers: Simple and BC ones. While the Simple scalers measure the aggregate rate, the BC ones measure the rate per specific LHC bunch number (BC). There are 128 Simple scalers and 26 BC ones, both scaler types sum the trigger items’ counts over either 1 or 10 seconds.

For commissioning and testing purposes, the Phase-Measurement Unit and Test-Pattern Generator have been implemented in the module’s logic.

The Phase-Measurement Unit measures the interval between leading edges of incoming ALFA trigger signals and the main clock of the module, respectively. The resolution of this measurement is 2.5 ns.

The Test-Pattern Generator allows to generate internally any ALFA triggers’ patterns which may
arrive to all inputs of the module within one orbit signal of the LHC. The patterns can be generated for specific number of cycles or as long as they’re enabled.

A dedicated, standalone software has been developed to create and verify the logic for the trigger items. The configuration of the module and access to rates of the trigger items uses ATLAS TDAQ software. The module is configured and controlled by the RCD application. Every 1.3 sec the scalers from the module are readout using the VME interface. The collected data are then published either as raw numbers or in form of histograms.

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**Session Classification:** POSTER Session

**Track Classification:** Trigger
Serial Powering Optimization for CMS and ATLAS Pixel Detectors within RD53 Collaboration for HL-LHC: System Level Simulations and Testing

Thursday, 14 September 2017 15:15 (25 minutes)

Serial powering is the baseline choice for low mass power distribution for the CMS and ATLAS HL-LHC pixel detectors. For this scheme, two 2.0A Shunt-LDO (SLDO) regulators are integrated in the RD53 prototype chip (65 nm) and are used to provide constant supply voltages to its power domains from a constant input current. System level simulation studies will be presented, in which a detailed regulator design in serially powered topology is used to evaluate and optimize system parameters for different operational scenarios of HL-LHC pixel detectors. Performance results from testing prototype SLDO chips will be shown, including x-ray irradiation.

Summary

Serial powering has been identified as the baseline low mass choice for powering the CMS and ATLAS pixel detectors in the HL-LHC era. The very large number of pixels, the high hit and trigger rates required designing a new chip in 65 nm CMOS technology within RD53 collaboration. Such a chip would require current levels of ~2.0 A under normal operating conditions. In a serially powered topology, pixel detector modules would be serially powered and each of those would be composed of up to four chips powered in parallel. Consequently, each current chain could require up to 8.0 A, including extra headroom to comply with fast dynamic current variations of the digital logic of the chip.

A serial powering scheme, based on a constant current supply, is possible by integrating an on-chip shunt-LDO regulator (SLDO) for each of the power domains of the chip (analog and digital). The SLDO concept, firstly introduced in FE-I4 chips (130 nm), combines a Low Drop-out (LDO) regulator with a shunt. Therefore, any excess of current injected in the serial power chain can be shunted, while the linear regulator part of the SLDOs provides independently the required voltage to the analog and digital power domains of the chip.

The SLDO has been redesigned in 65 nm and it is able to carry up to 2.0 A. The resistive behavior of the SLDO allows for the operation of multiple SLDOs in parallel, with well-defined current sharing, determined by their effective resistance, which is configurable. Another important novel SLDO feature is a configurable voltage, which allows an optimization of the power consumption in case of a failure of a chip in a module.

System simulations for a serial power system for the configuration of the CMS pixel detector have been used to study the performance of the SLDO under various operating conditions. The simulation was based on the SLDO 2.0A regulator detailed design, with serially powered pixel modules, each consisted of either two or four pixel chips powered in parallel. The dynamic profiling of both digital and analog power, failures and power up scenarios have been simulated to understand and optimize the parameters for stable operation of a serially powered system. The coupling of digital noise to the analog domain and vice versa has also been evaluated to be within the acceptable levels and the amount of extra shunt current needed for reliable, yet efficient, operation of the front-ends chips has been optimized.

In addition, a 2.0A SLDO prototype chip has been tested in serially powered mode, where its characteristics have been investigated e.g. the effective resistance, the use of the configurable voltage and the coupling of the noise of chips operated in parallel and in series. Finally, Xray
irradiation of the test-chips demonstrated radiation hardness of up to 500 Mrad without significant impact on their performance.

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**Session Classification:** Power, Grounding and Shielding

**Track Classification:** Power, Grounding and Shielding
The End-Of-Substructure Card (EoS) is the interface between the building block of the ITk Strip Tracker and the outside world. All the control and command signals, the data and the power will be passing through it. The card concept is built around using the lpGBT chip set and the VTRx optical link. The EoS will handle up to 28 640 MBit data links and 10 GBit Downlinks and Uplinks. It will be powered using a two-stage DCDC converter system. A first prototype was developed using the GBTx chipset, supporting link speeds up to 5 Gbit. We present first performance measurements of the system including the performance of the DCDC system.

Summary

The End-Of-Substructure Card (EoS) is the interface between the building block of the ITk Strip Tracker (staves and petals) and the outside world. In the ITk the modules consisting of the silicon sensor itself and the hybrids with the readout ASICS are placed on a common structure called a stave (in the barrel) and petal (in the end-cap). All module use a common bus-tape co-cured to carbon-fiber based structure to distribute power and signals. The data lines and command lines are then connected from the bus-tape to EoS. The power, both low and high voltage, are also distributed via the bus tape and connected to the EoS. All these connections will be made using wire-bonds. The card concept is build around using the lpGBT chip set and the VTRx optical link, both common developments for the LHC Upgrades. The command signals will be coming in on a 10 Gbit/s link and will be de-multiplexed by the lpGBT and send to the stave/petal. The incoming data from the sensor, which depending on the type of stave or petal will be up to 28 lines, will be at a rate of 640 Mbit/s and be then multiplexed by one or two lpGBTs into 10 Gbit/s data links. The conversion from electrical to/from optical will be handled by the Vtrplus chips set. All the power lines including sense wires will be going through the EoS. The LV lines will be rated for 12 V and the HV lines for 750 volts. The EoS itself will be powered using the 12 V and generate 2.5 and 1.2 V using a DCDC converter system using the upFeast and DCDC2s chips currently developed at CERN.

As a first prototype for the Stave2017 program an EoS has been designed and manufactured using the GBTx/VTRx chipset, which supports link speeds up to 5 Gbit. We present first performance measurements of the system including the performance of the DCDC system.

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Session Classification: POSTER Session

Track Classification: Radiation Tolerant Components and Systems
Radiation Hard GaNFET High Voltage Multiplexing (HV-Mux) for the ATLAS Upgrade Silicon Strip Tracker

The outer radii of the inner tracker (ITk) for the Phase-II Upgrade of the ATLAS experiment will consist of groups of silicon strip sensors mounted on common support structures. Lack of space creates a need to remotely disable a failing sensor from the common HV bus. We have developed circuitry consisting of a GaNFET transistor and a HV Multiplier circuit to disable a failed sensor. We will present two variants of the HV Mux circuitry and show irradiation results on individual components with an emphasis on the GaNFET results. We will also discuss the reliability of the HV Mux circuitry and show plans to ensure reliability during production.

Summary

To increase the physics reach of the Large Hadron Collider (LHC) a major upgrade of the collider, known as the High Luminosity LHC (HL-LHC) is planned to be operational around 2026. The ATLAS detector will need to undergo major upgrades to cope with the increased luminosity. One of the major upgrades is the Inner Tracker (ITk), which will be an all-silicon detector consisting of pixel detectors at the inner radii and silicon strip sensors in the outer radii.

The silicon strip detector will be fabricated from staves in the barrel region and petals in the end-cap regions. They consist of multiple silicon sensors mounted on a common thermal-mechanical support and cooling structure. Due to a drive to reduce material and a lack of space, it will not be possible to bring individual high voltage bias to each sensor. Groups of sensors will need to share a common high voltage bias. Should a sensor fail due to its developing a low breakdown voltage or a short, other working sensors will also be lost.

We began a program to develop a method to disconnect a malfunctioning sensor from the HV bias bus. The main requirements on the high voltage multiplexing circuitry (HV Mux) is that it be capable of switching -500 V, operate in a 2 Tesla magnetic field, and survive fluences of 2 x 10^{15} hadrons/cm^2 and ionizing doses ~ 50 Mrad.

We initially focused on two emerging technologies, Gallium Nitride and Silicon Carbide, for an HV switch that could potentially be radiation hard. Additionally, we considered a unique design using 3D Trench technology for a custom JFET. We have concluded that only Gallium Nitride technology is capable of meeting our radiation requirements.

We will report on an extensive irradiation campaign on a variety of Gallium Nitride Field-Effect Transistors (GaNFETs) that have survived doses as high as 1 x 10^{16} neutrons/cm^2 and over 200 Mrad. Results from irradiations with neutrons, protons, pions, and gamma rays will be presented. We have developed an HV Multiplier circuit that controls the state of the GaNFET. The multiplier circuit accepts a -50 kHz square wave from a radiation hard ASIC operating at 2.5V and generates a gate-source voltage of several volts but offset by the bias voltage to the sensor (as much as -500 V). The components of the HV Multiplier circuit must meet the radiation hardness requirements of the GaNFET. We will report on their radiation hardness and demonstrate that we believe we have developed an HV Multiplier circuit that is sufficiently radiation hard. We have developed a dual-stage variation of the HV Mux circuit than can operate at -700 V or even lower. The introduction of such circuitry should not introduce more failures or loss of sensor operation.
due to HV Mux circuitry failure than if the HV Mux circuitry was not implemented and we instead rely on low rates of sensor failures. We will present a risk analysis demonstrating the tradeoffs of implementing HV Mux vs not implementing. We will present our plans to ensure the reliability of the HV Mux circuitry in our continuing R&D phase as well as during production.

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**Session Classification:** Radiation Tolerant Components and Systems

**Track Classification:** Radiation Tolerant Components and Systems
Development of 4 × 28-Gbps and 4 × 14-Gbps VCSEL Array Drivers in 65 nm CMOS for HEP Applications

Tuesday, 12 September 2017 17:45 (15 minutes)

We present designs and test results of two radiation-tolerant VCSEL array driver ASICs fabricated in 65 nm CMOS technology, VLAD28 and VLAD14. VLAD28 is a 4 × 28-Gbps driver, delivering 2 mA bias and 5 mA modulation currents with a power consumption of 90 mW/ch. VLAD14 is a low-power 4 × 14-Gbps driver, delivering 2 mA and 6 mA modulation with a power consumption of 44 mW/ch. The two drivers have respective innovative structures in the output stage for high-speed and low-power operation. Full-channel optical tests will be carried out in the summer and the results will be reported at the workshop.

Summary

VCSEL-based, high-speed, low-power, radiation-tolerant short-range optical data links are in high demand for detector data transmission in the LHC upgrades as well as in other physics detector developments. VCSEL array driver ASICs are the key components in the optical links. Last year we presented two designs of 10-Gbps/ch VCSEL array drivers in 65 nm CMOS technology. As an evolution of the development, we will report on further research and design in 65 nm CMOS technology: a high-speed 4 × 28-Gbps/ch VCSEL array driver (VLAD28) and a low-power 4 × 14-Gbps/ch VCSEL array driver (VLAD14).

Each channel in both VLAD28 and VLAD14 consists of an equalizer stage (1.2 V), a four-stage pre-driver (1.2 V) and an output driver (1.2 V, 2.5 V). The equalizer stage is an amplifier with a 3-bit configurable RC degeneration to provide appropriate frequency peaking in 28-Gbps/ch and 14-Gbps/ch applications. It compensates the input high-frequency loss in PCB traces and especially due to bonding wires when the data rate goes up to 28-Gbps/ch. The four-stage pre-drivers in the VLAD28 and the VLAD 14 both adopt the shared inductor structure to enable peaking in the four stages by using only two inductors.

The output driver of VLAD28 is based on the last year’s design with the bandwidth boosted by a feed-forward capacitor. We propose on-chip AC-coupling between the pre-driver and the output driver to isolate the two power domains, and adopt a stacked tail-current source in the output stage to ensure the safety of the thin oxide MOS transistors in differential pair. Hence, the cascode NMOS, used at the output branch to sustain the output DC voltage of 1.8 V (due to the VCSEL forward voltage), can be removed to improve the bandwidth effectively by reducing the output capacitance and eliminating the cut-off recovery of the MOS. The output driver of VLAD14 is a new design. It features a novel PMOS current mirror as the load of the differential MOS without bandwidth degradation, so that the current at the output branch could be – Imod ~ Imod, instead of the 0 ~ Imod in the regular design. The modulation efficiency is improved from the structure level in VLAD14.

Both VLAD28 die and VLAD14 die have a size of 2000 µm × 1230 µm. They receive 200 mVp-p differential CML signals as inputs. In the default settings, VLAD28 outputs a 2 mA bias current and a 5 mA modulation current at 28 Gbps/ch with the power consumption of 90 mW/ch, and VLAD14 outputs a 2 mA bias current and a 6 mA modulation current at 14 Gbps/ch with the power consumption of 44 mW/ch. Both designs have been submitted for fabrication in February, 2017, and are expected to be tested electrically and optically during the summer of 2017. The full-channel optical link tests will be conducted, and the results will be reported in the conference.
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Presenter: Dr GUO, Di (Southern Methodist University (US))

Session Classification: POSTER Session

Track Classification: ASIC
A High Luminosity LHC Track Trigger for the CMS Detector

Tuesday, 12 September 2017 15:15 (25 minutes)

During the High Luminosity LHC, to maintain a manageable trigger rate and achieve its physics goals, the CMS detector will need charged particle tracking at the hardware trigger level. The tracklet approach is a track-finding algorithm based on a road-search algorithm that has been implemented on commercially available FPGA technology. This algorithm has achieved high performance in track-finding and completes tracking within 3.4 μs on a Xilinx Virtex-7 FPGA. An overview of the algorithm and its implementation on an FPGA are discussed and the results of an end-to-end demonstrator system that meets timing and performance requirements are presented.

Summary

The upgrades of the Compact Muon Solenoid particle physics experiment at CERN’s Large Hadron Collider provide a major challenge for the real-time collision data selection. We present a novel approach to pattern recognition and charged particle trajectory reconstruction using an all-FPGA solution. The challenges include a large input data rate of about 20 to 40 Tbps, processing a new batch of input data every 25-ns, each consisting of about 10,000 precise pairs of position measurements of particles ('stubs'), perform the pattern recognition on these stubs to find the trajectories, and produce the list of parameters describing these trajectories within 4-μs. A proposed solution to this problem is described, in particular, the implementation of the pattern recognition and particle trajectory determination using an all-FPGA system. The results of an end-to-end demonstrator system based on Xilinx Virtex-7 FPGAs that meets timing and performance requirements are presented. This is presented on behalf of the CMS Collaboration.

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Presenter: Prof. WINER, Brian (The Ohio State University)

Session Classification: Trigger

Track Classification: Trigger
A 3.2 Gbps Serial Link Transmitter for CMOS Pixel Sensors in 0.18 µm CMOS Technology

We present a serial link transmitter designed for CMOS pixel sensors in a 0.18 µm CMOS Technology. The transmitter includes a digital interface block with Reed-Solomon encoder, a Phase-Locked Loop (PLL), a serializer and a Current Mode Logic (CML) driver with pre-emphasis. Functionalities of the transmitter is verified by simulation, consuming 174 mW from a 1.8 V power supply. The transmitter aims to be integrated into a CMOS sensor chip, but this first prototype will be fabricated standalone in this May. We will report the measurement results in the final paper.

Summary

Numerous future subatomic physics experiments demand CMOS pixel sensors with high-speed serial data links due to the increasing hit density, low material budget requirements. A serial data link meets requirement of this application due to its saving cables/connectors and high reliability in contrast to a parallel data link. We present a serial link transmitter designed for CMOS pixel sensors in a 0.18 µm CMOS Technology. The transmitter encodes the received pixel data with Reed-Solomon correction algorithm and send data in serial at 3.2 Gbps. The transmitter includes a PLL for clock generation, a digital interface block with Reed-Solomon encoder, a serializer and a CML driver with pre-emphasis. The radiation immunity is considered in the whole design.

The PLL generates a 1.6 GHz clock from a 40 MHz reference clock. A ring Voltage-Controlled Oscillator (VCO) is employed because of low power consumption. The VCO consists of four delay cells with positive feedback to gain fast slewing. The charge pump current and he loop filter resistor is programmable to minimized the jitter performance. Because the half-rate serializer structure is sensitive to the duty cycle of clock signal, a duty-cycle correction circuit is used to alleviate Duty-Cycle Distortion (DCD). The clock divider in the PLL loop is triplicated to resist SEU.

The digital interface block encodes the user data into 320-bit data frame in which there are 10-bit frame head, 256-bit pixel data, 14-bit timestamp and 40-bit overhead. The 256-bit raw data is received at 10 MHz from a CMOS sensor. In this prototype, we generate the 256-bit raw data through a pseudorandom binary sequence (PRBS) to emulate sensor data. The data with timestamp is scrambled and then encoded with Reed-Solomon algorithm. There are up to 20 consecutive bits could be corrected in a frame, benefitting from this RS(31,27) encoding in our scheme, which is suitable for burst errors in subatomic experiments. The penalty is a 40-bit overhead being added to the payload. The digital interface block delivers data with 32-bit width at frequency of 100 MHz to the serializer. The digital interface block is fully triplicated because that the feedbacks in the scrambler and the encoder are sensitive to errors induced by SEU.

The serializer is a 32:1 multiplexer with 5-stage binary-tree structure. Only the last stage is sensitive to duty-cycle error of the clock that is mitigated by the duty-cycle correction circuit. The serializer provides a complementary signal and its two copies of one and two clock period delay to the CML driver.

The CML driver realizes pre-emphasis with one main driver and two post-taps. The output swing and the tap coefficient is programmable. The maximum swing when all the pre-emphasis are off is 800 mV across two 50 Ω internal termination resistors.

The 3.2 Gbps serial link transmitter is designed in a 0.18 µm CMOS technology. The functionalities
are verified by simulation. The transmitter consumes 174 mW from a 1.8 V power supply. The prototype will be submitted in May. We expect to report the measurement results in the final paper.

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**Presenter:** Dr SUN, Quan (Southern Methodist University)

**Session Classification:** POSTER Session

**Track Classification:** ASIC
Development of ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC

Wednesday, 13 September 2017 17:45 (15 minutes)

The high-luminosity LHC will provide 5-7 times higher luminosities than the original design. An improved readout system of the ATLAS Liquid Argon Calorimeter is needed to readout the 182,500 calorimeter cells at 40-80 MHz with 16 bit dynamic range in these conditions. Low-noise, low-power, radiation-tolerant and high-bandwidth electronics components are being developed in 65 and 130 nm CMOS technologies. The design of the readout chain and the status of the R&D of the components will be presented.

Summary

The LHC high-luminosity upgrade in 2024-2026 requires the associated detectors to operate at luminosities about 5-7 times larger than assumed in their original design. The pile-up is expected to increase to up to 200 events per proton bunch-crossing. To be able to retain interesting physics events even at rather low transverse energy scales, increased trigger rates are foreseen for the ATLAS detector. At the hardware selection stage acceptance rates of 1 MHz are planned, combined with longer latencies up to 60 micro-seconds in order to read out the necessary data from all detector channels. Furthermore, the expected total radiation doses of $10^{13}$ neq/cm$^2$ (NIEL) and 0.3kGy (TID) are beyond the qualification range of the current front-end electronics. Under these conditions, the current readout of the ATLAS Liquid Argon (LAr) Calorimeters does not provide sufficient buffering and bandwidth capabilities. Furthermore, the expected total radiation doses are beyond the qualification range of the current front-end electronics. For these reasons a replacement of the LAr front-end and back-end readout system is foreseen for all 182,500 readout channels, with the exception of the cold pre-amplifier and summing devices of the hadronic LAr Calorimeter.

The system will follow a free-running architecture, where the calorimeter signals are amplified, shaped and digitized by on-detector electronics, then sent at 40MHz to the backend, which performs the energy and time reconstruction, and buffers the data until trigger signals are received. The analogue electronics needs to amplify and shape the triangular calorimeter signals over a dynamic range of 16 bits, with low noise and excellent linearity. Developments of low-power preamplifiers and shapers to accomodate these requirements are ongoing in two technologies. In CMOS 65 nm, a fully differential design allows to cover the dynamic range with a programmable termination, two gains and a shaper stage with programmable peaking time. A second design is implemented in 130 nm CMOS, which features a new line termination preamplifier using an electronically cooled resistance. The tests of the two gains of this prototype demonstrate an excellent linearity and the stability of the input impedance.

In order to digitize the analogue signals after shaping, radiation-hard, low-power 40MHz 14-bit ADCs are being developed using a SAR architecture in 65 nm CMOS technology. Such ADCs will allow the digitization of the full calorimeter dynamic range using a two-gain system. This architecture will lead to a total bandwidth of 275 Tbps to be sent off-detector. A newly designed VCSEL array driver shows that the required 10Gb/s transfer rate at 20-35mW per channel is achieved, suitable for integration into a low-power optical link package.

Results from the design studies on the performance of the components of the LAr readout system will be presented, as well as the results of the tests of the first prototypes.

Abstract submitted on behalf of the ATLAS Liquid Argon Speaker’s Committee

Speaker to be nominated later
Primary authors: ENARI, Yuji (University of Tokyo (JP)); ATLAS LAR CALORIMETER COLLABORATION

Presenter: HORN, Philipp (Technische Universitaet Dresden (DE))

Session Classification: POSTER Session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience
The Phase-I Trigger Readout Electronics Upgrade for the ATLAS Liquid-Argon Calorimeters

Thursday, 14 September 2017 09:20 (25 minutes)

Electronics developments are pursued for the trigger readout of the ATLAS Liquid-Argon Calorimeter towards the Phase-I upgrade scheduled in the LHC shut-down period of 2019-2020. The LAr Trigger Digitizer system will digitize 34000 channels at a 40 MHz sampling with 12 bit precision after the bipolar shaper at the front-end system, and transmit to the LAr Digital Processing system in the back-end to extract the transverse energies. Results of ASIC developments including QA and radiation hardness evaluations, and performances on prototypes will presented with the overall system design.

Summary

The upgrade of the Large Hadron Collider (LHC) scheduled for a shut-down period of 2019-2020, referred to as the Phase-I upgrade, will increase the instantaneous luminosity to about three times the design value. Since the current ATLAS trigger system does not allow sufficient increase of the trigger rate, an improvement of the trigger system is required. The Liquid Argon (LAr) Calorimeter read-out will therefore be modified to use digital trigger signals with a higher spatial granularity in order to improve the identification efficiencies of electrons, photons, tau, jets and missing energy, at high background rejection rates at the Level-1 trigger. The new trigger signals will be arranged in 34000 so-called Super Cells which achieves 5-10 times better granularity than the trigger towers currently used and allows an improved background rejection.

The readout of the trigger signals will process the signal of the Super Cells at every LHC bunch-crossing at 12-bit precision and a frequency of 40 MHz. The data will be transmitted to the back-end at 5.12 Gb/s using a custom serializer and optical converter. ASICs have been developed for ADC, serializer and transmitter for this project and PCB boards are being developed now. In the new back-end system, the received digital data will be processed with a FIR filter, optimal filtering, on a FPGA (Intel-FPGA Arria-X) to identify the bunch crossing and extract the transverse energy with a fixed latency. The results of the digital processing are transferred to the level-1 trigger system for trigger object reconstruction. The backend system is developed using the ATCA architecture. ATCA carrier blade with RTM will carries four Advanced Mezzanine Cards with the FPGA. In total, the backend system will consist from 31 carrier boards in three ATCA shelves.

In order to verify the full functionality of the new Liquid Argon trigger readout system, a demonstrator set-up has been installed on the ATLAS detector and has been operated in parallel to the regular ATLAS data taking during the LHC Run-2. Noise level and linearity on the energy measurement have been verified to be within our requirements. We have collected data with 13 TeV proton-proton collisions during the LHC Run-2, and have observed real pulse from the detector through the demonstrator system.

The talk will give an overview of the Phase-I Upgrade of the ATLAS Liquid Argon Calorimeter readout and present the custom developed hardware including their role in real-time data processing and fast data transfer. This contribution will includes the performance of the newly developed ASICs including their radiation tolerance and quality assurance, the performance of the prototype boards in the demonstrator system. Results of the system integration test with the final prototypes will be reported.
**Primary authors:** ENARI, Yuji (University of Tokyo (JP)); ATLAS LAR CALORIMETER COLLABORATION

**Presenter:** OCHOA, Ines (Columbia University (US))

**Session Classification:** Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Design and Test of a 65nm CMOS Front-End with Zero Dead Time for Next Generation Pixel Detectors

Tuesday, 12 September 2017 17:45 (15 minutes)

This work is concerned with the design of a synchronous analog processor with zero dead time developed in a 65 nm CMOS technology, conceived for pixel detectors at the HL-LHC experiment upgrades. It includes a low noise, fast charge sensitive amplifier with detector leakage compensation circuit, and a compact, single ended comparator able to correctly process hits belonging to two consecutive bunch crossing periods. A 2-bit Flash ADC is exploited for digital conversion immediately after the preamplifier.

A thorough discussion on the design and on the characterization of the readout channel will be provided in the conference paper.

Summary

Next generation pixel chips at the HL-LHC will operate with extremely high particle rates and radiation levels. In the so-called phase 2 upgrade, ATLAS and CMS will need a completely new tracker detector complying with the very demanding operating conditions and the delivered luminosity (up to 5x10^34 cm^-2s^-1 in the next decade). Very low noise performance of the analog front-end, along with stable low threshold operation, will be key points for the new chips in order to be highly efficient.

The 65 nm CMOS technology has been chosen by the designer community for the development of future readout chips at the HL-LHC. This technology retains the good degree of tolerance to ionizing radiation that is typical of CMOS processes in the 100 nm regime and enables the integration of advanced in-pixel analog and digital functions.

A synchronous analog front-end with zero dead time, called IFCP65, has been designed in a 65 nm CMOS technology in the framework of the CERN RD53 collaboration. It includes a low noise, fast charge sensitive amplifier with detector leakage compensation, and a compact, single ended comparator able to correctly process hits belonging to two consecutive bunch crossing periods. A 2-bit flash ADC is exploited for the analog-to-digital conversion.

The analog processor includes a charge sensitive amplifier (CSA) based on a regulated cascode gain stage and featuring a leakage current compensation circuit able to deal with the radiation-induced increase in the detector leakage. The output response of the CSA, whose measured charge sensitivity is close to 10 mV/ke, is characterized by a fast rising edge (a few nanoseconds), with an overall current consumption of the stage close to 4µA. The equivalent noise charge measured at the preamplifier output is close to 65 electrons for a 35 fF detector capacitance. The signal at the CSA output is fed to the threshold discriminator with auto-zero capability, which provides hit/no-hit information at the channel output. It is operated in two different phases, lasting 12.5 ns each: in the first one, called reset phase, the comparator gets reset and a proper bias is provided to the two stages making up the comparator. During the second one, an active comparison takes place by injecting both the CSA output and the threshold signals at the comparator inputs.

A 2-bit flash ADC is exploited for digital conversion immediately after the charge sensitive amplifier. The ADC design is based on three comparators with the same architecture used for the hit comparator, resulting in a conversion time for the in-pixel ADC equal to 12.5 ns. The ADC can be turned off, thus enabling a pure binary operation of the readout channel.
A thorough discussion on the design and on the characterization of the readout channel, included in a prototype chip integrating an 16x16 pixel matrix, will be provided in the conference paper.

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**Presenter:** BRAGA, Davide (FERMILAB)

**Session Classification:** POSTER Session

**Track Classification:** ASIC
Commissioning Experience and Upgrade Plans of the Pixel Luminosity Telescope for Luminosity Measurement at CMS

Wednesday, 13 September 2017 17:45 (15 minutes)

The Pixel Luminosity Telescope (PLT) is a dedicated system for luminosity measurement at the CMS experiment using silicon pixel sensors. It was installed during LS1 and has been providing luminosity measurements throughout Run 2. The online bunch-by-bunch luminosity measurement employs the “fast-or” capability of the pixel readout chip (PSI46) to quickly identify likely tracks at the full 40MHz interaction rate. In addition, the full pixel information is read out at a lower rate, allowing for more detailed offline analysis. In this talk, we will present details of the commissioning and operational history of the currently installed hardware and experience with offline analysis, in addition to upgrade plans for LS2.

Summary

The Pixel Luminosity Telescope (PLT) is a dedicated system for luminosity measurement at the CMS experiment using 48 silicon pixel sensors arranged into 16 “telescopes”, each consisting of three planes. The PLT was installed during LS1 at the beginning of 2015 and has been providing online and offline luminosity measurements throughout Run 2. The PLT is located outside the CMS pixel endcaps, with eight telescopes on either side of CMS installed around the beampipe. The silicon sensors and PSI46 pixel readout chips are the same as used in the CMS pixel detector. The online bunch-by-bunch luminosity measurement exploits the “fast-or” capability of the PSI46 readout chip, not used by the CMS pixel detector, which reads out a signal indicating if any of the pixels on the sensor was hit at the full bunch crossing rate of 40 MHz. Triple coincidences where a fast-or signal is received for all three telescopes in a plane are then measured in order to obtain an estimate of the luminosity, which provides an online bunch-by-bunch luminosity measurement with excellent statistical precision.

In addition, the full pixel information is read out at a lower rate, from which the track information can be fully reconstructed. This allows for the calculation of corrections to the online luminosity from effects such as the miscounting of tracks not originating from the interaction point and detector efficiency, as well as monitoring of the operational status and performance of the detector. The luminosity measurement is calibrated using Van der Meer (VdM) scans, in which the separation of the two colliding beams is scanned in order to measure the cross-sectional profile of the beams, from which the absolute luminosity can be determined. These scans were performed successfully in 2015 and 2016 during proton-proton, lead-lead, and proton-lead running and used to calibrate the PLT.

In this talk, we will present details of the commissioning and operational history of the currently installed hardware and experience with offline analysis, in addition to upgrade plans for LS2.

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**Presenter:** DELANNOY SOTOMAYOR, Andres Guillermo (University of Tennessee (US))

**Session Classification:** POSTER Session

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
A Micropower Readout ASIC for Pixelated Liquid Ar TPCs

Tuesday, 12 September 2017 17:45 (15 minutes)

The Liquid Argon Pixel (LArPix) prototype ASIC implements 32 channels of analog front end circuitry and backend digitizers at a power consumption of less than 50 uW/channel. LArPix is envisioned as a component of a potential DUNE near detector TPC module. Demanding noise, power, and dynamic range requirements are imposed by myriad particle interaction scenarios. Widely varying track signatures with charge depositions of 1-20 MIP (15k e-/MIP) per pixel at burst rates of up to 500 kHz must be accommodated. A unique design solution for these competing requirements will be presented, including initial functionality of the June 2017 tapeout.

Summary

The motivation for LArPix is to enable large liquid Argon TPC operation in high-rate environments. In addition to increased hit rate capability, another primary enabling factor is the reduced trajectory ambiguity achievable with a pixel-based detector. The feasibility of the pixel sensor array approach has been demonstrated by the LHEP group at U. Bern. The LArPix ASIC seeks to evolve that initial proof of concept towards a working detector system by using a full-custom, micropower ASIC solution.

The 32-channel prototype IC will be submitted for fabrication in a mixed-signal 0.18 um CMOS process in June 2017. The IC will be integrated onto a detector pixel array operating at 88K in liquid Argon. These detector planes will be part of a demonstrator TPC envisioned for neutrino experiments, e.g. as a component of the DUNE near detector. The LArPix IC analog channel is comprised of a charge readout Analog Front End (AFE) and Successive Approximation ADC (SAR). The digital backend logic provides timing, control, hit buffering, and serial communication with daisy-chain readout. The devices themselves will be assembled onto the detector PCB plane, physically over top of the communication and power buses. The arrangement is such that the devices form a track over the service buses, with 16 detector elements connecting to each side of a LArPix IC.

The AFE nominal power consumption is ~18-24 uW per channel, with the balance of power in the SAR and backend at less than 25 uW per channel. A total power of <50 uW per channel is compatible with operation in LAr. The AFE implements a pure charge integrator, comparator, threshold trim DAC, analog buffer, and low-power Schmitt trigger to condition the comparator output. The time resolution of the analog channel is 2 us, while limiting the ENC to <500 e- RMS at room temperature. The ENC of the AFE decreases to <300 e- RMS at 88K. These values are at or less than 1/3rd the 1500 e- RMS noise requirement, which is 1/10th MIP. The CSA operates with a switched reset, which is derived as the OR’ed combination of a periodic reset and a hit detection reset. The reset signal is generated by the ADC sampling and control engine, with the programmable periodic reset allowing for the clearing of leakage current and spurious background charge. Other features of the AFE include a trim DAC per channel, test pulse input, and high gain mode. The 5-bit trim DAC provides a fine tuning of the 8-bit, 6 mV resolution global DAC to accommodate severe channel mismatch at LAr temperature. The SAR will digitize the nominal AFE dynamic range of 20 MIP to a resolution of 8 bits. A high gain mode of 3 MIP dynamic range is available as a configuration setting in the AFE.
Primary authors: KRIEGER, Amanda (Berkeley Lab); DWYER, Dan (Lawrence Berkeley National Lab); GNANI, Dario (Lawrence Berkeley National Lab. (US)); GRACE, Carl (Lawrence Berkeley National Laboratory); GARCIA-SCIVERES, Maurice (Lawrence Berkeley National Lab. (US))

Presenter: KRIEGER, Amanda (Berkeley Lab)

Session Classification: POSTER Session

Track Classification: ASIC
Electronics and Firmware of the Belle II Silicon Vertex Detector Readout System

Wednesday, 13 September 2017 17:45 (15 minutes)

The Silicon Vertex Detector of the Belle II Experiment at the KEK in Tsukuba, Japan, consists of 172 double-sided strip sensors. They are read out by 1748 APV25 chips, and the analogue data are sent out of the radiation zone to 48 modules which convert them to digital. FPGAs then compensate line signal distortions using digital finite impulse response filters and detect data frames from the incoming stream. Then they perform pedestal subtraction, common mode correction and zero suppression, and calculate the peak timing and amplitude of each event from a set of data samples using a neural network.

Summary

At the High Energy Accelerator Research Organization (KEK) in Tsukuba, Japan, the Belle II experiment will start in 2019 to refine the exploration of the asymmetry between matter and antimatter of the original Belle experiment with a 40 times higher luminosity of 8x10^35 cm^-2s^-1, and to search for new physics beyond the standard model by measuring the tracks of the collision products of electrons and positrons. This requires a redesign of the detector and its peripherals.

One of the Belle II sensor subsystems is the Silicon Vertex Detector, which consists of 172 orthogonal double-sided strip silicon sensors made of 6 inch wavers each. They are arranged cylindrically in four layers around the collision point. These sensors are read out by 1748 radiation-hard CO2 cooled APV25 front-end chips, partially sitting directly on the sensors (“Origami” chip-on-censor-concept), and powered by radiation-hard DC-DC converters in junction boxes inside the magnetic field. One time-division multiplexed differential analogue data signal is sent by each one of these read-out chips out of the radiation zone over approximately 15 meter long copper cables to four crates with 48 so called FADC modules, which convert the data streams to digital using one flash analog digital converter per APV25 chip.

Each of these FADC modules also includes a field programmable gate array (FPGA) chip, namely an Altera Stratix IV GX, which compensates analog line signal distortions using digital finite impulse response filters, and detects data frames in the incoming streams. It then reorders the strip signal data according to the physical arrangement, performs pedestal subtraction and common mode correction to each strip value to eliminate static offsets, executes zero suppression to discard empty strip data for data size reduction, and it calculates the peak timing and amplitude of each event from a set of data samples using a neural network in real-time to further reduce the amount of data. Eventually, the processed data are sent to the pixel detector to provide information for timing and the determination of spatial regions of interests, as well as to a data acquisition system which collects the data of all subdetectors and performs high level trigger data selection.

We will show an overview of the Silicon Vertex Detector data readout system, from the detector itself with its front-end electronics, over the cabling, junction boxes, power supplies for the read-out chips and the “high voltage” biasing of the silicon sensors, read-out-signal potential separation and digitization, to the data processing inside the FPGAs on the FADC modules and the data output systems. Furthermore we will present most recent test results of the prototypes of the system in beam tests and long-term-tests, improvements we applied to the electronics with comparisons to previous prototypes, and first analysis results of simulations of the expected performance of the
neural network for the hit time finding system in the FADC firmware.

**Primary author:** THALMEIER, Richard (Austrian Academy of Sciences (AT))

**Presenter:** THALMEIER, Richard (Austrian Academy of Sciences (AT))

**Session Classification:** POSTER Session

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
SEE Tolerant Standard Cell Based Design While Guaranteeing Specific Distance Between Memory Elements

Tuesday, 12 September 2017 08:30 (20 minutes)

Single Event Effects (SEEs) comprising of Single Event Upsets (SEUs) and Single Event Transients (SETs) corrupts the data in storage nodes/registers. Triple Modular redundancy (TMR) with clock delay insertion is a system level technique that counters SEEs in storage nodes. However, such an implementation is not straightforward in standard cell based digital design which uses CAD tools like Genus/RC compiler and Innovus for synthesis & Physical design. This paper presents a successful automation methodology that maps the intended registers in the Verilog RTL with triplicated cell during synthesis and guarantees minimum distance between memory elements during placement & routing leading to SEE tolerant standard cell based digital design.

Summary

Single Event Effects (SEEs) are very common in ASICs used for detector electronics due to the ionizing particles from the particle collisions. SEEs comprise of Single Event Upsets (SEUs) and Single Event Transients (SETs) and manifest themselves as bit flips in sequential elements and glitches in combinational gates. A Single Event Upset (SEU) in data path register results in incorrect data packets from the serial links, whereas an SEU in global configuration registers makes the chip non-functional. In a joint effort between Atlas/CMS groups for RD53A pixel chip the estimated bit flips due to SEUs in global configuration registers is every ~20s per chip, whereas in pixel registers is ~60 bit flips per second per pixel per chip. Hence SEE tolerant design is unavoidable for RD53A at pixel configuration registers, global configuration registers and data path registers in digital chip bottom.

Traditionally TMR implementation is handled by the RTL designers during hardware description in Verilog/VHDL. The drawback with this approach is while doing synthesis & optimization the tools might remove the intended triplicated redundancy logic; therefore, the top-level designer must carefully verify the TMR presence in the synthesized gate level netlist, which is cumbersome and time taking in large designs. The problem aggravates when the RTL is written by one designer and the digital design flow is carried out by another designer.

Another approach is to synthesize the digital logic and replace the intended register cell with the custom triplicated standard cell. This approach is functional but has drawbacks in that it might cause routing congestion in big chips that have many TMR cells.

In this article, we introduce the automation methodology to implement SEU tolerant digital design using conventional semi-custom design tools adopted in RD53A pixel chip for Atlas/CMS experiments. The methodology is based on Cadence Genus tool for logic synthesis and Innovus for the physical design, which are commonly used tools for digital design in high energy physics community.

We demonstrate the methodology by introducing additional stages/steps during synthesis and physical design. The registers in the Verilog RTL are mapped with triplicated cell during synthesis and additional constraints during place and route guarantees minimum distance between memory elements. This methodology is verified on a simple design but it can be easily scalable to large designs consisting of multi-million standard cells. The TMR mapping is demonstrated in
following cases which are quite relevant during digital design:
1. Triplicating the register which has \( tmr \) as the instance name in RTL
2. Triplicating all the registers in the RTL
3. Triplicating registers in one of the module in RTL
4. Triplicating the register along with correction mechanism

Through this approach, it is possible to implement TMR in any register of the design, avoids routing congestion as the triplicated flops are spread across the entire core area of the chip and guarantees minimum distance between memory elements to counter multiple bit flips in TMR at any time.

**Primary author:** MIRYALA, Sandeep (Fermi National Accelerator Lab. (US))

**Presenter:** MIRYALA, Sandeep (Fermi National Accelerator Lab. (US))

**Session Classification:** Programmable Logic, Design Tools and Methods

**Track Classification:** Programmable Logic, Design Tools and Methods
Two High-Speed Dual-Channel VCSEL Driver

We present two designs of a dual-channel VCSEL driver ASIC, named LOCld130 and LOCld65, aiming for the upgrade of ATLAS Liquid Argon Calorimeter. Each channel of the driver operates at 5 Gbps or 10 Gbps respectively. They are implemented in commercial 130 nm and 65 nm CMOS technologies. In typical case the 5 Gbps driver dissipates 56 mW/channel (VCSEL included) and the 10 Gbps 58 mW/channel. Both designs will be prototyped this summer.

Summary
Based on years of R&D, wafers of the dual-channel VCSEL driver, LOCld, implemented in a commercial 250 nm Silicon-on-Sapphire CMOS technology are produced. LOCld is the baseline choice for ATLAS Liquid-Argon-Calorimeter trigger upgrade. We design LOCld130 as a drop-in backup to LOCld, benefiting from the 1.5 V 130 nm technology to save power. We develop LOCld65 using the same 65 nm technology with which lpGBT is being developed. lpGBT is the serializer-deserializer (SerDEs) ASIC developed chiefly for upgrades of the HL-LHC. The serializer operates at 5 or 10 Gbps. While the predecessor of lpGBT, the GBTx SerDes has a matching optical transceiver (VTRx) developed through the Versatile Link common project, the optical module being investigated in VL+ will be based on array optics with a VCSEL driver that has a different driving mechanism and is not suitable for single channel transceivers. We advocate and design the dual-channel VCSEL driver with each channel operates up to 10 Gbps. Although both LOCld130 and LOCld65 are dual-channel drivers, each channel in the ASIC is individually powered, making them suitable for applications in dual-channel optical transmitters such as MTx and VTTx or in transceivers such as MTRx and VTRx. LOCld65 is to provide a perfect match to lpGBT when the application does not call for array optics, and to benefit from the current development of optical modules of MTx and VTTx.

The analog core of LOCld130 has two parts: a limiting amplifier (LA) and a high-current differential driver. The minimum input signal is assumed to be 200 mVP-P. The LA gain is designed to 14 dB. A shared inductive peaking is used in the 2-stage amplifier to boost the bandwidth to 3.5 GHz. The passive peaking also compensates the high-frequency signal loss due to the ESD pad. Both modulation and biasing currents are programmable with I2C. The total power consumption of one VCSEL driving channel is 56 mW when the modulation current is 6 mA with a 2 mA bias. Power for I2C is below 1 mW.

LOCld65 is similar to LOCld130. Because the input signal is expected to be 100 mVP-P per the lpGBT design specification the LA has 4 stages with shared inductive peaking. An active feedback cell is used between the stages to adjust the gain and bandwidth by programing its current. The feedback cell significantly reduces the process effect on the LA gain and bandwidth. The LA is simulated to have a gain of 18-dB and a bandwidth more than 7 GHz. The output driver has a pre-emphasis option to improve the output signal with different load. The total power consumption of each VCSEL driver channel is 58 mW with 6 mA modulation and 2 mA bias.

Both designs have been verified in simulation and will be submitted for prototype fabrication this summer. We expect to test the chips by the end of this year.
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Presenter: ZHOU, Wei (Central China Normal University)

Session Classification: POSTER Session

Track Classification: ASIC
Performance of the CATIA ASIC, the APD Readout Chip Foreseen for the CMS Barrel ECAL Electronics Upgrade at the HL-LHC

Tuesday, 12 September 2017 17:45 (15 minutes)

The CMS ECAL barrel electronics will be upgraded for the HL-LHC to meet the latency and bandwidth requirements of the Phase-II Level-1 trigger system. The front-end electronics will mitigate the increasing noise from the avalanche photodiodes (APDs), discriminate against anomalous APD signals and provide improved timing information. The foreseen solution is to replace the current Charge-Sensitive-Amplifier with a Trans-Impedance Amplifier (TIA) which should provide the extra bandwidth needed to maintain the integrity of the detector signal shape. The first ASIC prototype, called CATIA, has been successfully designed in TSMC 130 nm CMOS technology and its test results will be presented.

Summary

The LHC Phase-II upgrade will lead to a significant increase in luminosity which implies the full replacement of the ECAL Barrel (EB) electronics to meet the Level-1 trigger requirements. By including the front-end electronic in this upgrade, there is a possibility to mitigate the increasing noise induced by avalanche photodiode (APD) ageing, to improve the suppression capability of APD anomalous signals and to reach the intrinsic timing resolution of the detector constituted by crystals and APDs, in order to help to discriminate between energy deposits coming from different overlapping events. This can be done by replacing the actual APD readout chip (MGPA) based on a Charge Sensitive Amplifier (CSA) with a high speed Trans-Impedance Amplifier (TIA) - 50 MHz of bandwidth - followed by 160 MspS 12-bit ADCs. The high speed TIA and high speed ADC will enable the discrimination of spike signals from the scintillation signals by analyzing the characteristic differences of their shapes (width measurement). In addition, they will provide time measurements at the level of 30 ps for electrons and photons above 50 GeV. The architecture of the TIA is a Regulated Common-Gate (RCG) TIA which offers a reduced input resistance compatible with the high input capacitance (200 pF) of the APD providing the high bandwidth foreseen. The gain is achieved by a resistor chosen to fit the maximum input signal at 2TeV for an INL < +/- 0.1%. The output dynamic is split into 2 ranges: 200 GeV & 2 TeV. The 200 GeV is achieved through a gain10 stage after the TIA.

The first step of this electronics upgrade is to design this TIA independently of the ADC to confirm the simulation study results and to analysis the performances obtained with the TSMC 130 nm process. This was achieved by prototyping an ASIC called CATIA formed by 2 different channels realized in the 2 voltage supplies allowed by the process, 1.2V and 2.5V, for 4 channels in total. The difference between channels comes from the architecture of the gain10 stage which permits to define or control the internal DC voltage level.

The chip was submitted in October 28 2016 and received in the end of February 2017. The tests performed in laboratory with pulse generators and an APD detector confirm the functionality of the chip and the performances obtained prove that the TIA is a good candidate for the ECAL Barrel electronics HL-LHC upgrade.

Primary author: CMS COLLABORATION
Presenter: GUILLOUX, Fabrice (CEA/IRFU,Centre d'étude de Saclay Gif-sur-Yvette (FR))

Session Classification: POSTER Session

Track Classification: ASIC
Prospects for a Precision Timing Upgrade of the CMS PbWO Crystal Electromagnetic Calorimeter for the HL-LHC

Thursday, 14 September 2017 08:55 (25 minutes)

The upgrade of the Compact Muon Solenoid (CMS) crystal electromagnetic calorimeter (ECAL), which will operate at the High Luminosity Large Hadron Collider (HL-LHC), will achieve a timing resolution of around 30 ps for high energy photons and electrons. We will discuss the benefits of precision timing for the ECAL event reconstruction at HL-LHC. Simulation studies on the timing properties of PbWO crystals, as well as the impact of the photosensors and the readout electronics on the timing performance, will be presented. Test beam studies, including new results from 2017, on the timing performance of PbWO crystals with various photosensors and readout electronics will be shown.

Summary

The electromagnetic calorimeter (ECAL) of CMS is currently operating at the LHC. The instantaneous luminosity during the current LHC Run2 is in the range of up to $2 \times 10^{34}$ cm$^{-2}$s$^{-1}$ in routine operation. With an upgrade at the end of the decade, the High-Luminosity LHC (HL-LHC) will increase the instantaneous luminosity by about a factor of 2 to 5 from current levels. The goal of the HL-LHC is to accumulate a total of at least 3 ab$^{-1}$ of data.

Particular challenges at HL-LHC are the harsh radiation environment, the increasing data rates and the extreme level of pileup events, up to 200 simultaneous proton-proton collisions. The pileup mitigation may be substantially improved by means of precision time-tagging of calorimeter clusters, by associating them to primary vertices via 4D triangulation. We will discuss in detail the timing performance requirements for such a 4D triangulation technique and how it can be achieved with the upgraded CMS ECAL.

We review the design and R&D studies for the HL-LHC CMS ECAL crystal calorimeter upgrade for which the lead tungstate PbWO$_4$ crystals, the Avalanche Photo-Diode (APD) photodetectors with their respective motherboards as well as the overall mechanical structure of the ECAL barrel will remain unchanged. The readout electronics will be replaced to cope with the higher bandwidth and latency required for operation at the HL-LHC and will enable the calorimeter to achieve a timing resolution of around 30 ps for high-energy photons.

The upgraded very front-end (VFE) electronics will achieve this timing performance by shortening the shaping time from the current 43 ns to 20 ns and increase the digitization rate from 40 MHz to 160 MHz. The VFE will employ re-designed ASICs to optimize shaping time and sampling to reduce the impact of noise, out-of-time pileup, and anomalous isolated large signals in the APDs. Pulse shaper and preamplifier ASIC options we are currently investigating include Trans Impedance Amplifiers (TIA) and a further iteration of the current architecture (MGPA, CR-RC) as an alternative, optimized for a 130 nm process, faster shaping and additional rejection logic for anomalous signals. As digitizers we consider multi-channel ADCs with 12-bit resolution at a higher sampling rate of 160 MHz, which benefits, in particular, the timing resolution. Prototype boards with the above design criteria are currently undergoing lab and test beam measurements. We will present results from these test beam measurements - including new ones from 2017 - with a prototype utilizing a 5x5 matrix of CMS ECAL PbWO4 crystals with readout electronics following the design path described above. Different digitization speeds were emulated offline to demonstrate the requirements for the final choice of the readout.
We will also discuss in detail extensive simulation studies on the optimization of the shaping time and sampling rate to achieve optimal timing performance. We will also show simulation studies and further test beam measurements on the timing properties of large-size scintillating crystals, as used in the CMS ECAL. These studies illustrate that for the performance targets we envision indeed the photodetector and readout chain are the limiting factors for the timing performance.

**Primary author:** CMS COLLABORATION  
**Presenter:** JESSOP, Colin (Notre Dame)  
**Session Classification:** Systems, Planning, Installation, Commissioning and Running Experience  
**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Design of the New Front-End Electronics for the Readout of the Upgraded CMS Electromagnetic Calorimeter for the HL-LHC

Wednesday, 13 September 2017 17:45 (15 minutes)

At the high-luminosity upgrade of the LHC (HL-LHC), the electromagnetic calorimeter of CMS (ECAL) will have to cope with a challenging increase in the number of interactions per bunch crossing and radiation levels. The ECAL front-end readout electronics was completely redesigned, with the goals of providing precision timing, low noise and added flexibility in the trigger system. It will use a faster pre-amplifier, increase the sampling frequency from 40 MHz to 160 MHz and implement a trigger system that resides entirely off-detector. The design of this new electronics will be presented along with the test results of the first prototypes.

Summary

The electromagnetic calorimeter (ECAL) of CMS is currently operating at the LHC. The instantaneous luminosity during the current LHC Run2 is in the range of up to $2 \times 10^{34}$ cm$^{-2}$s$^{-1}$ in routine operation. With an upgrade at the end of the decade, the High-Luminosity LHC (HL-LHC) will increase the instantaneous luminosity by about a factor of 2 to 5 from current levels. The goal of the HL-LHC is to accumulate a total of at least 3 ab$^{-1}$ of data.

With such high luminosity and consequent event rate, the primary driver of the ECAL front-end electronic upgrade are the requirements on the first level of the CMS trigger system, implemented with custom-design hardware boards. Specifically, the latency has to be of 12.5 $\mu$s, about a factor of two more than the current electronics, and the sustainable rate must go up to 750 kHz, about a factor of five more than the current design.

The front-end readout electronics was completely re-designed to satisfy these requirements, and the opportunity was taken to optimize the mitigation of radiation-induced noise increase in the APDs, the rejection of APD anomalous signals, and the time resolution of the arrival of electromagnetic showers.

The individual boards of the new electronics will follow the same configuration and form factor as the present ones, mostly imposed by the decision not to modify the cooling system or the motherboards connecting the very-front-end (VFE) to the crystal APDs. The VFE pre-amplifier will reduce as much as possible the shaping time of the signal, by employing a Trans-Impedance Amplifier (TIA), which will sample the pulse at 160 MHz. Two gain stages will follow and digitize signals up to 2 TeV with 2 12-bit ADCs. High-speed optical links and their foreseen evolutions at 10 Gb/s (lp-GBT) will enable us to send to the off-detector electronics all the single crystal data via a data transmission unit with lossless compression.

The system will use 130 nm CMOS technology for the replacement of analogue ASICs and 65 nm technology for digital ones, which are both naturally radiation-tolerant and provides up to 75% gain in power consumption. A specific low-voltage regulator card is being developed to provide all the required bias voltages. Control signals and clock distribution will be provided by (redundant) GBTX control buses.

The talk will discuss in detail the requirements of the new ECAL front-end electronics along with the design options and adopted choices to fulfill them. It will also show the results of beam tests performed with a first prototype of the TIA electronics using discrete components.
Primary author: CMS COLLABORATION
Co-author: COMETTI, Simona (Universita e INFN Torino (IT))
Presenter: GUILLOUX, Fabrice (CEA/IRFU, Centre d'étude de Saclay Gif-sur-Yvette (FR))
Session Classification: POSTER Session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience
Design Studies for the Off-Detector Electronics of the Upgraded CMS Electromagnetic Calorimeter for the HL-LHC

Wednesday, 13 September 2017 17:45 (15 minutes)

At the high-luminosity upgrade of the LHC (HL-LHC), the electromagnetic calorimeter of CMS (ECAL) will have to cope with an increase in the number of interactions per bunch crossing and radiation levels. CMS implements a sophisticated two-level triggering system composed of the Level-1, instrumented by custom-designed hardware boards, and a software High-Level-Trigger. The off-detector electronics has been redesigned with increased capabilities, exploiting the full granularity of the calorimeter at Level-1. The talk focuses on the new design and its expected performance, compared to the LHC Run2 in terms of trigger rate, rejection of anomalous signals, and selection efficiency for electrons and photons.

Summary

The electromagnetic calorimeter (ECAL) of CMS is currently operating at the LHC and its barrel part consists of 61200 lead tungstate crystals. The instantaneous luminosity during the current LHC Run2 is in the range of up to $2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$ in routine operation. With an upgrade at the end of the decade, the High-Luminosity LHC (HL-LHC) will increase the instantaneous luminosity by about a factor 2 to 5 from current levels. The goal of the HL-LHC is to accumulate a total of at least 3 $\text{ab}^{-1}$ of data.

CMS implements a sophisticated two-level triggering system composed of the Level-1, instrumented by custom-design hardware boards, and a software High-Level-Trigger.

With the luminosity foreseen for the HL-LHC, and consequent event rate, the requirements on the CMS Level-1 trigger system are a latency of 12.5 $\mu$s, about a factor of two more than the current electronics, and a sustainable rate up to 750 kHz, about a factor of five more than the current design.

The front-end readout electronics was completely re-designed to satisfy these requirements. In contrast to the current electronics, which hosts the computation of “trigger primitives” (coarse information on the deposited energy in ECAL, exploited at Level-1) directly on the on-detector electronics, the upgraded design will shift their computation off-detector. This will be possible by means of 10 Gb/s high-speed optical links (lp-GBT) transmitting off-detector the single-crystal information, serialized by groups of 25 crystals. Accounting for one additional link for every 25 crystals, to transmit the system clock and control signals, an order of 10k of such links will suffice for the whole ECAL.

The processor used offline to compute trigger primitives are not required to be radiation tolerant, as they will be located in the service cavern. Therefore design choice opens up to commercial solutions, such as the CTP7/MP7 $\mu$TCA boards.

The algorithms to be implemented in this board include: conversion of digitized pulse data into transverse energy, rejection of anomalous APD signals based on topological criteria, basic clustering of localised energy. The board will also interface with the central CMS L1 trigger and DAQ systems.

The talk will discuss in detail the requirements of the new ECAL off-detector electronics and the design options and choices for its architecture. The algorithms to be implemented will be illustrated.
and compared to the current system, along with the first estimates of their performance in terms of trigger rates, rejection of anomalous signals, selection efficiency for electrons and photons.

**Primary author:** CMS COLLABORATION

**Presenter:** GOADHOUSE, Stephen (University of Virginia (US))

**Session Classification:** POSTER Session

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Development of a Monolithic Low Power, High Speed Pixel Sensor for Particle Tracking in High Energy Physics Experiments

Wednesday, 13 September 2017 17:15 (15 minutes)

We have developed a 2nd generation high resistivity CMOS process, suited for integration of complementary pixel circuitry. High charge collection efficiency can be maintained after neutron irradiation up to $10^{16}$ neq/cm² when applying a depletion voltage to the backside of the 50 µm thick devices. Results measured with a 15 µm MAPS detector, fabricated in this technology, will be presented.

Based on the Orthopix architecture, we are developing a megapixel detector with digital pixel output on 20 µm pitch supporting a frame rate of 50 MHz at a power dissipation of 200 mW/cm². Process and design will be presented.

Summary

The next generation of detectors for high energy physics experiments with high luminosity must support hit rates >1 MHz/mm² and remain functional after accumulating a neutron radiation dosage up to $2 \times 10^{16}$ neq/cm². In addition, the excellent tracking information of today’s pixel detectors must be extended to cover a larger area while at the same time existing power budgets must not be exceeded. Present generation pixel detectors are mostly based on hybrid or 3D IC technology, but it is questionable whether they can be fabricated sufficiently economically to meet budget constraints.

Monolithic Active Pixel Sensors (MAPS), fabricated using mainstream CMOS image sensor (CIS) processes, can be operated with very low power consumption and can be produced in large quantities at low cost. However, available CIS technologies use low resistivity silicon and only allow integration of one type of transistor inside the pixel (typically NMOS). These constraints cause limitations in the maximum achievable readout speed, minimum power consumption, and radiation hardness. Some improvements in radiation hardness could be made in such devices when adding a high resistivity EPI layer, thereby introducing a drift component to the charge collection. But preferably a detector backside bias voltage can be increased as radiation damage is accumulated. This is the practice pursued in existing hybrid pixel detectors.

Sensor Creations has developed a custom CMOS process using high resistivity float zone wafers. The feasibility of this technology was demonstrated in a 640x512 pixel resolution imager with 15 µm pitch. The devices are 50 µm thick and can be fully depleted by applying a voltage of at least -10V to an electrode that is added to the backside of thinned wafer. The 1st generation devices, however, suffered from early breakdown causing high leakage current and low quantum efficiency due to incomplete depletion.

After an extensive analysis of the structure using TCAD simulation tools, the process was revised and a 2nd generation high resistivity CMOS technology created. In the improved process implementation, full depletion can be achieved without breakdown. In addition, it is now possible to integrate complementary circuitry into the unit cell so that a functionality, comparable to that of hybrid pixel detectors, can be supported.

In this presentation, we will show measurement results from our fully redesigned 640x512 pixel image sensor, processed in the 2nd generation technology. In addition, we will review on-going
design work for a radiation hard, high speed low power megapixel detector array based on the “Orthopix” architecture. In the new monolithic sensor, the pixel comprises a charge amplifier and discriminator and all data transfer inside the array is done in the digital domain. The new device has a pixel pitch of 20 µm and can be read out at a frame rate of 50 MHz and a power dissipation of 200 mW/cm². This level of performance meets the initial goal of a 1 MHz/mm² hit rate within existing power budgets.

**Primary authors:**  Dr LAUXTERMANN, Stefan (Sensor Creations, Inc.); Dr PETTERSSON, Per-Olov (Sensor Creations, Inc.); Dr VURAL, Kadri (Sensor Creations, Inc.); Dr WONG, Selmer (Sensor Creations, Inc.)

**Presenter:**  Dr LAUXTERMANN, Stefan (Sensor Creations, Inc.)

**Session Classification:**  POSTER Session

**Track Classification:**  Radiation Tolerant Components and Systems
The AdvancedTCA standard has been selected as one hardware platform for the upgrades of the back-end electronics of the CMS and ATLAS experiments of the Large Hadron Collider. In this context, the CERN EP-ESE group has designed and produced an IPMC mezzanine card for the management of AdvancedTCA blades. This paper presents the CERN-IPMC hardware and the software environment to be used for its customization and describes a test pad that can also be used as a development kit. Finally, it also introduces the foreseen conditions for distributing the module.

Summary

Originally developed for the telecommunication industry, the AdvancedTCA standard has been selected as one of the platforms for the upgrades of the ATLAS and CMS back-end electronics at CERN. In this context, the CERN EP-ESE group launched in 2011 the xTCA evaluation project whose aim is to perform technical evaluation of equipment, provide support for the selected components as well as design and support standardized system components.

The AdvancedTCA standard, defined by the PCI Industrial Computer Manufacturer Group (PICMG), outlines a modular architecture by defining physical, electrical and functional specifications. It offers a wide range of hardware management features to monitor (temperatures, voltages, current, etc.) and control (fan speed, power management, etc.) the system as well as ensure its proper operation (interoperability, current requirement, e-keying, etc.). These actions are performed by specific controller modules which are interconnected via an Intelligent Platform Management Interface (IPMI) bus: Module Management Controller (MMC) for AMCs, Intelligent Platform Management Controller (IPMC) for ATCA boards and Carrier IPMC for ATCA carriers as well as Shelf Manager for ATCA shelves and MicroTCA Carrier Hubs. In the frame of the CERN xTCA evaluation project, a commercial Intelligent Platform Management Controller (IPMC) solution from Pigeon Point was evaluated in 2015. Following this evaluation, a mezzanine card was designed to be used on existing and future AdvancedTCA blades compliant with a specific form factor (VLP DIMM-DDR3) already proposed by LAPP for the ATLAS experiment.

A first batch of IPMCs was successfully produced in spring 2017 and is ready to be distributed. In parallel, a complete software environment and documentation were set up to ease the customization of the CERN-IPMC: implementation of sensors, customization of the FRU information, etc. To fully validate the controller, a small tester board was designed to carry out automatic tests. It provides connectivity to all of the interfaces available on the mezzanine card: IPMB buses, one I2C line dedicated to sensor monitoring and another for the power management. Additionally, all of the GPIO pins are connected to a CPLD in order to which allows monitoring them through an USB connection. Finally, the JTAG master and the UART interfaces managed by the IPMC are directly routed to connectors. Finally, this automatic tester can also be used as a development kit for early users.

This paper provides a description of the CERN-IPMC with all supported features as well as a presentation of the test pad used for production. It also outlines the foreseen conditions for distributing the IPMCs to interested users.
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Presenter: MENDEZ, Julian Maxime (CERN)

Session Classification: Other

Track Classification: Other
The GBT-FPGA, part of the GBT project framework, is a VHDL-based IP designed to offer a back-end counterpart to the GBTX ASIC, a radiation tolerant 4.8 Gb/s optical transceiver. The GBT-SCA (Slow Control Adapter) radiation tolerant ASIC is also part of the GBT chipset and is used for the slow control in the HEP experiments. In this context, a new module named GBT-SC has been designed and released to handle the slow control fields hosted in the GBT frame for Internal Control (GBTx) and External Control (SCA). This paper presents the architecture and performance of this new module as well as an outline of recent GBT-FPGA releases and future plans.

Summary

The GBT-FPGA project was launched in 2009 following a study that consisted in validating the implementation of the GBTX serializer-deserializer in FPGAs. The project then gradually evolved to provide a common and centrally supported VHDL core to the GBT community. This IP, available for many FPGAs, ensures proper communication with the GBTX ASIC through the GBT link. This complete communication architecture has been widely selected for the upgrades of the DAQ, trigger and timing systems of the LHC experiments.

Based on the GBT chipsets, this system is divided into two parts: the Rad-hard ASICs, which are used close to the detectors, and the back-end modules implemented in FPGAs. The GBT-FPGA core offers a back-end counterpart to the GBTx, compatible with GBT frame definition and providing a 4.8 Gb/s high-speed serial link. The communication is typically done using the GBT protocol which is organized in frame of 120 bits sent at 40MHz. The frame structure can be divided in 5 fields: the header, Internal Control (IC), External Control (EC), payload and Forward Error Correction (FEC). The GBTX can be configured to divide the payload in up to 40 fields, called e-links, dedicated to the communication with front-end chips. The EC field is an additional e-link specifically designed to be used for the control of the GBT-SCA. Finally, the IC field is internally used for the configuration of the GBTX.

The GBT-SCA is a radiation tolerant chip that is used by the LHC experiments for the slow control of the front-end electronics. It provides several interfaces that can be controlled by a set of internal registers: 32 General Purpose IOs pins, up to 16 concurrent I2C masters, one SPI master with 8 slave select outputs, one JTAG master, up to 32 ADC inputs including one hard-wired internal temperature sensor and 4 DAC outputs. The GBT-SCA follows the HDLC communication standard by means of an 80 Mb/s serial lane, which is driven by a dedicated GBTX e-link. However, all of the general purpose e-links can be used for this purpose meaning that up 41 GBT-SCA chips can practically be concurrently controlled over the same GBT link.

A new VHDL module, released in spring 2017, fully compliant with the GBTX and the GBT-SCA ASICs, has been designed by the GBT-FPGA team in order to provide a common IP dedicated to Slow Control. Named GBT-SC, it offers a simple solution to manage the Internal and External Control fields of the GBT frame and can be instantiated in complement to the GBT-FPGA IP. Allowing to control between 1 and 41 SCAs, it features parallel configuration of several chips and is optimized in terms of latency and resource. Finally, additional acceleration modules are implemented in example designs to speed up as much as possible the use of the GBT-SCA interfaces. These goal are to limit the impact of the protocol used to control the firmware and can be additionally implemented depending on the requirements.
This talk introduces the new GBT-SC IP with a presentation of its architecture and performance as well as a summary of the recent GBT-FPGA developments and future plans.

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**Presenter:** MENDEZ, Julian Maxime (CERN)

**Session Classification:** Programmable Logic, Design Tools and Methods

**Track Classification:** Programmable Logic, Design Tools and Methods
A Compact Size, 64-Channel, 80 MSPS, 14-Bit Dynamic Range ADC Module for the PANDA Electromagnetic Calorimeter

Wednesday, 13 September 2017 08:55 (25 minutes)

A compact-size, 64-channel, 80 MSPS, 14-bit dynamic range ADC module for the scintillating electromagnetic calorimeter of PANDA was developed, tested in various detector readout set-ups and are currently in mass production phase. The module performs signal filtration, extract important signal parameters and allow for resolving and parametrizing overlapping pulses. Processed data are pushed to optical links running at 2 Gbit/s. The ADC module is equipped with a PLL phase noise cleaner and allows for defined latencies. 225 of these modules will be placed inside of the PANDA detector volume, exposed to magnetic field of up to 2T and a non-negligible radiation flux.

Summary

The Electromagnetic Calorimeter (EMC) of the Anti-Proton Annihilation at Darmstadt (PANDA) detector at the Facility for Antiproton and Ion Research (FAIR) consists of over 15000 PbWO4 crystals and is designed for detection and parametrization of particles with kinetic energies up to 15 GeV [1]. For accurate reconstruction of events in the PANDA, a correct merging of energy spills as low as 1 MeV per crystal is desired. Since all EMC crystals will be equipped with double photo-sensor readout and a 14-bit dynamic range is obtained in a dual-range ADC structure, the total number of digitizer channels placed inside of the detector volume will exceed 60000, requiring highly compacted electronics.

The signals entering the ADC are shaped using analog filters and then processed by a set of 8-channel 14-bit, 80 MSPS analog-to-digital converter circuits. Digitized samples are sent to 2 FPGAs via 128 LVDS links running at 560 Mbit/s each. The FPGAs allow for signal filtration, and extracting of important signal parameters, such as time of arrival, pulse amplitude and pulse integral. Analog and digital signal filtration parameters and algorithms were optimized to fulfill the required dynamic range and provide acceptable pile-up resolution at the anticipated maximum hit rate of 500 kHz per channel.

The processed data are pushed to optical links via multi-gigabit transceivers (GTX) running at 2 Gbit/s. The implemented UDP/IP core leads to a great simplification of lab setups allowing the SADC data to be directly transferred to a PC for test purposes.

The ADC modules are equipped with PLL phase noise cleaners and allow for defined latencies. The ADC module is compliant with the SODA System, for which the reference clock is distributed by a detector synchronization system (SODA), using the down-link part of the ADCs optical transceiver [2].

In order to test the endurance of the ADC in a radiation environment, the device was irradiated with a neutron beam at The Svedberg Laboratory (TSL), Uppsala University in June 2016 and with a proton beam delivered by the AGOR cyclotron at KVI, Groningen in November 2016. During the experiment, the Xilinx Soft Error Mitigation (SEM) Controller was placed in the FPGA. During the a test beam-time at Max Lab in Lund, 2014, the ADC was used in a detector setup for testing response of EMC Forward End-Cap PbWO4 crystals to photons with energies of 11, 26, 38 and 62 MeV. After off-line energy reconstruction, the relative energy resolution was found to be fulfilling the Technical Design Report requirements of the PANDA EMC with a safety margin.

The dimensions of the 64-channel modules amount to 100x150 mm. Despite a high channel density, no measurable crosstalk has been observed. The power consumption amounts to 22W. This requires efficient cooling, which will be accomplished by liquid-cooled aluminum encapsulations.
in the PANDA.

2. I. Konorov et al., Conference Record, 2009 IEEE NSS, Orlando, Florida, USA.

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**Presenter:** MARCINIEWSKI, Pawel (Uppsala University)

**Session Classification:** Production, Testing and Reliability

**Track Classification:** Production, Testing and Reliability
Electrical and Functional Characterisation with Single Chips and Module Prototypes of the 1.2 Gb/s Serial Data Link of the Monolithic Active Pixel Sensor for the Upgrade of the ALICE Inner Tracking System.

Tuesday, 12 September 2017 16:45 (15 minutes)

The upgrade of the ALICE Inner Tracking System uses a newly developed Monolithic Active Pixel Sensor (ALPIDE) which will populate 7 tracking layers surrounding the interaction point. Chips communicate with the readout electronics using a 1.2 Gb/s data link and a 40 Mb/s control link. Event data are transmitted to the readout electronics over microstrips on a Flexible Printed Circuit and a 5m long twinaxial cable.

This contribution describes the experimental characterisation activity to verify the reliability of control and data transmission for single chips and prototypes of the detector modules, in laboratory setups and beam tests.

Summary

The upgrade of the ALICE Inner Tracking System uses about 25000 specifically developed, large area Monolithic Active Pixel Sensors (MAPS), arranged in 7 cylindrical layers surrounding the interaction point. Each layer is segmented into staves. In the 3 innermost layers, a stave contains 9 sensors. Each sensor sends data directly to the readout electronics over a dedicated data link. The 4 outer layers segment staves into half-staves and modules, with one half-stave built out of 4 or 7 modules. One module combines 14 sensors in a master/slave configuration, with two master chips controlling 6 slave chips each. Every master chip has a data link to the readout electronics. Slave data is forwarded on a local bus to the master chip. The operating bit rate for the data links is 1.2 Gb/s for the three inner layers and 400 Mb/s for the four outer layers. The physical medium includes microstrip traces on the Flexible Printed Circuits and a 5 m long twin, mini-coaxial cable to the readout electronics.

The pixel sensor used is a custom designed chip named ALPIDE, fabricated in an 180 nm CMOS process. It uses a custom Data Transmission Unit (DTU), combining a Phased Locked Loop (PLL), a Double Data Rate (DDR) serialiser and a pseudo Low-Voltage Differential Signalling (LVDS) driver with pre-emphasis.

This contribution outlines the characterisation effort for assessing the DTU performance of single sensors and prototypes of the detector modules. Laboratory test setups were designed to model the final system as close as possible. The test setups use the same electrical transmission line as planned for the final system. The receiver links on the readout electronics side were implemented using the first prototype of the final readout system. Testing procedures to assess electrical, functional and jitter performance were implemented using the different prototypes of single sensors and modules. An electrical characterisation of the transmission lines for both control and data link was performed. A jitter study of the data link describes the jitter behaviour in relation to chip load and supply noise. The results were compared with the previous chip prototypes to check the improvements of the modifications made in the circuits. This study provided input to establish the operating conditions and margins for reliable transmission of data.

An irradiation campaign was performed, testing the chip and in particular the Data Transmission Unit under radiation in a 30 MeV proton beam. The behaviour of the DTU's components was monitored during the tests, analysing signs of upsets or functional interrupts of the circuitry. Received bit sequences were checked online for bit errors, event data from test pulses collected for offline
analysis. No functional or data upset was observed during irradiation. There was no observation of an increase of jitter due to irradiation.

This contribution will describe the setup, the characterisation techniques and the experimental results, focusing on the electrical and jitter performance. It will include results from the irradiation tests.

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**Presenter:** BONORA, Matthias (University of Salzburg (AT))

**Session Classification:** POSTER Session

**Track Classification:** Production, Testing and Reliability
Development of Depleted Monolithic Pixel Sensors in 150 nm CMOS technology for the ATLAS Inner Tracker Upgrade

Thursday, 14 September 2017 11:30 (25 minutes)

This work presents a Depleted Monolithic Active Pixel Sensor (DMAPS) prototype manufactured in LFoundry 150 nm CMOS process. The described device, named LF-Monopix01, was designed as a proof of concept of a fully monolithic sensor capable of operating in the environment of outer layers of ATLAS Inner Tracker upgrade for High Luminosity LHC. Implementing such device in the detector will result in a lower production cost and lower material budget compared to presently used hybrid designs. In the presentation the chip architecture will be described, followed by simulation and measurement results.

Summary

There has recently been an increased interest within the high energy physics community in employing CMOS manufacturing processes to develop active silicon pixel sensors on depletable substrates. In order to better organize the design efforts an R&D collaboration called “CMOS demonstrator” was started within ATLAS with a goal of qualifying the available CMOS technologies to build depletable high performance and cost efficient CMOS detectors with low material budget for the ATLAS ITk upgrade. Within this collaboration several prototypes have been developed in few different technologies. Presented measurement results were encouraging, showing that CMOS sensors might be a feasible choice for ATLAS ITk, but vast majority of designs developed so far were either passive sensors or sensors with an integrated first stage of analog front-end, thus still requiring bump-bonding or gluing to a dedicated readout chip. A natural next step is an attempt to integrate sensor, analog front-end and readout circuit into one chip. This paper presents such a device – a DMAPS prototype baptized LF-Monopix01 designed in LFoundry 150 nm CMOS technology. The chosen process features quadruple wells and a charge collection node is formed by a very deep N-well embedding the in-pixel electronics. A deep P-type layer allows isolating transistor N-wells from the very deep N-well, so that full CMOS capability is achieved within the pixel. The readout of the pixel array follows the “column drain” architecture. In every pixel, the charge signal is first amplified by a Charge Sensitive Amplifier (CSA), and then compared to an adjustable threshold by a discriminator. Two 8-bit time stamps corresponding to the leading and trailing edge of the discriminator output, respectively, are stored in RAM cells. A hit in a pixel initiates token signal propagation to a readout controller, which initiates the priority scan, such that hit pixels are successively read out. The data is serialized and sent off-chip at a rate of 160 Mbps by a LVDS driver. For design simplicity, the readout controller is implemented off-chip in a FPGA. The design contains a matrix of 129×36 pixels, with a pixel size of 250 µm × 50 µm. The matrix is composed of 9 pixel flavours, evenly distributed into four columns each. The flavours differ by designs of the CSA architecture (2 types), the discriminator architecture (2 main types) and the placement of pixel readout circuitry (in-pixel or at the periphery).

The design was fabricated on a high resistivity (> 2 kOhm•cm) P-type substrate. First measurement results show that readout circuitry is fully functional and sensor breakdown voltage is above 280 V. During the presentation the prototype will be described in detail, followed by simulation results and the latest measurements results.
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Presenter: RYMASZEWSKI, Piotr (University of Bonn (DE))

Session Classification: ASIC

Track Classification: ASIC
Data Acquisition Board for a Beam-Tagging Hodoscope Used in Hadrontherapy Monitoring

Wednesday, 13 September 2017 17:45 (15 minutes)

This paper presents a data acquisition board associated with a beam-tagging hodoscope to be used in hadrontherapy for ion-range monitoring. The board was designed to couple to a 64-channel multi-anode photomultiplier, and to meet the hodoscope's requirements: 1-mm spatial resolution and 1-ns temporal tagging resolution, with 100-MHz counting rate capability. It mainly consists of two 32-channel readout ASICs, a signal-processing control FPGA and a 3-Gbit/s optical transceiver to a µTCA-based data acquisition system. The board was fabricated and its operation was verified by test bench. Beam tests (with hodoscope and acquisition system) have been scheduled and are being prepared.

Summary

There have been suggested methods to implement real-time ion-range monitoring for quality assurance in hadrontherapy. Prompt gamma (PG) detection is a promising technique and several prototypes using various modalities are under developments worldwide. Some systems use time-of-flight (TOF) measurements to discriminate PG from the neutron background (e.g. TOF PG cameras), while others employ Prompt Gamma Timing approach for indirect measurement of ion range. All require precise measurement of arrival time of incident ions detected by a beam-tagging hodoscope. One type of such hodoscopes for this purpose has been developed by CLaRyS collaboration network (consisting of several IN2P3 laboratories). It consists of an array of scintillating fibers in vertical and horizontal directions. The optical fibers are coupled to multi-anode photomultipliers.

We report here the development of a data acquisition (DAQ) board to be associated with a scintillating-fiber-based hodoscope. The board incorporates two 32-channel readout ASICs, a FPGA (StratixII GX EP2SGX30C/D) and an optical transceiver (enhanced small form-factor pluggable transceiver). Each readout ASIC also integrates a time-to-digital converter (TDC) and a multiplexed analog output for monitoring of scintillating fibers ageing. The FPGA performs data processing, transmission and slow control. The transceiver performs electrical-and-optical-signal conversion and bi-directional transmission at 3 Gbit/s rate. Via an optical fiber, the board can be connected to a µTCA-based data acquisition system. The board also include a clock jitter cleaner (LMK04828) to generate several clock signals from an external reference clock. The board supports two types of triggers: a self-trigger for stand-alone tests and an external trigger for coupling with imaging systems like prompt gamma cameras. In order to optimize data throughput, the transceiver uses only basic 8-/10-bit protocol and fully exploits specific control symbols to distinguish different types of frames (control, monitoring, and data).

The board was designed to meet the system requirements: 1-mm spatial resolution, 1-ns timing resolution, and 100-MHz counting rate capability. To ensure time-measuring precision and transmission reliability, phase determination and frequency synchronization techniques were implemented. The board was fabricated and its operation was verified by test benches. Beam tests (with hodoscope and acquisition system) have been scheduled and are being prepared.

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Presenter:  AMINA, ANNAGREBAH

Session Classification:  POSTER Session

Track Classification:  Systems, Planning, Installation, Commissioning and Running Experience
Two optical link data transmission ASICs have been designed for the ATLAS Liquid Argon (LAr) Calorimeter Phase-I upgrade. The latency of each ASIC and its corresponding receiver implemented in the back-end FPGA, are critically specified to be less than 150 ns. We present the latency measurements of two ASICs. The optical link latency measurement results indicate that both ASICs achieve their design goals and meet the latency specification. The consistence between the ASIC design simulation and measurements validates the ASIC characterization.

Summary

In the ATLAS Liquid Argon (LAr) Calorimeter Phase-I upgrade, the optical link is used to transmit the front-end detector data to the back-end control room. Two Application Specific Integrated Circuits (ASICs), LOCx2 and LOCx2-130, have been designed for such an upgrade. Each ASIC has two channels of serializers with custom encoders. LOCx2 is designed and fabricated in a 250-nm Silicon-on-Sapphire CMOS process and has been produced and is in packaging processing. LOCx2-130 is fabricated in a 130-nm bulk CMOS process to back up LOCx2. The latency budget is 75 ns for each ASIC itself and 150 ns for the whole link, excluding the time passing through the optical fiber. As a key specification, the latency of each ASIC and its corresponding receiver must to be validated.

We measure the ASIC latency by measuring the time difference between the input parallel data and the serial output data. The input parallel data have a special fixed pattern in an LHC clock cycle and another fixed, different pattern in all other clock cycles. For LOCx2, its scrambler functional block is turned off, so that we can locate the position of each bit in the input parallel data and in the serial output data. For LOCx2-130, since its scrambler cannot be turned off, we cannot identify the position of a specific bit in the output serial data. Instead, we determine the position of the nearest frame header and calculate the latency. Since there is a frame header in every 25 ns, the latency measurement of LOCx2-130 has an ambiguity of n * 25 ns (n = 1, 2, 3...). Such an ambiguity is eliminated later by comparing to the ASIC simulation and the latency of the whole link.

For the whole-link latency, we generate a pulse aligned with the special input parallel pattern feeding into the ASIC and another pulse aligned with the recovered special pattern on the receiver side. The two pulses are logically OR’d together and output via a pair of different pins of the FPGA to an oscilloscope. The latency is the time difference between these two pulses. The use of a single output pin eliminates the delay skew of output pins and reduces the measurement error. The measurement results show that the ASIC latency is from 24.0 ns to 27.2 ns and the latency of the whole link is from 68.2 ns to 74.3 ns for LOCx2. The ASIC latency is from 34.4 ns to 40.7 ns and the latency of the whole link is from 100.2 ns to 106.2 ns for LOCx2-130. The optical link latency measurement results indicate both ASICs achieve their design goals and meet the latency specification. The ASIC latency measurement matches with the ASIC simulation. The latency of the whole link is consistent with the measurement using the Xilinx ChipScope Pro Analyzer tool. The consistence between the ASIC design simulation and measurements validates the ASIC characterization.
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Session Classification: POSTER Session

Track Classification: ASIC
The Characterization of a Low-Power, Low-Latency, Dual-Channel Serializer ASIC for Detector Front-End Readout

We present the design and test results of LOCx2-130, a low-power, low-latency, dual-channel serializer ASIC for detector front-end readout. LOCx2-130 consists of two serializer channels with custom encoders and each channel operates at 4.8 Gbps. The ASIC is fabricated with a commercial 130-nm CMOS process and is packaged in a 100-pin QFN package. LOCx2-130 consumes 440 mW and achieves a bit error rate of below 10-12 with a latency of from 34.4 ns to 40.7 ns.

Summary

ASIC serializers are needed for the front-end optical readout due to the demand on data bandwidth, high channel density, low power consumption, low transmission latency and radiation tolerance. Based on a commercial 130-nm CMOS process, we have designed a dual-channel serializer ASIC LOCx2-130 to meet these demands, in particular in the ATLAS Liquid Argon Calorimeter Phase-I trigger upgrade.

LOCx2-130 has two serializer channels and each channel operates at 4.8 Gbps. The two channels share a PLL. Each channel has a custom data encoder called LOCic and a serializer. The LOCic receives the data from the upstream ADCs to form data frames and is digitally synthesized with the transmission latency optimization. The LOCic is protected with the triple modular redundancy (TMR) technique. LOCx2-130 can interface one out of three types of ADCs, a 12-bit ASIC ADC, a 12-bit commercial ADC ADS5272 and a 14-bit commercial ADC ADS5294. A synchronous First-in-First-Out (FIFO) accommodates a clock skew of up to 3.125 ns between the two ASIC ADCs. The serializer and the PLL are adapted from a design that originates from the CERN’s GBTX ASIC. We slightly modified the design to share a PLL between two serializers. The GBTX designer Paulo Moreira reviewed the whole design of LOCx2-130.

LOCx2-130 has been packaged in a 100-pin plastic quad-flat no-leads (QFN) package and has been evaluated. The test system consists of a test board and a Kintex-7 FPGA. The FPGA implements ADC emulators (ASIC ADC, ADS5272 and ADS5294) as the input of the LOCx2-130 test board. The FPGA-embedded input/output delay modules are used in the ADC emulators to ensure signal alignment. The FPGA also implements two link receivers. Each link receiver includes the deserializer of a Multiple-Gigabit Transceiver (MGT), a LOCic decoder, and an error logger. The deserializer converts the 4.8 Gbps serial data stream into parallel data. Then the LOCic decoder recovers the original ADC data and checks if there are errors in the recovered data. The error logger records error types and time stamps.

Our test shows the power consumption of LOCx2-130 is 440 mW at the design speed of 4.8 Gbps. In the link test, the receiver implemented in the FPGA identifies the date frame boundary correctly and the frame data passes the CRC check. The output of the serializer passes the eye mask test with a bit error rate of below 10-12. The latency of the whole link, including the receiver and the serializer, is from 100.2 to 106.2 ns and the chip latency is from 34.4 ns to 40.7 ns. As expected, the serializer tolerates 3.125 ns clock skew between two input ASIC ADCs. Irradiation tests will be carried out in the coming months and will be presented in the workshop and in the proceeding.
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Presenter: Dr GONG, Datao (Department of Physics, Southern Methodist University, Dallas, TX 75275, USA)

Session Classification: POSTER Session

Track Classification: ASIC
The Quality Assurance Test of a VCSEL Driver ASIC for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade

Tuesday, 12 September 2017 17:15 (15 minutes)

A VCSEL driver ASIC, LOCld, has been designed for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade. In total about 7000 chips have been produced and are in packaging process. We present the quality assurance test aiming at screening all functional chips before they are assembled into optical transmitter modules. A detailed test procedure is proposed. A dedicated test board has been designed and in fabrication. The test results will be present in the workshop and in the proceeding.

Summary

LOCld is a dual-channel vertical-cavity surface-emitting laser (VCSEL) driver ASIC designed for the optical data link to read out the ATLAS Liquid Argon Calorimeter. LOCld will be assembled in MTx, a dual-channel optical transmitter module and in MTRx, an optical transceiver module. In MTx each channel of LOCld operates at 5.12 Gbps. In MTRx, only one channel of LOCld operates at 4.8 Gbps and the other channel is not powered up. In total about 7000 LOCld chips have been produced and are in packaging process. In order to ensure the functionality of LOCld and save the production cost of MTx/MTRx, a quality assurance (QA) test will be conducted on each LOCld chip. Only the chips passing the QA test will be assembled in MTx or MTRx.

A detailed QA test procedure is proposed. The QA test includes an I2C configuration test, an eye mask test, the bias current range, and a bit-error-rate (BER) test. Firstly, for the I2C test, we use the I2C interface to read the internal registers of each chip after power-up and write the registers and read back the configuration registers. Secondly, a custom eye mask at 5.12 Gbps is used to screen the eye diagram of each the ASIC. The modulation current is set to an optimal value estimated from the prototypes. The power consumption will be recorded. Those chips with power consumption beyond three times of standard deviation away from the average value will be discarded. Thirdly, the minimum and maximum of the bias current of LOCld will be measured. Finally, about 1% of the chips from each wafer will be put in a BER test for 15 minutes.

A dedicated test board has been designed and is in fabrication process. Four channels of two chips will be tested at the same time with a single test board. Each chip is placed in a socket. The single-channel signal in a pattern of a pseudo-random binary sequence 2^7-1 from a signal generator of a bit error rate tester will be fanned out to two chips under test. The output signals of each chip will be connected to differential probes of a high-speed real-time oscilloscope.

The QA test is planned in June and July of 2017. The test results will be presented in the workshop and in the proceeding.

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**Presenter:** LIU, Tiankuan (Southern Methodist University (US))

**Session Classification:** POSTER Session

**Track Classification:** Production, Testing and Reliability
The Quality Assurance of a Low-Latency, Low-Overhead, Dual-Channel Transmitter ASIC for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade

Tuesday, 12 September 2017 17:00 (15 minutes)

We present the quality assurance (QA) test of LOCx2, a low-latency, low-overhead transmitter ASIC for the ATLAS Liquid Argon Calorimeter Phase-I upgrade. In the QA test we will screen about 7000 LOCx2 chips to ensure their basic functionality. The QA test system, including two printed circuit boards, firmware, software, are under development. All tests are automatically conducted and controlled by LabVIEW software running on a computer. The test results will be reported.

Summary

The ATLAS Liquid Argon Calorimeter (LAr) Phase-I trigger upgrade requires high-speed, low-latency data transmission to read out the LAr Trigger Digitizer Board (LTDB). To meet this requirement, LOCx2, a dual-channel transmitter ASIC, has been designed, each channel operating at 5.12 Gbps. LOCx2 can accommodate data from three types of ADCs, an ASIC ADC and two Commercial-Off-The-Shelf (COTS) ADCs. About 7000 LOCx2 chips have been produced and are in packaging process. In order to ensure the basic function of the chips before assembly, a Quality Assurance (QA) test must be conducted.

The QA test measures the serial output eye diagram, the Bit Error Rate (BER) and the I2C interface of each chip. We also plan to sample about 1% of the chips that pass the above tests in each wafer to measure the Phase-Locked-loop (PLL) tuning range, the jitter of the serial output, and check the 3.125-ns skew tolerance in the ASIC ADC mode.

The QA test system has two setups. The first setup is for eye diagram observation, the PLL tuning range tests and serial output jitter measurement. The eye diagram, the PLL tuning range, and the serial output jitter are measured by using a high-speed real-time oscilloscope. The eye diagram and the serial output jitter are observed on the 5.12-Gbps serial output signals. The PLL tuning range is measured on the PLL output signal when the input clock frequency is adjusted. The printed circuit board (PCB) used to characterize the chip before will be used in the test. To shorten the test, LabVIEW will be used to control automatically the procedure and record the test results.

The second setup is for the I2C interface, the BER, and input skew tests. The BER test will be measured under the combination of three different power supply voltages (2.25 V, 2.5 V, 2.75V) and three ADC types. The BER test is the most time-consuming part. In order to shorten the BER test time, a QA test system is being developed so that six chips are tested simultaneously. The system includes a commercial FPGA evaluation board KC705, two printed circuit boards (PCBs), FPGA firmware, and software written in LabVIEW to control the system. KC705 is used in the system as ADC data generators and the data link receivers with error loggers. Since the KC705 does not have enough pins to output ADC signals to six chips, only one ADC emulator is implemented in the FPGA. Two test PCBs are being developed. The ADC emulator signals from the FPGA are fanned out into six groups on the first PCB. Twelve pairs of differential high-speed signals from six chips are output to the FPGA, four pairs via the first PCB and the other eight pairs via the second PCB and coaxial cables. In order to test the BER automatically, software is developed in LabVIEW to control the test process.
All the 7000 LOCx2 chips will be tested in this summer. The QA test result will be presented in the workshop and the proceeding.

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**Presenter:**  LIU, Tiankuan (Southern Methodist University (US))

**Session Classification:**  POSTER Session

**Track Classification:**  Production, Testing and Reliability
A next generation control infrastructure to be used in Advanced TCA (ATCA) blades at CMS experiment is being designed and tested. Several ATCA systems are being prepared for the High-Luminosity LHC (HL-LHC) and will be installed at CMS during technical stops. The next generation control infrastructure will provide all the necessary hardware, firmware and software required in these systems, decreasing development time. It includes an Intelligent Platform Management Controller (IPMC), a Module Management Controller (MMC) and an Embedded Linux Mezzanine (ELM) processing card. The chosen architectures, their testability, integration and the advantages over existing solutions will be discussed.

Summary

Several institutes are presently designing hardware, firmware and software that will be used in CMS for data taking during the High Luminosity LHC (HL-LHC) physics runs, starting in 2025. Most of the architectural choices have been focused in designing Advanced TCA (ATCA) blades and, as part of the PICMG 3.x standard, each blade needs to implement a set of control and management functionalities.

The next generation control infrastructure presented includes three different hardware systems that together implement the PICMG 3.x standard, provide additional features, flexibility and decrease the time necessary to design and test an ATCA blade.

The implemented control infrastructure consists of:

- An Intelligent Platform Management Controller (IPMC) mezzanine: Designed to be the blade management controller, containing a low power Xilinx ZYNQ system-on-chip (SoC) FPGA running RTOS to handle time critical sensitive tasks. Open hardware and firmware allows extensive user customization by taking advantage of several general purpose inputs/inputs (GPIOs) available together with the ZYNQ’s Programming Logic (PL). The mezzanine measures 82mm by 30mm and can be easily replaced.

- A Module Management Controller (MMC): Used to control and manage several individual sub modules in an ATCA blade. The blade IPMC will control one or more MMCs using I2C. An Atmel SAM4N Cortex-M4 microprocessor running RTOS handles critical tasks and alarms. A reference design is available to be implemented in a custom hardware layout.

- An Embedded Linux Mezzanine (ELM) processing card: Used as the primary blade on-board computer, featuring a high-end Xilinx ZYNQ SoC running Linux. It provides high speed ethernet access to the blade and all peripherals connected to the ELM. Eight multi-gigabit transceivers are also available for extended connectivity as well as several high performance GPIOs. Compatible Xilinx processing FPGAs (e.g. Virtex-7, Virtex Ultrascale) can exploit the ZYNQ architecture by using AXI chip-to-chip interface for a seamless integration inside the Xilinx ecosystem. The ELM mezzanine measures 84mm by 75mm and has been designed with upgradability in mind. The talk will cover the architecture choices of the hardware modules, how they are being tested, their performance results, how they fit in the ATCA environment and their advantages over existing solutions.
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Session Classification: POSTER Session

Track Classification: Systems, Planning, Installation, Commissioning and Running Experience
The SALT, a 128-Channel Readout ASIC for Upstream Tracker in the Upgraded LHCb Experiment

Tuesday, 12 September 2017 14:50 (25 minutes)

SALT is a 128-channel readout ASIC for silicon strip detectors in the upgraded Tracker of LHCb experiment. It will extract and digitise analogue signals from the sensor, perform digital processing and transmit serial output data. SALT is designed in CMOS 130-nm process and uses a novel architecture comprising of analogue front-end and ultra-low power (<0.5 mW) fast (40 MSps) sampling 6-bit ADC in each channel. The first version of full 128-channel prototype was already tested and the second version was submitted. The design and tests results will be presented.

Summary

Present Large Hadron Collider beauty (LHCb) detector performance is limited by readout electronics and data acquisition architecture. After the upgrade of LHC machine it will be capable to deliver more than one order of magnitude higher luminosity than presently used by the LHCb detector. To achieve this goal various detectors will need a new faster front-end electronics with the read-out running at the bunch-crossing rate of 40 MHz.

Silicon strip detectors in the upgraded Upstream Tracker (UT) of LHCb experiment will be read out by new Application Specific Integrated Circuit (ASIC) called SALT (Silicon ASIC for LHCb Tracking). This 128-channel chip, designed in CMOS 130 nm technology, extracts and digitises analogue signals from the sensor, performs Digital Signal Processing (DSP) and transmits a serial output data. The ASIC uses a novel architecture comprising an analogue front-end and an ultra-low power (<0.5-mW) fast (40-MSps) sampling 6-bit ADC in each channel. The front-end comprises a charge preamplifier and a fast ($T_{peak}=25$ns and fast recovery) non-standard shaper with complex poles and zeros in transfer function, required to distinguish between the LHC bunch crossings at 40-MHz. The front-end should work with sensor capacitances between 5–20-pF. An ultra-low power (<1-mW) DLL is used to control precisely the ADC sampling phase.

Digitised data from each ADC channel are processed in a DSP block which first subtracts pedestals and calculates mean common mode, subtracted then in each channel. The last DSP step is zero suppression (ZS). After ZS the data are buffered in SRAM, then a packet is formed and sent to DAQ via a number of serial DDR e-links. An ultra-low power (<1-mW) PLL is used in data serialization and fast data transmission circuitry.

An 8-channel prototype of the SALT, comprising most important functionalities, was designed, fabricated, successfully tested and the results were already presented (TWEPP 2016).
The present 128-channel prototype is a complete ASIC for LHCb detector. It includes, except functionalities mentioned above, internal generation of common mode voltage, monitoring ADCs (for PLL, DLL and internal DACs), band-gap reference source, variable number of active e-links, hybrid suitable power distribution, etc.

The 128-channel SALT prototype was tested and found functional. In the first step, the digital functionality and operation were extensively tested (serializers and deserializer with DDR e-links, the DSP operations, fast and slow control interfaces, etc.) and, except several small features, all functionalities were correct. After verification of digital processing and data transmission analogue pulses were observed, using DLL to shift the ADC sampling phase. The ADC performance fully agrees with expectations. The analogue front-end measurements qualitatively agreed with simulations, although quantitative results on noise and mismatch between channels showed that improvements in the design are still needed. The results of tests with discussion of possible improvements and planned corrections will be presented.

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Presenter: SWIENTEK, Krzysztof Piotr (AGH University of Science and Technology (PL))

Session Classification: ASIC

Track Classification: ASIC
Development of a High-Throughput Tracking Processor on FPGA Boards

Tuesday, 12 September 2017 15:40 (25 minutes)

We present the latest results on the prototype of a tracking processor capable of reconstructing events in a silicon-strip tracker at about 40 MHz event rate with sub-microsecond latency. The processor is based on an advanced pattern-recognition algorithm, called "artificial retina", inspired to the vision system of the mammals. We design and implement this processor on a board equipped with Altera Stratix V FPGA's. Future applications of this novel approach as real-time track trigger at LHC experiments are also discussed.

Summary

Computing and storage demands of future LHC experiments at very high luminosity represent a challenge for HEP data processing, which calls for an efficient and scalable usage of the hardware. The increasing input rates and growing complexity of physics events, along with the finite bandwidth for writing to long term storage, call for sophisticated and computing intensive trigger algorithms. The available CPU time and I/O bandwidth, to and from storage, limit the amount of offline data reprocessing that can be performed. Moving part of the data processing, e.g. track reconstruction, to the online stage has multiple benefits: the stored event size can be reduced, trigger selection may be improved, and less processing has to be done offline.

While Moore’s law for CPU was slowing down, FPGAs performances have increased steadily in the last few years. These devices are also particularly suited to perform repetitive tasks, such as tracking, with low power consumption, and they also allow for low and fixed latencies. Therefore an FPGA-based tracking unit could be integrated in the DAQ architecture at a moderate cost and act as a “track-detector”, thus making event reconstruction primitives immediately available to event-building and high-level-trigger farms.

Our goal is to develop and implement a parallel computational methodology that allows to reconstruct events with an extremely high number (>100) of charged-particle tracks in pixel and silicon strip detectors at 40 MHz, thus matching the requirements for processing LHC events in real time. Our approach relies on a massively parallel pattern-recognition algorithm, dubbed “artificial retina”, inspired by studies of the processing of visual images by the brain as it happens in nature. The artificial retina algorithm is based on two main concepts. First, for each track pattern we compute a quantity that measures how any combination of entered hits matches the pattern itself. Second, the hit sequence delivered to a pattern is an appropriate subset of all the events hits, reducing the data bandwidth involved in the process. Preliminary studies on simulation already showed that high-quality tracking in large detectors is possible with sub-microsecond latencies when this algorithm is implemented in modern FPGA devices.

After successfully developing a first prototype based on a 6-layer silicon detector and implementing that on an FPGA board with 4 Altera Stratix III chips, we port the system to a faster Stratix V FPGA chip. After additional optimization on this device, we were able to process events with low occupancy at 40 MHz rate and 0.5 us latency. We also present a feasible implementation of a larger scale system distributed over multiple commercial PCIe boards carrying Altera FPGA’s. Further possible developments are also discussed, that will enable even greater performance, including 3D reconstruction, and “embedded operation”, in which the reconstructed tracks are transparently incorporated with the data being read out.
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Presenter:  CENCI, Riccardo (SNS and INFN-Pisa, Italy)

Session Classification:  Trigger

Track Classification:  Trigger
Upgrade of the YARR DAQ System for the ATLAS Phase-II Pixel Detector Readout Chip

Wednesday, 13 September 2017 17:00 (15 minutes)

Yet Another Rapid Readout (YARR) is a DAQ system based on a software driven architecture using PCIe FPGA boards. It was designed for the readout of current generation ATLAS Pixel detector readout chips, which have a readout bandwidth of 160 Mb/s. YARR has been upgraded to accommodate the higher 5 Gb/s bandwidth of the next generation readout chip in development by the RD53 collaboration for the Phase-II upgrade of the ATLAS and CMS detectors. The performance results of the migration to a new PCIe FPGA board, the PLDA XpressK7, will be presented.

Summary

YARR utilises commercial-off-the-shelf PCIe FPGA cards as a reconfigurable I/O interface, which act as a simple gateway to pipe all data from Pixel detector modules via the high speed PCIe connection into the host system’s memory. All further data processing can be performed in software, which gives the advantages of high flexibility and being independent of specific hardware platforms. This readout architecture can directly interface with software emulators of Pixel detector readout chips. This greatly aids the software development as a software emulator removes the dependency on hardware availability and is also a great tool to reduce the threshold for new users to test the DAQ system. Furthermore, the emulator can be used to set up a test environment of the software package - a crucial feature to enable continuous integration and maintain a high quality of the software.

For the readout of the current generation Pixel detector readout chip, YARR uses the SPEC board which features a Xilinx Spartan 6 FPGA and a local PCIe bus bridge IC. To cope with the much higher bandwidth of the next generation readout chips, the newer Xilinx Series 7 FPGAs have to be used. Furthermore, to increase the portability of the firmware to a broader range of PCIe boards, the integrated PCIe endpoint will be used after migration instead of a local bus bridge. Results of the firmware migration of the XpressK7 card with a Xilinx Kintex 7 FPGA, including performance benchmarks of the scatter-gather DMA transfers, will be presented.

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Presenter:  WHALLON, Nikola Lazar (University of Washington (US))

Session Classification:  POSTER Session

Track Classification:  Programmable Logic, Design Tools and Methods
Characterization and Verification Environment for the 65 nm Pixel Readout-Chip RD53A

Thursday, 14 September 2017 11:45 (20 minutes)

For the Phase II Upgrade of LHC, new hybrid silicon pixel detectors are required for charged particle tracking. The RD53 collaboration is currently designing a large-scale prototype sensor readout chip “RD53A”, which will be available soon. The SiLab group at the University of Bonn is highly involved in testing/verification and several chip design tasks.

A modular and versatile test- and data acquisition system for this next generation pixel readout is being developed to perform single-chip and module measurements. The concept and implementation of this FPGA-based system, the software framework and first test results of RD53A will be presented.

Summary

Due to significantly increased hit rates, new readout chips with highly complex digital architectures will have to deliver drastically increased data rates and ensure unprecedented radiation tolerance, especially close to the interaction point. The collaboration “RD53” was formed to approach these challenges, by designing a pixel readout chip in a 65 nm CMOS process, suitable for the inner layers of both the ATLAS and the CMS experiment.

The design efforts for the 500-million-transistor RD53A chip are split in two fundamental parts: Full custom analog and synthesized digital. In order to verify the digital design and to characterize the prototype chips, a test- and data acquisition (DAQ) environment, consisting of software frameworks and dedicated FPGA-based hardware, is currently being developed in Bonn. The aim is to use the same Verilog/Python framework for the DAQ system hardware as well as during the design verification process. This is achieved by utilizing a Co-Simulation testbench environment and including the System-Verilog repository, which finally will be used to synthesize the digital part of RD53A into CMOS logic for production. This approach also allows for valuable feedback to the digital designers and more efficient firmware development, because it can already be evaluated with the behavioral model of the chip prior to its submission.

Several aspects of the existing USBpix3 DAQ system must be adapted for the needs of RD53A, in order to cope with the increased data rate of up to 5 Gbit/s using the Aurora 64b66b protocol in single- and multi-lane configurations. This requires a new variant of USBpix3 with several Multi-Gigabit-Transceiver channels, DDR3 memory for buffered readout and a new dedicated Single Chip Card (SCC) for the first measurements of the prototype chips. The SCC hosts the wire-bonded device under test, provides thermal management and allows for multiple powering schemes, including serial powering. As soon as the prototypes are available, characterization measurements will be performed with the new DAQ system.
Jochen Christian (University of Bonn (DE)); WERMES, Norbert (University of Bonn (DE))

**Presenter:** VOGT, Marco (Universitaet Bonn (DE))

**Session Classification:** Programmable Logic, Design Tools and Methods

**Track Classification:** Programmable Logic, Design Tools and Methods
A SEU-Immune Self-Tuned Pixel Chip Architecture

Readout chips of hybrid Pixel detectors use low power amplifier and threshold discrimination to sense and digitise charge deposited in semiconductor sensor. Due to variability in CMOS transistors each pixel circuit needs to be calibrated individually to achieve response uniformity. Traditionally this is addressed by programmable threshold trimming in each pixel. In this presentation a self-adjusting threshold mechanism is presented, which corrects the threshold for both spacial and time variation. The behaviour of this circuit has been simulated to evaluate its performance compared to traditional calibration results. The simulation results show that this mechanism can perform equally well, but eliminates instability over time and is immune to single event upsets.

Summary

The self-adjusting mechanism exploits the electrical noise as relative measure for the threshold and automatically adjusts the threshold to always achieve the same frequency of noise hits passing the threshold. The mechanism is implemented in form of an up/down counter and combinatorial filter logic, which replaces the traditional trim DAC register. This circuit could be a key technology to enable smooth detector operation in HL-LHC conditions, as it mitigates a variation in pixel threshold cause by Single-Event-Upsets of digital logic and changing transistor characteristics resulting from change in temperature or induced by ionising radiation.

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Session Classification: POSTER Session

Track Classification: Radiation Tolerant Components and Systems
Measurements and Simulations of Single-Event Upsets in a 28 nm FPGA

Thursday, 14 September 2017 08:55 (25 minutes)

Single-Event Upsets (SEUs) in the configuration memory of a 28 nm FPGA, used in the PANDA electromagnetic calorimeter, have been studied. Results from neutron and proton irradiations are presented. A GEANT4-based Monte Carlo simulation of SEU mechanisms in nanometric silicon volumes has been developed for studies of the energy dependence. At PANDA, a neutron flux of $1 \cdot 10^2$ cm$^{-2}$ s$^{-1}$ at the location of the front-end modules is expected at the lowest antiproton beam momentum and a luminosity of $1 \cdot 10^{31}$ cm$^{-2}$ s$^{-1}$, leading to a predicted Mean Time Between Failures of 47(10) hours per FPGA in the calorimeter.

Summary

The Facility for Antiproton and Ion Research (FAIR) is currently under construction in Darmstadt, Germany. One of the experiments at FAIR is PANDA (Anti-Proton Annihilation at Darmstadt), where antiprotons with momenta between 1.5 GeV/c and 15 GeV/c will interact in a hydrogen target.

The Electromagnetic Calorimeter (EMC) of PANDA will be read out by approximately 600 front-end digitiser modules, each featuring two 28 nm FPGAs. PANDA will be hardware-trigger-less, and these modules form the EMC software-based trigger.

Single-Event Upsets (SEUs) in the FPGA configuration memory are expected. This has been measured in the past, but to estimate the rate of such errors in PANDA, information about the energy dependence of the SEU cross section is needed. This may be obtained through irradiations at known particle energies, combined with Monte Carlo simulations.

In the present work, one front-end module has been irradiated with neutrons and protons at different energies up to 184 MeV and the SEU cross sections have been determined.

The module was irradiated with neutrons at TSL in Uppsala, Sweden. The neutron beam had a continuous energy distribution between 0 and 180 MeV, and the SEU cross section was determined to be $7.4(6) \times 10^{-15}$ cm$^2$ bit$^{-1}$, assuming only neutrons above 10 MeV cause SEUs.

The module was irradiated with protons at KVI-CART in Groningen, the Netherlands. Measurements were performed at three beam energies: 80, 100 and 184 MeV. The SEU cross sections at these energies were determined to be $7.9(9) \times 10^{-15}$ cm$^2$ bit$^{-1}$, $6.7(5) \times 10^{-15}$ cm$^2$ bit$^{-1}$ and $5.7(6) \times 10^{-15}$ cm$^2$ bit$^{-1}$, respectively.

The measured cross sections agree with previous measurements, validating the experimental procedure.

A GEANT4 model of a memory cell containing four cubic Sensitive Volumes (SVs) has been developed. Neutrons and protons with energies matching those in the experiments were directed into the cell, and the SV size $d^3$ and the critical energy required to cause an SEU, $E_{\text{crit}}$ were fitted to give the best agreement with experiments. With the resulting values $d = 125(6)$ nm and $E_{\text{crit}} = 4.6(2)$ keV both the experimental neutron and proton cross sections are reproduced. With a critical energy this low, even low-energy neutrons and protons potentially cause SEUs — this will be studied in further experiments and simulations.

The PandaRoot framework was used to simulate $2 \times 10^6$ 1.5 GeV/c $p\bar{p}$ interactions in PANDA. Assuming a PANDA luminosity of $10^{-31}$ cm$^{-2}$ s$^{-1}$, the maximum flux of neutrons at the location...
Measurements and Simulations of the EMC digitisers was determined to be $1 \times 10^2 \text{ cm}^{-2} \text{ s}^{-1}$, giving a Mean Time Between Failures (MTBF) of 47(10) hours per FPGA. Dependence of the MTBF on pbar momentum and luminosity will be studied further to determine the need for error mitigation.

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**Presenter:** PRESTON, Markus (Stockholm University (SE))

**Session Classification:** Radiation Tolerant Components and Systems

**Track Classification:** Radiation Tolerant Components and Systems
KlauS4 is a 7-channel mixed-mode Silicon-Photomultiplier readout ASIC for imaging calorimetry at a possible future linear collider, where one key aspect is the low-power consumption of the readout ASICs. Each channel consists of a low-noise front-end with two gain branches to deal with a large input signal range, and a 10-bit power efficient SAR ADC to digitize the charge information; a common digital part for data storage and transmission is also implemented into this chip. For each channel, an additional pipelined stage is used to increase the quantization resolution to 12-bit when necessary. Detailed design of the ASIC, results on characterization measurements and first test-beam results will be presented.

Summary

A high granular imaging calorimeter system with a large number of channels is planned to be operated at future linear collider experiments. For such a system the analog hadron calorimeter (AHCAL) of the CALICE collaboration is being developed; its concept is based on organic scintillator tiles read out by silicon-photomultipliers connected to highly integrated readout electronics. Due to the high integration and the dense environment, the used readout ASICs are required to dissipate not more than 25 μW per channel when being power pulsed with >0.5% duty cycle.

The analog front-end is designed to achieve sufficient SNR for a single pixel signal using low-gain SiPMs, while allowing charge measurements for the full sensor dynamic range. A current conveyor structure is used for the input stage to lower the input impedance. Two branches for charge integration with different gains are implemented: A high-gain branch for single pixel signals mainly required for calibration and a low-gain branch spanning the large charge range. An automatic gain-selection is implemented to determine which gain branch is digitized. In addition a comparator is implemented to generate a digital trigger signal for time stamping with sub-nanosecond resolution; the trigger is also used to initiate the ADC conversion.

The amplitude of the output signal from the front-end is digitized by an ADC to get the charge information. A 10-bit Successive-Approximation-Register ADC is adapted to minimize the power consumption. To measure the single pixel signal from SiPMs with the intrinsic gain as low as 105, an addition pipelined SAR stage is implemented to increase the quantization resolution to 12-bit.

The design of the front-end and the ADC were already presented in TWEPP14 and TWEPP15. The current version, KLauS4, combines both parts into a single channel. In the new chip, 7 channels as well as the digital part for data transmission and configuration are implemented.

The performance of the chip has been characterized in detail under laboratory conditions. The equivalent noise charge for the high-gain stage is measured to be as low as 5 fC for a total input capacitance less than 100 pF. The low-gain branch can achieve 1% INL/FSR linearity up to 150 pC. For the 10-bit ADC, the DNL is measured to be -0.52/+0.14 LSB; for the ADC in 12-bit mode, the obtained DNL is -0.44/+0.36 LSB. Single-photo-spectra (SPS) for 10 μm pitch SiPMs have been obtained showing a clear separation of the photo-peaks. In power-pulsed operation, less than 10 μs is needed for the front-end to settle. The performance results for the chips with and without power-pulsing are compared with good agreement.

Test measurements have also been carried out at the DESY test-beam facility using a three-layer setup comprised of scintillator tiles, 25 μm SiPMs and KLauS4 ASICs. The multi-channel operation
could be verified recording MIP spectra in all of the 15 equipped channels. Various analog and
digital functionalities were tested successfully, such as the auto-gain selection and power-gating,
which show good agreement with the pre-selected and non-gated spectra, respectively.

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**Session Classification:** ASIC

**Track Classification:** ASIC
Design and Characterisation of the Monolithic Matrices of the H35DEMO Chip

Design and Characterisation of the Monolithic Matrices of the H35DEMO Chip

Wednesday, 13 September 2017 11:30 (25 minutes)

The H35DEMO chip is a HV/HR-MAPS demonstrator of 18.49 mm x 24.4 mm, fabricated with a 0.35 µm HVCMOS process from AMS in four different substrate resistivities. The chip is divided into four independent matrices with a pixel size of 50 µm x 250 µm. Two of the matrices include all the digital readout electronics at the periphery. This contribution describes the two standalone matrices of the H35DEMO chip and will present the results of two testbeams carried out with unirradiated and irradiated samples with different substrate resistivities.

Summary

High Voltage/High Resistivity Depleted Monolithic Active Pixels (HV/HR-DMAPS) is a technology which is being investigated for the 5th layer of the Inner Tracker of the ATLAS detector at HL-LHC. Currently, several groups have started to develop some demonstrators in order to validate this technology at large scale in different CMOS processes. The H35DEMO is the first HV/HR-DMAP demonstrator built. It was fabricated with a 350nm HVCMOS process in 4 different substrate resistivities: 20, 80, 200, and 1000 Ω•cm. It includes four different matrices with a pixel size of 50 µm x 250 µm. The pixels of two of them include analog front-end electronics and have to be readout with an FEI4 chip. In the other two, the pixels also include analog readout electronics together with digital electronics to readout them out in the periphery.

The two standalone matrices are composed of 16 rows and 300 columns. One of the pixel matrices is called nMOS because the analog front-end electronics are mainly composed of a preamplifier, a shaper, and a discriminator that only uses nMOS transistors. In these pixels, the pMOS transistors are built in the DNWELL which is the collecting node. If a CMOS discriminator was used instead of a nMOS, the large voltage commutations would inject noise directly to the DNWELL. Two different types of nMOS discriminators were implemented. The first half of the matrix contains a simple nMOS comparator while the second half contains a more complex nMOS discriminator which compensates the time-walk. The output of the discriminators is converted to a CMOS signal in a readout cell (ROC) connected to each pixel by means of a CMOS discriminator. The second matrix is called CMOS and the pixels are like those of the nMOS matrix but with no nMOS discriminator. The output of the shaper is discriminated by a CMOS comparator placed at the readout cell connected to the pixel.

The ROCs are the same for both matrices and are placed at the periphery arranged in a matrix of 120 columns and 40 rows. They store an 8-bits global time stamp into a DRAM when a hit is detected. The architecture of these cells is column drain and the layout was made full custom in order to embed all the electronics in 125 x 20 µm². Each column is terminated with an End Of Column (EOC). It stores the time stamp and data of the read pixel.

The readout of the matrix is asynchronous, zero suppressed and triggerless. The matrix is handled by a control unit and reads sequentially the content of each EOC cell at 40MHz. The read data is passed to 2 serializers that transmit the data off-chip at 320MHz through LVDS pads.

A first testbeam was carried out at CERN in late 2016. Unirradiated samples of 200Ω•cm were used and efficiencies of around 97% were measured. A new testbeam campaign was done during April 2017 at Fermilab. This campaign was more extensive and irradiated samples with different substrate resistivities.
substrate resistivities were tested. The results of this testbeam will be presented during the conference.

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**Session Classification:** ASIC

**Track Classification:** ASIC
A high-Precision Timing ASIC for TOF-PET Applications

Wednesday, 13 September 2017 12:20 (25 minutes)

Detectors with precise time-of-flight measurement capabilities are a very active area of research in particle physics and imaging, due to their improved accuracy and background rejection. In this contribution we present a monolithic readout ASIC, developed for a novel PET scanner, featuring a 30 ps time resolution for 511 keV photons using a SiGE HBT based front-end, capable of driving large input capacitances (up to 1 pF) while using less than 150 µW/channel. A fully-functional prototype has been submitted to IHP and a full version is in an advanced stage of design.

Summary

Time-of-flight (TOF) measurement in PET scanners allows a more accurate image reconstruction and/or a lower delivered radiation dose. In conventional PET, coincidence detectors are used to determine along which line of response an annihilation has occurred. The information added by the TOF measurement allows a more accurate determination of the position of the annihilation by reducing the line of response to a short segment. In order to extract valuable information on the position of the annihilation point, a high TOF precision is required (at least < 200 ps, but higher resolutions lead to more accurate results).

To achieve a good timing performance, front-ends need to have a low equivalent noise and a fast rise time (to reduce the jitter as much as possible). SiGe BiCMOS technology is a good candidate for this application.

We are developing a fully custom ASIC to take advantage of the characteristics of the SiGe BiCMOS process for timing measurements, integrating a fully-depleted pixel matrix with a low-power BJT-based front-end per channel, integrated on the same 100 µm thick die. All the pixels are multiplexed to a single TDC to extract timing information. Each front-end includes a BJT preamplifier with active feedback, a CMOS discriminator and a calibration DAC. A triggered readout logic is included to reduce the data to be read out of the system.

The target timing resolution is 30 ps for a 511 keV photon with a 1 pF input capacitance. The front-end has a gain of ~90 mV/fC and a rise time of ~1ns. Its low power consumption of ~135 µW, makes it possible to stack multiple ASICs on top of each other, in order to increase the detection efficiency. A total of more than 1 million channels will form the complete scanner.

A full-featured prototype with a small 10-by-3 pixel matrix has been submitted in March 2017, after a number of smaller prototypes to validate each block. A full-size chip is currently being designed.

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Presenter: VALERIO, Pierpaolo (CERN)
Session Classification: ASIC
Track Classification: ASIC
KALYPSO: a 1D Detector for High-Repetition Rate Experiments at Light Sources

Wednesday, 13 September 2017 17:00 (15 minutes)

KALYPSO is a 1D imaging detector with 10 MHz frame-rate developed for high repetition-rate experiments, such as electro-optical beam profile measurements with sub-ps resolution at ANKA and Eu-XFEL. KALYPSO consists of a Si or InGaAs microstrip sensor coupled to a front-end readout, integrated with an FPGA readout card. A Low Gain Avalanche Diode (LGAD) sensor is being developed to improve the time resolution. A DAQ framework transmits data to external GPU-based clusters, where data is processed in real-time at 7 Gbytes/s and a latency in the order of a few μs. We describe the system and the experimental results.

Summary

We present KALYPSO (KArlsruhe Linear arraY detector for MHz-rePetition rate SpectrOscopy), a 1D detector with a maximum frame-rate of 10 MHz. The detector has been developed to enable shot-to-shot beam profile measurement at different accelerators operating at MHz repetition rates (i.e., 4.5 MHz at European XFEL, 10 MHz at TELBE, 2.7 MHz at ANKA in single-bunch mode). In particular, Electro-Optical Spectral Decoding (EOSD) setups use a near-IR pulsed laser to probe the beam profile with sub-ps resolution.

The main characteristic of KALYPSO with respect to other detectors is the possibility to achieve MHz repetition rates while operating in full streaming mode: data are continuously acquired and processed with minimum latency, as required in real-time beam monitors and fast-feedback systems for beam correction. KALYPSO consists of a detector board and an FPGA-based readout card.

The detector board mounts a microstrip sensor, the front-end readout ASIC and a commercial Analog-to-Digital Converter (ADC). Depending on the demanding application, the sensor is a Si or an InGaAs linear array, with 256 pixels and a pitch of 50 μm, to detect radiation in the visible and near-infrared spectrum. In parallel with the development of the system, two custom microstrip sensors are being designed: one on a 300 μm Si substrate with 25 μm pitch, and the second in Low Gain Avalanche Diodes (LGADs) technology with 50 μm thickness and 50 μm pitch.

Because of their fast charge collection time, the internal gain mechanism and the possibility to produce highly segmented detectors, LGADs are attractive for future beam diagnostic detectors at synchrotron facilities, where low-intensity light pulses are produced with extremely high repetition rates (500 MHz at ANKA in multi-bunch mode).

The sensor is connected to the readout ASIC with high-density gold ball-to-wedge wire-bonds. A dedicated readout front-end chip is used as front-end amplifier. The analog outputs are digitized by a commercial ADC at 125 MS/s and 14 bits resolution. The detector card is connected to the back-end card through an industry-standard FMC connector.

The readout card is based on a Xilinx Virtex7 FPGA and controls detector operation. Real-time data processing can be performed both on the FPGA and on Graphical Processing Units (GPUs). To enable high system performance, a direct FPGA-GPU communication has been developed based on a custom PCI-Express 3.0 Direct Memory Access engine, with a throughput of more than 7GB/s and latencies below 2 μs. The first version of KALYPSO are in operation at the EOSD experimental setups at ANKA and Eu-XFEL. The commissioning at other facilities (DELTA, TELBE, SOLEIL) is...
planned for late 2017.
In this contribution, we describe the KALYPSO system and its applications, together with the ongoing development activities, namely the integration of the custom sensor based on LGADs. An overview of the experimental results obtained with KALYPSO will be also shown.

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Presenter:  ROTA, Lorenzo (KIT)

Session Classification:  POSTER Session

Track Classification:  Systems, Planning, Installation, Commissioning and Running Experience
Development of a Front-End ASIC for 1D Detectors with 12 MHz Frame-Rate

Tuesday, 12 September 2017 17:45 (15 minutes)

We present a front-end readout ASIC developed for a new family of ultra-fast 1D detectors. The ASIC is designed in 110 nm CMOS technology and is compatible with different semiconductor sensors (Si or InGaAs) and geometries. The chip contains up to 128 channels, each consisting of a Charge-sensitive Amplifier, a fully-differential shaping stage and an high-speed output buffer. A frame-rate of 12 MHz at full occupancy has been obtained with the first prototype. We also discuss a novel circuital solution to implement tunable time-variant trapezoidal shaping based on a Fully-Differential Difference Amplifier, to improve noise performance at high frame-rates.

Summary

A fully custom ASIC has been developed for a new generation of 1D detectors to be used for beam diagnostics at accelerators. The main requirements are a frame-rate in the MHz range with full occupancy, high-linearity and low-noise performance. Moreover, since the chip will be integrated on a detector card together with high-speed digital and RF circuits, high rejection of common-mode and power-supply noise are mandatory. Finally, the chip must be able to process signals of both polarities with a variable detector capacitance (from 500 fF to 5 pF), in order to be compatible with different sensor technologies.

The chip is designed in 110 nm CMOS technology from UMC. The final version of the chip will consists of up to 128 channels with 50 μm pitch, to match the geometry of the sensors. Each channel is based on a synchronous readout and consists of a Charge-Sensitive Amplifier (CSA), a noise-shaping stage and a channel buffer. The CSA amplifier is implemented as a differential folded-cascode OTA.

The noise-shaping stage performs Correlated-Double-Sampling (CDS) in order to reduce low-frequency noise and the kT/C noise introduced by the synchronous reset mechanism. In order to achieve high frame-rates, a sample-and-hold channel buffer is needed to allow "integrate-while-read" operation. The output of each channel is connected through an analog multiplexer to a high-speed I/O buffer, which drives the external ADC with a settling time below 4 ns. To achieve high speed and low distortion with a 50 Ohm load, the output buffer has been designed with a two-stage class-AB OpAmp with cascode Miller compensation.

A first prototype based on a traditional CDS stage and with a limited number of channels has been submitted and characterized. With a power-supply voltage of 1.2 V and a power consumption of 1.7 mW/channel (including the 50 Ohm line-drivers), we have measured a gain of 37 mV/fC, a maximum frame-rate of 12 MHz and an ENC of 400 e- @ 1 pF at the maximum readout speed.

To improve the noise performance of the system, a novel time-variant noise-shaping stage has been designed. A novel circuital solution based on a Fully-Differential Difference Amplifier (FDDA) allows us to incorporate both noise-shaping and single-ended-to-differential conversion in a single stage, without loading the output of the CSA with a resistive load. With respect to the previous design based on a traditional CDS stage, simulations have shown a significant improvement in noise performance while maintaining the same power consumption. Moreover, the shaping time can be tuned according to the required frame-rate, therefore optimizing noise performance. An ENC of 140 e- @ 1 pF and a 10 MHz frame-rate has been estimated through Monte-Carlo simulations. The final version of the chip with the new noise-shaping stage will be submitted in summer 2017.
We will discuss the implementation and the characterization of the first prototype chip together with the improvements developed for the final version. In particular, we will describe the trapezoidal shaper based on FDDA and compare it with other solutions present in the literature.

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**Presenter:** ROTA, Lorenzo (KIT)

**Session Classification:** POSTER Session

**Track Classification:** ASIC
A 65 nm Macro-Pixel Readout ASIC (MPA) for the Pixel-Strip (PS) Module of the CMS Outer Tracker Detector Upgrade at HL-LHC

Tuesday, 12 September 2017 17:45 (15 minutes)

The MPA is the pixel readout ASIC for the hybrid Pixel-Strip module of the Phase-II CMS Outer Tracker upgrade at the High Luminosity LHC (HL-LHC). It employs a novel technique for identifying high transverse momentum particles and provides this information at a 40 MHz rate to the L1-trigger system. The chip also comprises a binary pipeline buffer for the L1-trigger latency, and a data path to support the readout of full events with a maximum trigger rate of 1 MHz and a latency of 12.8 µs. The design and implementation in a 65 nm CMOS technology of the first prototype ASIC that integrates all functionalities for system level operation are presented in this contribution.

Summary

The objective of the CMS Outer Tracker upgrade for the High Luminosity LHC (HL-LHC) is to adopt the use of double layer sensors to facilitate the quick, on-detector, identification of high-pT tracks (>2 GeV) and their transmission to the L1 trigger system at the 40 MHz bunch crossing rate. For the first time data coming from the Tracker will be used in the L1 trigger decision of a high luminosity hadron experiment. In parallel, a readout channel will transmit triggered events to the DAQ at a nominal average trigger rate of 750 kHz.

The Macro Pixel ASIC extracts hits (binary signals) from the pixelated sensor. It comprises a fast front-end with leakage current compensation and amplitude discriminator circuits with binary readout for a 120 x 16 pixel sensor array with dimensions of 23.16mm x 12.0 mm. Considering the 1920 channels per chip at a 40 MHz bunch-crossing rate, they represent roughly a data throughput of 80 Gbps per chip. Such an amount of data is processed and combined in real time with the input data (2.56 Gbps) coming from strip sensor layer in order to identify particles with high transverse momentum. A novel particle recognition algorithm, provides an almost lossless data transmission to the back-end at a bandwidth of 1.6 Gbps. This compression combines zero-suppression techniques with the capability of recognizing particles with high transverse momentum. In parallel, every event is stored for a maximum latency of 12.8 us and it can be required with a trigger signal. The chip supports a maximum trigger rate of 1 MHz and provides the encoded position and dimension of the pixel and strip clusters.

The ASIC is designed in an 8-metal 65 nm CMOS technology. It exploits a Multi-Supply Voltage (MSV) to strongly reduce the digital power consumption without degrading the Analog Front-End and Data transmission performance. Therefore, the digital core is powered at 1 V while the Analog Front-End and the custom-sLVS drivers and receivers are powered at 1.2 V. The sLVS differential interface utilizes a programmable current to optimize the power consumption while maintaining good signal integrity. The digital core is implemented using standard cell libraries of different threshold voltage devices (Multi-Vt design) to locally improve performance or reduce power consumption. For the distribution of the 40 MHz sampling clock, the chip features a clock distribution scheme based on a clock trunk for the distribution to the pixel rows which allows to achieve a very low clock skew (~1 ns), while it exploits a clock re-buffering at each pixel row for the system clock to increase the skew and reduce IR drops at the clock transition. The chip clock manager is capable of de-skewing the 40 MHz sampling clock to compensate for the particle time-of-flight. Full chip simulation and power verification show the achievement of the expected performance with a total power density lower than 100 mW/cm².
We will present the design architecture and the development work of the first prototype MPA ASIC integrating all required functionalities for system level operation. The design will be submitted for prototyping in a common full mask set 65nm engineering run with the SSA ASIC.

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**Presenter:** CERESA, Davide (CERN)

**Session Classification:** POSTER Session

**Track Classification:** ASIC
Short-Strip ASIC (SSA): A 65nm Silicon-Strip Readout ASIC for the Pixel-Strip (PS) Module of the CMS Outer Tracker Detector Upgrade at HL-LHC

Tuesday, 12 September 2017 17:45 (15 minutes)

The SSA is a silicon-strip readout ASIC for the hybrid Pixel-Strip detector of the CMS Outer Tracker High Luminosity LHC (HL-LHC) Phase II upgrade. It is a 120-channel ASIC with double-threshold binary readout architecture, utilizing a quick hit cluster finding logic to provide encoded hit information for particle momentum discrimination to the Macro Pixel ASIC (MPA) at the bunch crossing rate of 40MHz, while allowing the full sensor readout at a nominal average trigger rate of 750KHz. The design and the implementation in a 65nm CMOS technology of the first prototype ASIC that integrates all functionalities for system level operation will be presented in this paper.

Summary

The Compact Muon Solenoid experiment at CERN is foreseen to receive a substantial upgrade of the outer tracker detector and its front-end readout electronics, requiring higher granularity and readout bandwidth to handle the large number of pileup events in the High-Luminosity LHC. For this reason, the entire tracking system will be replaced with new detectors featuring higher radiation tolerance and ability to handle higher data rates and readout bandwidths. The possibility of identify particles with high transverse momentum to provide primitives for the L1 trigger decision, requires the adoption of double layer sensor modules and the development of two different front-end ASICs: the Short Strip ASIC (SSA) and the Macro-Pixel ASIC (MPA) allowing to reduce the total output data flow from 1.3Tbps to 30Gbps per module while limiting the total power density below 100mW/cm².

The SSA is the front-end ASIC responsible of reading-out the Short-Strip silicon sensor and to provide encoded information for the particle momentum discrimination. It is implemented in a 65nm CMOS technology utilizing 8 metal layers and is bump bonded to a flex hybrid. A total of 85000 SSA ASICs will be used in the CMS outer-tracker.

The analog front-end channel is composed by a regulated cascode pre-amp coupled to a booster amplifier followed by a double threshold folded cascode discriminator circuit capable to distinguish between hits with an energy over the minimum ionizing particle energy and high ionizing particles (HIPs). A single ended architecture of the input stage is optimal from the point of view of demanding requirements for the noise performance (ENC<1,000e-) and power consumption (<220μA per channel).

A digital back-end circuit processes the discriminated hits and generates the trigger data and the L1-accept readout data streams. The discriminator pulses are sampled at the bunch crossing rate and follow two distinct data paths: the trigger data path and the L1 data path. The first consists of a strip clustering logic that calculates the centroid position of the hit clusters, encode the information and apply a parallax correction. The encoded hits are transmitted with a bandwidth of 2.88 Gbps to the MPA ASIC for correlation with pixel sensor hits. In the L1 data path, the full sensor hit array is stored in a rad-hard static RAM waiting for the arrival of a Level-1 trigger. Up to 24 High Ionizing Particles hits (HIPs) flags are transmitted along the full short-strip sensor image.

For the design implementation, a fully scripted Digital-On-Top flip-chip methodology is used. Special attention was given in the use of radiation tolerant techniques in order to mitigate the effects of Single Event Upsets in the digital control circuitry, while maintaining low power consumption.
Radiation hardening techniques have also been adopted in the analog front-end circuits to guarantee operation up to a target Total Ionizing Dose of 100Mrad.

We will present the design architecture and the development work of the first prototype SSA ASIC integrating all required functionalities for system level operation. The design will be submitted for prototyping in a common full mask set 65nm engineering run along with the MPA ASIC.

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**Session Classification:** POSTER Session

**Track Classification:** ASIC
A Real-Time Demonstrator for Track Reconstruction in the CMS L1 Track-Trigger System Based on Custom Associative Memories and High-Performance FPGAs

Thursday, 14 September 2017 15:15 (25 minutes)

A Real-Time demonstrator based on the ATCA Pulsar-IIB custom board and on the Pattern Recognition Mezzanine (PRM) board has been developed as a flexible platform to test and characterize low-latency algorithms for track reconstruction and L1 Trigger generation in future High Energy Physics experiments. The demonstrator has been extensively used to test and characterize the Track-Trigger algorithms and architecture based on the use of the Associative Memory ASICs and of the PRM cards. The flexibility of the demonstrator makes it suitable to explore other solutions fully based on high-performance FPGA devices.

Summary

The increase of the luminosity to $5 \times 10^{34} \text{cm}^{-2} \text{s}^{-1}$ expected in the Large Hadron Collider after the upgrade scheduled for 2025 will bring the number of minimum bias interactions per bunch crossing to about 140. This would generate an unmanageable increase in the trigger rate. To keep the trigger rate below 1MHz, a value compatible with bandwidths in data transfers and processing power of trigger systems, we proposed the introduction of data reduction based on low-latency (<5us) track reconstruction from high-resolution Silicon Tracker information. Only data associated to high-Pt tracks (e.g.: tracks with energy >3GeV => 3% of the tracks) would be propagated to the L1 Trigger system.

Several groups studied different algorithms for track reconstruction through high-level simulations during the last years. Hardware implementations have been validated using real-time demonstrators based on “off-the-shelf” and custom components. We focused on algorithms that take advantage of a preliminary data reduction obtained filtering out “hits” that do not belong to “interesting” tracks that are associated to patterns stored in high-density Associative Memory (AM) custom devices. Algorithms are implemented in a high performance FPGA. They perform a further data reduction in the Track Candidate Builder (TCB) and they extract the Track parameters in the Track Fitter (TF).

We developed a proof-of-concept real-time demonstrator based on the Pattern Recognition Mezzanine (PRM) board, a custom board housing a set of AM ASICs (12 x AM06 in the version that produced the results that will be presented) and on a Xilinx Kintex UltraScale FPGA device where the TCB and TF are implemented. As host board we used the Pulsar-IIB board, a custom board developed at FNAL compatible with a full mesh high speed ATCA backplane. This board provides an ideal powerful building block for the development of scalable architectures requiring flexible high bandwidth board-to-board communications. Each board is equipped with two high-performance Xilinx Virtex-7 FPGA devices and four FMC connectors that allow the integration with custom or “off-the-shelf” mezzanine boards as the PRM board. The host PC uses a Gbit Ethernet link to control and monitor the demonstrator. IPBus protocol is used to access control and status registers and FIFOs. Input FIFOs are used to store patterns that will be pre-loaded into AM ASICs via JTAG and hits that will be transmitted to the PRM FPGA via high-speed (up to 10 Gbps/link) serial links (3 links/connector) to emulate Tracker data. Output FIFOs collect track parameters from the PRMs.
The final goal was to evaluate the system performance (e.g.: latency and efficiency in data filtering), to identify any necessary modifications to match bandwidth and latency constraints and to validate the component selection. System architecture, test results and figures of merit obtained with sets of data associated to physically relevant events will be presented. The entire SW/FW platform of our demonstrator is available to hardware and firmware developers interested in having a flexible and ready-to-use environment for the validation of other algorithms or hardware solutions.

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**Session Classification:** Trigger

**Track Classification:** Trigger
Radiation tolerant serial links for high-speed data transfer in High Energy Physics experiments

Tuesday, 12 September 2017 17:45 (15 minutes)

Radiation tolerant serial links for high-speed data transmission in High Energy Physics experiments have been developed at INFN-Pisa and UCSB in a commercial 65nm CMOS technology: 2Gbps Standard-Cell based Serializer and Deserializer and custom 3GHz SLVS Driver and Receiver. Results of test and characterization of the last version of the circuit prototypes produced in the second half of 2016 and tested and characterized, including TID and SEE tests, in the first half of 2017 will be presented. The Serializer and the SLVS Drivers and Receivers have been successfully used in the CHIPIX65-FE ASIC, a demonstrator of a Front-End ASIC for pixel detectors developed at INFN.

Summary

The increase of the luminosity (up to $5 \times 10^{34}$ cm$^{-2}$ s$^{-1}$) after the High Luminosity (HL) upgrade of the Large Hadron Collider (LHC) will require the complete re-design of the Front-End (FE) electronics of the inner Silicon Trackers of the LHC experiments because of the new harsh requirements with respect to data rates - up to 5Gbps from each FE ASIC - and radiation tolerance, Total Ionizing Dose (TID) - up to 1Grad - and Single Event Effects (SEE). Since 2014 within the framework of the RD53 collaboration ATLAS and CMS physicists and engineers have been working on the definition of a possible common architecture for the FE ASICs for the future pixel detectors and on the development of serial links that could be used in ASIC development. INFN-Pisa had been already working in collaboration with UCSB in the years 2012-2014 on the design in a commercial CMOS 130nm technology of radiation-tolerant blocks for the implementation of high-speed links. Since 2014 INFN-Pisa joined the RD53 and the INFN CHIPIX65 3-years project whose target was the development of a demonstrator FE ASIC in a CMOS 65nm technology for the readout of future pixel detectors.

We used Standard Cells to implement 20-bit Serializer (SER) and Deserializer (DES) devices, with Triple Modular Redundancy (TMR) to provide protection against SEEs. The Standard Cell approach is still compatible with the required data rates (2Gbps), while a custom design would be required for higher data rates. SER/DES devices provide Data-Strobe (SER) and Data-Valid (DES) output signals that can be used as read and write clocks for buffer FIFOs containing SER input data and DES output data. SER/DES devices have an area of 100um x 56um and 180um x 56um respectively and they dissipate 2.35mW and 17.85mW in typical conditions ($T = 25C$, $VDD = 1.2V$).

In the SLVS TX/RX devices the use of thin oxide transistors provides robustness against TID effects while the redundancy of analog building blocks protects against SEEs. In the TX twelve drivers in parallel guarantee SLVS specifications also in case of a radiation-induced error in one of the units. Rising and falling edges of the input signal are detected and used to implement pre-emphasis when this capability is enabled. The RX has a very simple structure based on three two-stage amplifiers in parallel followed by a voting logic. TX/RX dimensions are 130um x 36um and 30um x 16um respectively and absorbed currents are 5.4 mA and 1.3mA in typical conditions.

Final versions of SER/DES and SLVS TX/RX devices have been produced in the second half of 2016. Results of test and final characterization of prototypes, including results of irradiation tests (effects of TID up to 500 MRad and SEE cross-sections evaluated with irradiation with heavy ions) will be presented.
presented. SER and SLVS TX/RX devices have been successfully used as building blocks of the CHIPIX65-FE0 demonstrator ASIC. All the developed circuits are available as components of fully characterized library to ASIC designers.

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**Session Classification:** POSTER Session

**Track Classification:** ASIC
Gallium Nitride DC-to-DC Converter

High efficiency, radiation hard, hybrid GaN and CMOS integrated module DC-to-DC converter has been designed. The integrated, compact, low-mass, single-module DC-DC converter solution has an input voltage of 18V regulated down to an output voltage of 1.4V, with 5A maximum load current. It exhibits >80% efficiency. Discrete GaN transistors are used for the power stage, and the controller circuitry and power device drivers are integrated on a 0.35um CMOS chip. Radiation hardening by design (RHBD) techniques have been implemented and the goal is that the converter functions at total ionizing dose (TID) levels ≥150 megarad(Si).

Summary

Large high energy physics experiments are currently driving the development of new and more efficient powering schemes to cope with the increase of power demanded by the upgraded high-density front-end electronics boards. Due to the radiation levels up to hundreds of Mrad(Si) at the detector cores, commercial DC-DC converters cannot be used in these powering schemes. Therefore, a critical need exists for custom-designed radiation-hard DC-DC converters. Another requirement for these converters is the ability to function in high magnetic fields. Gallium Nitride (GaN) material, providing inherent radiation hardness, high switching frequency and large voltage swing is a viable contender for implementing these converter circuits. In the converter that will be presented, discrete GaN transistors are used for the power stage, and the controller circuitry and power device drivers are integrated on a 0.35um CMOS chip. Radiation hardening by design (RHBD) techniques have been implemented and the goal is that the converter functions at total ionizing dose (TID) levels ≥150 megarad(Si) and neutron fluence levels ≥2.0E15 n/cm², and is immune to Single Event Latchup (SEL). The converter will also be designed to cope with high magnetic field constraints, with low electromagnetic interference (EMI) for operation in the proximity of the noise-sensitive front-end electronic boards.

The hybrid GaN and CMOS integrated module DC-DC converter has the following specifications:

- Input voltage of 18V regulated down to an output voltage of 1.4V, with 5A maximum load current. The 18V input voltage is one of the main benefits of the proposed work (allows higher voltage delivered to the core which significantly helps with the power dissipation and cooling requirements).
- Exhibits >80% efficiency
- Integrated, compact, low-mass, single-module DC-DC converter solution. The components will be integrated to provide a single-package solution to meet the sizing requirements of most of the detectors in large particle physics experiments.

The feasibility of the design has been verified by designing and simulating the whole system, including the CMOS controller/drivers with GaN power stage, and also designing, fabricating and testing the first prototype board-level system of the DC-DC converter. This prototype system includes a candidate GaN power stage and many other components that will be parts of the final, radiation-hard system. A component off the shelf (COTS) driver chip was selected to drive the GaN stage in the prototype hardware system. The COTS driver is not tolerant enough for the extreme levels of radiation present at the detector cores, but allowed to collect important information on the DC-DC converter performance. The test results showing 18V input voltage, 1.4V output voltage, 5A output current and 82% efficiency will be discussed in the conference presenta-
tion. Meanwhile, a 0.35um CMOS chip that contains the controller and drivers, as well as radiation effect tests structures has been fabricated in April 2017. Schedule permitting, test results of this chip will also be discussed in the conference.

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Session Classification: POSTER Session

Track Classification: Power, Grounding and Shielding
Laboratory and Beam Test Results of TOFFEE ASIC and Ultra Fast Silicon Detectors

Wednesday, 13 September 2017 11:05 (25 minutes)

We report on the measurements performed on the full custom ASIC TOFFEE designed to read out Ultra Fast Silicon Detectors (UFSD). The ASIC has been tested in laboratory with custom test boards and an infrared laser hitting the sensor and emulating a minimum ionizing particle signal. Laser measurements showed that a time resolution of less than 50 ps is achievable with a 10 fC signal.

We will also present the beam test results for the TOFFEE and UFSD system which will be held in May at CERN.

Summary

In the High Luminosity LHC environment, the overlap of hundreds of events raises the need to distinguish events separated by a few tens of picoseconds.

In order to reach a precise time information it is required to have concurrently large and uniform signals from the detector and a fast readout electronics, as well as to minimize the noise.

To fulfill this requirement, the Ultra Fast Silicon Detectors (UFSD) are being developed and have an intrinsic resolution of about 20 ps, obtained at a beam test with pions in 2016. These sensors feature internal charge multiplication, electrode segmentation and provide a signal between 8 and 10 fC for a minimum ionizing particle. The moderate charge multiplication allows to have a fast and steep signal while keeping the avalanche noise low.

The TOFFEE ASIC, a 8-channel amplifier comparator chip, has been specifically designed in UMC 110 nm CMOS technology to read out the UFSD: the input stage has been optimized for the shape and charge of the sensor signal.

The ASIC has been developed in UMC 110 nm CMOS technology and is aimed to fulfill the CMS-TOTEM Precision Proton Spectrometer (CT-PPS) time resolution requirements (~ 30 ps per detector plane). It features LVDS outputs and the signal dynamic range matches the requirements of the High Precision TDC (HPTDC) system.

The chip has been received from foundry in September 2016 and tests started in October with custom boards.

Since February 2017, it has been possible to test the performances of TOFFEE coupled with UFSD sensors. The test board houses a 32-channel UFSD sensor wire-bonded to the ASIC and allows to read out 8 channels at the same time.

The laboratory setup involves the use of an infrared laser to emulate the charge deposition of a minimum ionizing particle in the sensor. The charge produced by the laser has been calibrated by means of a pin diode without charge multiplication.

A time resolution of less than 50 ps has been achieved with a 10 fC signal, dropping under 40 ps for higher charge values. This values include the jitter contribution of the laser and show good agreement with simulations.

A beam test is scheduled for May 2017 at CERN (SPS H8 beam line). In this beam test the data acquisition chain will be very close to the one foreseen at CT-PPS: an array of three TOFFEE + UFSD boards will be proofed with 180 GeV pions, while the output will be read out with the HPTDC.
This test campaign will be an important prediction of the actual performance of the system before its installation in the experiment, foreseen for the last quarter of 2017.

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**Session Classification:** ASIC

**Track Classification:** ASIC
An FPGA-Based Sampling-ADC for the Crystal Barrel Calorimeter

Tuesday, 12 September 2017 17:15 (15 minutes)

The digitization stage of the main electromagnetic calorimeter of the CBELSA/TAPS experiment in Bonn (Germany) is being equipped with custom 80 MSPS, 14 bit Sampling-ADCs. Onboard data processing with FPGAs allows determination of the signal characteristics, reducing the data substantially. The readout of the unprocessed sampling data allows offline analysis and refinement of the FPGA-algorithms.

A partial setup has shown promising results during a photoproduction-beamtime. It has been demonstrated that the SADCs are able to overcome the readout-rate limitation of the current QDC readout.

The full setup is planned to be commissioned within the next year.

Summary

The main electromagnetic calorimeter of the CBELSA/TAPS experiment has been equipped with a new Avalanche-Photodiode readout to obtain full trigger capability. Within the scope of this modification, the digitization stage of the energy branch is upgraded from Fastbus QDCs to custom Sampling-ADCs to gain a higher readout-rate.

The design has been adapted from the PANDA-SADC that is being developed by P. Marciniewski. A low noise switching power supply, as well as an analog input stage with multi-feedback filters, digitally controllable pole-zero compensation and baseline-shifting have been developed. Furthermore, a custom backplane was added for distribution of trigger, clock (phase) and slowcontrol.

The SADC features 64 channels with 14 bit and 80 MSPS in a NIM 1/12 cassette, with a power consumption of 22 watts. Two Kintex 7 FPGAs process the digitized signals onboard. Data is transferred with two 1Gbit/s UDP/IP copper links to COTS switches with 10Gbit/s uplinks. Event-buffering and -building is done in conjunction with a linux server system.

For the full readout of the calorimeter, two NIM crates will be equipped with SADCs, yielding 1536 channels; enough for the maximum of 1380 signals from the calorimeter as well as 60 fast energy sum signals. The full dynamic range of each channel is 2.5 GeV.

As the bandwidth of the processed CsI(Tl) scintillator crystal signals barely extends above 1MHz, the sampling rate is decimated by a factor of four, yielding a vertical resolution of 16 bit. The waveform data is reduced by means of further FPGA processing upon external or self trigger. Methods used for determination of timing and energy include digital constant fraction discrimination, integration and peak detection. Algorithms for pile-up determination ensure the recovery of previously discarded energy signatures. For the case of detected pile-up, and as a means of debugging, the readout of full samples is possible. Offline-analysis of the full samples has proven helpful for the refinement of the FPGA algorithms.

A preliminary setup, reduced to one quarter of the full calorimeter, has been operated during two early commissioning meson-photoproduction-beamtimes at the ELSA (Electron Stretcher Accelerator) facility in April and June 2017. The quality of the data has proven to be at least competitive to the existing QDC readout. Kinematic analysis have shown the expected signatures of π0- and η-mesons. The possibility of the oscilloscope-like access to all signals has been valuable for detector diagnosis during the beamtimes.
The readout-rate is limited mainly by the UDP/IP implementation and the necessary custom software-handshake to ensure data integrity. Yet, above 10 kHz readout rate have been obtained already, with room for further optimizations; whereas the current readout is limited to 1 kHz.

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**Session Classification:** POSTER Session

**Track Classification:** Other
General-Purpose Solution for Timepix3 – Katherine Readout

The contribution shows possibilities of the readout for Timepix3 (Ethernet Embedded Readout Interface for Timepix3 – called Katherine) for a wide range of applications. The architecture and features of the system are described in detail. The stress is laid on the usage of more readouts in a telescope configuration, where more Timepix3 sensors are operated and their time-dependent functions are synchronized. The fully radiation hardened solution for Timepix3 is also presented. Authors demonstrate and discuss the utilization of the device in ATLAS experiment.

Summary

The Katherine readout device is new embedded readout device using Gigabit Ethernet interface for Timepix3 pixel detectors (the latest generation of Medipix family). The device can manage one Timepix3 sensor and process all functions of the sensor as a high hit-rate, a time resolution (1.56 ns), event data-driven mode etc. Used interface – Gigabit Ethernet – makes it possible to communicate (up to about 15 Mhit/s) with back-end DAQ systems for long distance. That is an important benefit in comparison with USB-based readout devices used very frequently in Medipix/Timepix detectors domain. In the contribution, the main features of device are mentioned in detail – such as the implemented bias high voltage source (range ±300 V), automatic data sending via SSH, automatic compensation of ToA values (columns with shifted clock) etc. The readout device is equipped with a dual-core ARM A9 processor with the high computational power which is, in conjunction with the FPGA device, good platform for wide range of tasks where the need for extended features of the readout, according to requirements, is important.

The contribution summarizes also measurements accomplished with Katherine readout in the past. The results of equalization, energetic (ToT) calibration and time-walk corrections performed by the readout are mentioned. The significant emphasis will be placed on the usage of more readout devices in telescope configuration. For this purpose, the authors also use Time-to-Digital Convertor (TDC) device with time resolution of 13 ps for very accurate measurements of clock phase differences in sensors. The individual sensors with the readout can be far each other several meters. The concept of this measurement chain was tested at the SPS facilities at CERN in a 120 GeV/c pion beam and synchronization accuracy of ~0.8 ns was achieved.

The most important feature of the Katherine readout is its optimization for a long cabling. It is absolutely profitable when a user needs a long distance between sensor and readout electronics – typically for measurements in higher radiation field. The special extending option modules and chipboard for Timepix3 were designed for this purpose. Using that the fully radiation hardened measurement setup/chain can be built. The system setup was tested with 20 m long cabling with no communication speed reduction (640 Mbs speed used), and 100 m long cabling with reduction to 80 Mbs (per output data line). The contribution also presents the first real application using this solution – the system has been already installed in ATLAS cavern. The sensor’s position is 80 m away from the readout device placed in USA15 rack room. The maximal hit rate is 5 Mhit/s; however authors plan to make minor upgrade of the system and get approximately 10 Mhit/s. Clock data recovery technique is used for all Timepix3 output data, this avoid the worries about length matching of data cables. Data taken and obtained knowledge (e.g. dependence of cables quality)
will be the subject of the discussion as well. Another important point of the system is the price. The whole system can be considered as low-cost system.

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**Session Classification:** POSTER Session

**Track Classification:** Radiation Tolerant Components and Systems
FED Firmware Interface Testing with Pixel Phase 1 Emulator

Wednesday, 13 September 2017 16:30 (15 minutes)

A hardware emulation of the CMS pixel detector phase 1 upgrade front-end electronics was developed to test and validate the architecture of front-end driver (FED) firmware. The emulation, implemented on the CERN GLIB uTCA platform, drives optical transmitters to the back-end electronics. The firmware emulates the complex functions of the readout chips and Token Bit Managers and allows for possible exceptions in the output data. The emulation implements fixed data patterns and realistic simulated data to drive readouts at expected data and trigger rates. Testing software was developed to control and verify correct transmission of data and exception handling in the FED.

Summary

The pixel phase 1 upgrade has been installed in the CMS detector. The pixel detector modules are made up of two layers, a thin silicon layer and a readout chip that is bump bonded to the silicon pixels. The silicon pixel system is a reverse p-n junction that allows charged particles to create electron-hole pairs to measure the charge. This new detector includes an added detector layer for both the barrel and forward pixels. Along with a high efficiency readout chip (PSI46digv2 and PROC600) and increased precision for tracking and vertexing. The increased luminosity of the LHC in Run 2 will lead to a large expected data rate and therefore a high bandwidth front-end driver (FED) to manage the data. A CERN gigabit link interface board (GLIB) with Virtex 6 FPGA customized firmware and software is used to probe the features of new FED firmware releases. By exploiting an 8-way SFP FPGA Mezzanine Card a single GLIB can emulate 16 independent channels of the phase 1 pixel detector. Output from the pixel detector is converted from two 160 Mbps signals to one 400 Mbps optical output using bitwise interleaving and non-return-to-zero inverted (NRZI) encoding. The GLIB is used to emulate all layers of the pixel detector in multiple configurations to stress the FED. Many possible exceptions can be generated and read out such as, bit flips, missing event headers/trailers, and delayed events. Possible scenarios are out-of-sync due to event number error or timeout and missing events due to missing the event header. Utilizing these functions, it is possible to generate unlikely events or recreate conditions that are seen in the detector to probe the processes in the FED readout. Data can be sent in fixed event sizes or from simulated events that are locally stored on the GLIB. Using a FEROL 10 G link, realistic simulations of pileup of 70 and 130 can be read out at 2.4 Gbps at 100 kHz and 3.9 Gbps at 86 kHz, respectively. Larger data rates are possible, but the trigger rate is throttled by the AMC13. An installation has been integrated into the pixel DAQ test system at CMS for fast verification of FED firmware upgrades.

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Session Classification: POSTER Session
**Track Classification:** Programmable Logic, Design Tools and Methods
Metallic magnetic calorimeters (MMC) are new cryogenic detectors that offer a high resolution of single eV, a signal rise time of below 100 ns, a dynamic spectrum of several 10 keV and an almost optimal linearity. MMCS are of high interest for many experiments, such as dark matter detection or neutrino mass specification. Since pixel arrays of the sensor are read out at GHz-Frequency and each single pixel offers a fast rise time, a complex analog and digital readout system is required. This contribution will give an introduction to MMC technology in combination with the implemented readout electronics.

Summary

Detection of single particles with energies of a few eV up to several MeV plays a prominent role in many areas of physics. Conventional detectors such as semiconductor detectors or crystal spectrometers either offer a high dynamic range with limited resolution or vice-versa. In contrast, cryogenic detectors such as metallic magnetic calorimeters (MMCs) combine high spectral and temporal resolution while covering a broad energy range at the same time. Modern magnetic calorimeters as used for soft X-ray spectroscopy offer an energy resolution of 1.6 eV at 6 keV particle energy, a signal rise time below 100 ns, an energy bandwidth of several 10 keV and an almost ideal linear detector response. For the readout of MMCS, superconducting quantum interference devices (SQUIDs) are used since they provide a high system bandwidth and low noise. The latter two properties are mandatory for detectors with a high temporal and spectral resolution.

In addition to these, many experiments require spatial resolution to determine the location of an event or to collect a lot of events for high statistics. Both requirements can be fulfilled by using multi-channel detector systems, which contain a lot of independent pixels. But at the same time, the readout of such multi-channel detector systems turns out to be challenging. Microwave SQUID multiplexing as previously introduced by Irwin et al. for reading out arrays of superconducting transition edge sensors turns out to be a very promising approach. Here, non-hysteretic rf-SQUIDs are used to modulate the pixels' information on different carrier frequencies in the GHz range. The first part of our contribution will briefly introduce the applied MMC technology along with the highly innovative multiplexing technology.

In addition, the requirement of processing of the readout electronics imposed by MMC arrays is more demanding as compared to reading out transition edge sensor arrays due to the fast signal rise time of MMCS. For this reason, a customized readout system for microwave SQUID multiplexed MMC arrays will be presented as major in this contribution. The readout system is based on software defined radio. All digital processing is implemented on an FPGA. Fast Digital-to-Analog-Converters (DAC) and Analog-to-Digital-Converters (ADC) are used for creating and digitizing the MHz frequency comb which is sent to the multiplexer and modulated according to the actual state of the detectors. A customized high-frequency front-end electronics performs the up- and down-mixing of the frequency comb to the targeted frequency range of 4-8 GHz. Each of the three parts has been developed, implemented, integrated and evaluated. The first version of the system was successfully used to interface a 64 pixel MMC detector array. This solution allowed for the very first true multiplexed readout of a metallic magnetic calorimeters, i.e. to record events on various independent channels in parallel, by just using one pair of coaxial cables into the cryostat. Moreover, we will show, how this system architecture can be extended to the readout of thousands
of channels in parallel. Eventually, we target the simultaneous readout of up to 100 k channels with this approach.

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**Session Classification:**  Systems, Planning, Installation, Commissioning and Running Experience

**Track Classification:**  Systems, Planning, Installation, Commissioning and Running Experience
The ATLAS Fast Tracker System

Thursday, 14 September 2017 15:40 (25 minutes)

The Fast Tracker (FTK) system, one of the ATLAS trigger upgrades, is presently being commissioned. The information from the 100 million channels of the tracking detectors is presently exploited at the HLT only for a subset of the events or for limited detector regions due to timing limitations. The FTK system is designed to deliver full event track reconstruction for all tracks with pT above 1 GeV at a Level-1 rate of 100 kHz. This provides full track information with excellent quality at the HLT input. This high performance is obtained by using a combination of dedicated ASIC hardware based on associative memories and high performance Field Programmable Gate Arrays.

Summary

From 2010 to 2012 the Large Hadron Collider (LHC) operated at a centre-of-mass energy of 7 TeV and 8 TeV, colliding bunches of particles every 50 ns. During operation, the ATLAS trigger system has performed efficiently contributing to important results, including the discovery of the Higgs boson in 2012. The LHC restarted in 2015 and will operate for four years at a mass energy of 13 TeV and 14 TeV and bunch crossing of 50ns and 25ns. These running conditions result in the mean number of overlapping proton-proton interactions per bunch crossing increasing from 20 to 60. The FTK will allow the trigger to utilize tracking information from the entire detector at an earlier event selection stage than ever before, allowing for more efficient event rejection. This hardware system is designed to perform full scan track reconstruction of every event accepted by the ATLAS first level hardware trigger. To achieve this goal the system uses a parallel architecture, with algorithms designed to exploit the computing power of custom Associative Memory chips, and modern field programmable gate arrays. The processor will provide computing power to reconstruct tracks with transverse momentum greater than 1 GeV in the whole tracking volume. The tracks will be available at the beginning of the trigger selections, allowing for the development of more pileup resilient triggering strategies. The Fast Tracker system will be massive, with about 8000 Associative Memory chips and 2000 field programmable gate arrays, providing full tracking with a rate up to 100 KHz and an average latency below 100 microseconds. A partial FTK system has been built in 2016. Additional production is on going. It will be installed as it is delivered. The system is currently under commissioning. The final version of the electronic boards is presented, with details covering the hardware status and installation of the system. An overview of the commissioning status and first data-taking experience is presented.

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Session Classification: Trigger
Track Classification: Trigger
A Low-Noise CMOS Pixel Direct Charge Sensor, Topmetal-IIa, for Low Background and Low Rate-Density Experiments

Tuesday, 12 September 2017 17:45 (15 minutes)

We present the design and characterization of a CMOS pixel direct charge sensor, Topmetal-IIa, fabricated in a standard 0.35μm CMOS process. The sensor features a 45 × 216 pixel array with a 40μm pixel pitch which collects and measures external charge directly through exposed metal electrodes in the topmost metal layer. Each pixel contains a low-noise charge-sensitive preamplifier to establish the analog signal, which is accessible through a time-shared multiplexer. Initial tests show that the sensor achieved a <10e− analog noise per pixel. These characteristics enable its use as the charge readout device in future Time Projection Chambers without gas-avalanche gain, which has unique advantages in low background and low rate-density experiments.

Summary

We have successfully implemented a CMOS Integrated Circuit, Topmetal-IIa, that is uniquely suitable for charge collection and measurement in a Time Projection Chamber without gas-avalanche gain. It is a direct charge sensor with 40μm pitch between pixels fabricated in a standard 350nm CMOS technology without any post-processing. A metal node (Topmetal) is placed on the top of each pixel in a 45 × 216 pixel array for direct charge collection. Each pixel contains a low-noise charge-sensitive preamplifier (CSA) with a 1.3fF feedback capacitor to establish the analogue signal. The Topmetal electrode is directly connected to the input of the CSA. A ring electrode (Gring), which is in the same topmost metal layer as the Topmetal, surrounds the Topmetal while being isolated from it. In order to explore the charge collection behavior of different architectures between Gring and Topmetal as well as to realize the intended applications accordingly, we divided the Topmetal-IIa matrix in 3 sectors, each one implements a different Topmetal-Gring flavour. 3 different Topmetal-Gring architectures mean that only Topmetal is exposed, only Gring is exposed, and both Topmetal and Gring are exposed, respectively. A 2-bit in-pixel DAC is applied to the gate node of the feedback transistor of the CSA, in order to calibrate the total mismatch of the devices, hence improving the CSA’s peaking and decay time uniformity. What’s more, the CSA’s sensitive voltage biases that have significant contributions to the output noise are individually provided by the peripheral Low-Pass Filter (LPF) with tunable cut-off frequency, aiming to improve the noise performance. The analog signal from each pixel is read out through the traditional “rolling shutter” style time-shared multiplexer controlled by the array scan unit, and then is fed to two array-shared analog buffers, of which one is capable of 50 Ohm driving strength aiming to eliminate the external buffer hence reducing the entire readout system noise. For its intended application, event-rate density is expected to be low and charge (both free electron and ion) drifting speed is expected to be slow; therefore, we tuned the CSA to have long signal retention and eliminated the in-chip pulse shaper while focusing on improving the noise performance. Some simulation and preliminary test results confirm the low-noise design and correct readout implementation. The Equivalent Noise Charge of the sensor is <10e− rms at a 15μs peaking time and 150ms decay time with a detector capacitance of 11.5fF.

To improve beyond Topmetl-IIa, besides optimizing the LPF design, we can further increase the working margin of CSA’s sensitive voltage biases. We will investigate these options in future Top-
metal sensor development. We will present the overall design and some initial test results of the Topmetal-IIa chip in the conference.

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**Session Classification:** POSTER Session

**Track Classification:** ASIC
LAPA, a 5 Gb/s Modular LVDS Driver in 180 nm CMOS with Capacitively Coupled Pre-Emphasis

Tuesday, 12 September 2017 17:45 (15 minutes)

A pseudo-LVDS driver has been designed in a 180 nm technology for operation up to 5 Gb/s. It contains parallel main driver units based on an H-bridge circuit steering a current on an external load. The number of active units is selectable, to reduce switching capacitance and static current, and hence power consumption, if a smaller current swing can be tolerated.

Pre-emphasis is applied with a capacitively coupled charge-injection circuit. In nominal condition with a steering current of 4 mA over a 100 Ω termination resistor it consumes 30 mW from a 1.8 V supply.

Summary

The ATLAS experiment at CERN plans to upgrade its Inner Tracking system (ITk) for the High-Luminosity LHC in 2026. After the ALPIDE monolithic sensor was successfully implemented in the TowerJazz 180nm CMOS imager technology, and promising irradiation results were obtained modifying this process, an ATLAS-specific development in this modified process was started. As part of the development a 5 Gb/s LVDS driver has been designed. This driver is used both in a full pixel matrix prototype MALTA (Monolithic pixel sensor from ALICE to ATLAS), and in a specific test chip LAPA (pseudo-LVDS driver for the Atlas Pixel Apparatus). The MALTA chip contains 40 parallel drivers, and LAPA 16.

The LVDS driver contains a main driver and a pre-emphasis circuit.

The main driver is based on a H-bridge scheme that steers the current on the external output load. Each half branch of the H-Bridge has a three transistor circuit that act as a switchable current source.

The transistor defining the OFF current IoFF is in series with the transistor defining the ON current IoN. Another transistor, operated as a switch, is in parallel with the transistor defining the OFF current. When the switch is in the OFF state, the output current is limited to IoFF, and when it is ON, the output current is limited to IoN. This scheme avoids a current source in series with the H-bridge, resulting in a larger operating margin above saturation, allowing a reduction in transistor size (width) and hence dynamic power consumption.

The main driver consists of seven driving units operating in parallel. The number of active units can be varied to adapt the circuit switching capacitance to allow the required static current, hence optimizing the dynamic power consumption. The design is optimised to generate 400 mV over a 100 Ohm termination resistor using a 4 mA current. Under these conditions, the expected power dissipation to transmit a 2.5 GHz clock signal is approximatively 30 mW.

Speed performance can be improved applying pre-emphasis with a capacitively-coupled charge injection circuit.

LAPA integrates 16 independent capacitively-coupled charge injection circuits, of which an arbitrary number can enabled to vary the pre-emphasis according to the need. Each circuit consist of a CMOS buffering stage that drives a coupling capacitance of 25 fF. The layout is carefully optimized to reduce the parasitic capacitance of the buffering driving node and the overall pad capacitance. The pre-emphasis strength is so tunable in order to optimize the performance in terms of speed and dynamic power consumption, depending on the external load of the driver.
A common mode feedback circuit holds the common mode to about 800 mV, but this circuit can be disabled if the common mode voltage is set externally.

Main driver current biases can be adjusted using four bits on-chip digital-to-analog converters, with a total maximum output current of 6.4mA.

LAPA is embedded in MALTA chip. A separate test chip implements 16 LAPA drivers, with CMOS and LVDS input-output pads, for a detailed characterization.

Results and measurements will be presented.

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**Presenter:** CARDELLA, Roberto (CERN)

**Session Classification:** POSTER Session

**Track Classification:** ASIC
A Monolithic HV/HR-MAPS Detector with a Small Pixel Size of 50 µm x 50 µm for the ATLAS Inner Tracker Upgrade

This paper presents a HV/HR-MAPS detector designed in the framework of the HVCMOS collaboration for the ATLAS Inner Tracker update in the HL-LHC era. It was fabricated with a 150 nm HVCMOS process which includes a layer to isolate the bulk of PMOS transistors from the collecting node of the sensor. All front-end electronics are integrated inside the pixel, which is of only 50 µm x 50 µm, and include a preamplifier, a shaper, a discriminator and a digital block with FEI3 column drain architecture. Experimental results will be presented.

Summary

Monolithic pixel detectors, built by means of a deep-n-well over a high resistivity p substrate and reverse biased at a high voltage, present a large depletion region. This yields to fast charge collection and moderate levels of radiation hardness, around 1e-15neq/cm². Such performances and a moderate fabrication cost has turned the interest of several groups on developing some demonstrators for the 5th layer of the upgrade of the Inner Tracker detector of ATLAS for the HL-LHC era.

In this contribution will be presented a small demonstrator of 5.0 mm x 2.5 mm fabricated with a 150 nm process from LFoundry. The pixel matrix occupies 3.9 mm x 2 mm of the total area and it is composed of 40 rows and 78 columns with a pixel size of only 50 µm x 50 µm. In such a small area the analog and digital front-end electronics have been integrated. The inclusion of a CMOS discriminator and digital gates in pixel was possible by using an isolation layer that avoids punch through between the n-wells and the deep n-well (collecting node of the sensor).

The matrix has four different pixel flavours distributed in 2 submatrices of 40 rows and 20 columns and another two of 40 rows and 19 columns. The differences between the flavours are on the analog front end electronics. These are composed of preamplifier, shaper, and CMOS discriminator. The feedback capacitor was implemented in two different ways. In the first one no isolation layer was placed under the preamplifier so the bulk of the PMOS transistors is shorted to the collecting node (deep n-well). The drain-bulk capacitance of the PMOS output transistor is used as the feedback capacitor. In the second one the isolation layer was placed under the preamplifier and a MIM feedback capacitor was used. Two variants were implemented for these two pixels flavours, one with linear transistors and the other with circular transistors.

The function of the digital front-end electronics is to capture the time stamp for the leading edge and trailing edge transitions of the discriminator when a hit is detected. This information is stored in a 16-b DRAM memory. The layout was made full custom in order to integrate all the electronics in the given area. Each hit pixel contains 22 bits of information to be read out: 16 bits for the time stamp information and 6 bits for the address. This information is sent from the pixel that has detected a hit through a 22-b bus to an End Of Column (EOC) cell where it is stored temporarily. The EOC cells form a shift register which is read continuously by a control unit at 40 MHz. This passes the data to 2 serializers which transmit the information at 640 MHz through LVDS ports. The readout is asynchronous and with no trigger.
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Presenter: CASANOVA MOHR, Raimon (Universitat Autònoma de Barcelona (ES))

Session Classification: POSTER Session

Track Classification: ASIC
A Full Custom ASIC for Large Area 4-Dimensional Tracking

Tuesday, 12 September 2017 17:35 (15 minutes)

Large area silicon trackers with excellent time and position resolution are now considered in the upgrade programs of the ATLAS and CMS detectors.

In this contribution we present the development of a custom ASIC chip meant to be bump-bonded to segmented Ultra-Fast Silicon Detector, aiming to achieve a combined time resolution of $\sigma \sim 30$ ps.

The ASIC is implemented in standard CMOS 110 nm technology.

Summary

The design of large area 4-dimensional silicon tracking detectors with excellent time and position resolutions requires the development of specialized silicon sensors and appropriate electronics.

The silicon sensor that we deemed appropriate for this project are the so called Ultra-Fast Silicon detectors (UFSD). UFSD are a novel type of silicon detectors based on the Low-gain avalanche diode design: the controlled internal gain combined with an appropriate sensor geometry allow having large and short current signals, ideal for timing measurements. Beam test results have demonstrated the capability of UFSD to achieve a time resolution of ~ 30 ps.

In this contribution we present the first development of a custom built ASIC specifically designed to read-out large area Ultra-Fast Silicon detectors (UFSD) with a time resolution of ~ 30 ps.

The readout ASIC is implemented in a standard CMOS 110nm technology and organized as a 4x24 pixel matrix, flip-chip assembled to the tentative 1x3 mm$^2$ sensor pads. The on-pixel circuitry includes amplification, timing discriminator and a low power TDC with sub-50 ps binning. The timing discriminator incorporates both constant fraction (CFD) and leading-edge modality. Charge measurement is also provided to allow for off-line calibration of systematic amplitude-related effects. The baseline option for the TDC is to re-use an already existing IP employing time-interleaved analogue interpolators. A topology built with ring oscillators will also be considered.

The pixel logic, working with a clock frequency of 320 MHz or above, manages data building, local configuration, and the operation of the TDCs. This architecture is expected to keep the per-pixel power budget below 5 mW, yielding the necessary 30 ps r.m.s. time resolution. Data, clock, configuration and control signals are propagated asynchronously from pixel to pixel.

The end-of-column logic reads and stores event data from each 24-pixel column, manages the global configuration (periphery bias and chip operation), and serialises the data stream which is then output through 4 640 Mb/s LVDS links.

Preliminary simulation studies based on silicon-proven IP architectures were started, intended to define the rate capability and the readout strategy.

The first reticle-size prototype is expected to be taped-out during 4Q 2018.

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Presenter: CARTIGLIA, Nicolo (INFN Torino (IT))

Session Classification: POSTER Session

Track Classification: ASIC
FE65-P2: a Pixel Prototype Readout Chip in 65nm Technology for HL-LHC Upgrades

Thursday, 14 September 2017 11:55 (25 minutes)

We present the latest results of the FE65-P2 pixel readout test chip. This is a 64 by 64 pixel matrix on 50 um by 50 um pitch, produced in 65nm CMOS technology at the end of 2015. FE65-P2 was designed to demonstrate small pixel performance and stable operation down to 500 electron threshold even with the front end pixel amplifiers embedded in a synthesized logic environment. The FE65-P2 results inform the ongoing design of a large format (400 by 192 pixels) demonstrator readout chip to be produced by the RD53 collaboration in mid 2017.

Summary
FE65-P2 makes use of layout scheme dubbed “analog islands in a digital sea”, where each set of four analog front ends (analog quad) is fully surrounded by synthesized logic, which is not a step and repeat layout, leading to a slightly different environment around each analog quad. A comprehensive substrate isolation strategy was used to achieve the required low stable threshold and excellent uniformity. FE65-P2 chips are being bump bonded to miniature matching sensors to allow full module performance studies. Test results will be presented including irradiation and beam tests. This work is carried out in the context of the RD53 collaboration, which is developing the pixel readout technology to cope with the high rate and radiation together with low noise and low power requirements for the High Luminosity LHC upgrades of the ATLAS and CMS experiments.
Quad Module Hybrid Development for the ATLAS Pixel Layer Upgrade

Tuesday, 12 September 2017 17:30 (15 minutes)

A quad chip module hybrid—assembled with FE-I4 chips—has been fabricated to test performance in a serially powered module chain as would be used in the upgraded ATLAS pixel layer at the High Luminosity LHC. This poster presents the results of the development of a flex circuit board interface for the quad chip modules and system integration tests of modules installed on an I-beam. Experience from these hybrid assemblies will inform the design of a flex hybrid for the new large format readout chip, RD53A, which will be produced in 2017 by the RD53 collaboration.

Summary

A quad chip module hybrid—assembled with FE-I4 chips—has been fabricated to test performance in a serially powered module chain as would be used in the upgraded ATLAS pixel layer at the High Luminosity LHC. This poster presents the results of the development of a flex circuit board interface for the quad chip modules and system integration tests of modules installed on an I-beam. Experience from these hybrid assemblies will inform the design of a flex hybrid for the new large format readout chip, RD53A, which will be produced in 2017 by the RD53 collaboration.

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Presenter: DUNNE, Katherine (Lawrence Berkeley National Lab)
Session Classification: POSTER Session
Track Classification: Production, Testing and Reliability
Design and Characterization of the Readout ASIC for the BESIII CGEM Detector

Thursday, 14 September 2017 11:05 (25 minutes)

TIGER (Turin Integrated Gem Electronics for Readout) is a mixed-mode ASIC for the readout of signals from CGEM (Cylindrical Gas Electron Multiplier) detector in the upgraded inner tracker of the BESIII experiment, carried out at BEPCII in Beijing. The ASIC includes 64 channels, each of which features a dual-branch architecture optimized for timing and energy measurement. The input signal time-of-arrival and charge measurement is provided by low-power TDCs, based on analog interpolation techniques, and Wilkinson ADCs, with a fully-digital output. The design and test results of TIGER first prototype are presented showing its full functionality.

Summary

The ASIC presented is developed for the readout of signals coming from the CGEM detector of the BESIII experiment. The detector is scheduled to be installed during the 2018 upgrade and features an innovative, lightweight three-layer triple-CGEM tracker with analog readout. This type of readout employs a charge centroid method to improve the spatial resolution while keeping the front-end channels to a relatively small number of about 10000.

In order to meet the requirements set by the experiment, the readout ASIC has been designed to operate with an input capacitance of about 100 pF, input dynamic range 1-50 fC, power consumption <10 mW/channel, and event rate of 60 kHz/channel. Additionally, a time resolution better than 10 ns is required in order to time-tag each hit and operate the detector in the so-called "micro-TPC" mode thus improving the spatial resolution of angled tracks.

Designed in a 110 nm CMOS technology, the ASIC consists of 64 channels, references and bias generators, a digital global controller and an internal test pulse calibration circuitry. Each channel comprises an analogue front-end for signal amplification and shaping and a mixed-mode back-end to digitize the information.

The front-end is composed of a charge sensitive amplifier coupled to two shapers, each of which is connected to a discriminator with a programmable threshold. The time-branch shaper generates a fast signal, optimized for timing measurements with a leading-edge threshold, while the energy-branch shaper provides a slower signal, allowing for better signal integration and equivalent noise charge (ENC) optimization.

The time measurement is performed by two low-power TDCs, each of which is composed by four time-to-amplitude converters and a 10-bit Wilkinson ADC. A quad-buffered Sample&Hold (S/H) circuit is connected at the output of the energy-branch shaper, operating as a digitally controlled peak detector. The signal peak amplitude is digitized by the same Wilkinson ADC used by the TDC, so the charge information is obtained either from the time-over-threshold (ToT) or the S/H circuit. The event data are sent to a digital block, running at 160 MHz, that controls the chip operations, handles the global and channel registers configuration and manages the off-chip data transmission through 2 LVDS output links.

The ASIC has been electrically characterized and all the specified requirements are met within the limited power budget of 10 mW per channel. The S/H linearity is very good (less than 0.2%) for an input charge in the 5-40 fC range. The TDC resolution is better than 50 ps r.m.s., such that its contribution to the intrinsic time resolution becomes negligible. The equivalent noise charge (ENC)
with 100 pF input capacitance is about 2500 electrons. Despite the fact that the measured noise performance is already adequate for our application, PSRR, interference and grounding conditions are currently under study. First results of tests with the CGEM prototype using cosmic rays and a 90Sr source will be presented.

This research activity has been performed within the BESIIICGEM Project, funded by European Commission in the call H2020-MSCA-RISE-2014.

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**Presenter:** COSSIO, Fabio (Politecnico di Torino e INFN Torino (IT))

**Session Classification:** ASIC

**Track Classification:** ASIC
FPGA Based Wireless Time Interval Measurement System with Picosecond Resolution

Thursday, 14 September 2017 11:05 (20 minutes)

We present a theoretical analysis, simulation and implementation results of an FPGA-based wireless Time Interval Measurement (TIM) system. The TIM features a single channel TDC with a Serial Peripheral Interface (SPI) and wireless transmission. The TDC is based on the Vernier ring oscillator method to achieve both high resolution and wide dynamic range. The TDC architecture with an SPI is implemented in Altera Cyclone IV Device, and a wireless ZigBee module (IEEE 802.15.4 standards) is used for transmission of the measured time interval values. The paper concludes with the description of the prototype application to investigate SPAD after-pulsing.

Summary

Timing measurement is used to determine most of the physical quantities like the energy of a particle or crossing time. In mixed-signal systems used for timing measurement, TDCs are the vital building blocks used for digitizing of analog signals in time domain. The emergence of High Energy Physics (HEP) detectors measuring in sub 10 ps-rms resolution demand a high-resolution TDC for timing measurements in the ps-rms resolution to realize the full potential of today’s HEP detectors.

Compared to full-custom CMOS ASIC, FPGAs have advantages in the implementation of fully digital TDC architectures as it provides benefits such as cheaper development cost, customizability, etc. The prototype discussed in this paper is implemented in an FPGA. The standard uncertainty for the time intervals from 0 to 30 ns were less than 17.43 ps-RMS with the resolution of approximately 10 ps and reliable wireless data transmission using Zigbee protocol.

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Presenter: Mr SRINIVASAN, Balaji (LICET)

Session Classification: Programmable Logic, Design Tools and Methods

Track Classification: Programmable Logic, Design Tools and Methods
Monolithic Pixel Development in 180 nm CMOS for the Outer Pixel Layers in the ATLAS Experiment

The ATLAS experiment at CERN plans to upgrade its Inner Tracking system for the High-Luminosity LHC in 2026. After the ALPIDE monolithic sensor for the ALICE ITS was successfully implemented in a 180nm CMOS Imaging Sensor technology, the process was modified to combine full sensor depletion with a low sensor capacitance (~2.5fF), for increased radiation tolerance and low analog power consumption. Efficiency and charge collection time were measured with comparisons before and after irradiation. An overview of the measurements and the ATLAS-specific development towards full-reticle size CMOS sensors and modules in this modified technology will be given.

**Summary**

The Inner Tracking system (ITk) of the ATLAS detector[1] will be upgraded in 2026 for the High-Luminosity Large Hadron Collider. The present ITk pixel detector is based on hybrid sensors. Monolithic active pixel sensors (MAPS) can be produced in commercial CMOS technology and offer higher resolution and lower material in the vertex detector.

ALICE is the first experiment at the LHC implementing a large silicon tracker with MAPS. The ALPIDE monolithic sensor implemented in a 180 nm CMOS Imaging Sensor technology[2] features a high resistivity epi-layer (>1 kΩ-cm) with possibility to apply reverse bias (-6V). However, the sensor depletion volume is limited to the region around the collection electrode and signal charge generated outside the depleted area is still collected primarily by diffusion. The required tolerance to non-ionizing energy loss (NIEL) in the outer ATLAS pixel layers is $1.5\times10^{15}$ 1 MeV $n_{eq}/cm^2$, two orders of magnitude higher than the ALICE ITS. This requires a drift field and hence depletion over the full sensitive layer to reduce charge carriers collection time and reduce the probability of charge trapping signal loss. Moreover, a short charge collection time, combined with a fast front-end, is fundamental to separate hits from consecutive bunch crossings (25 ns).

For use in high radiation environments like the ATLAS ITk, a process modification in this technology developed in collaboration with the foundry[3] creates a deep planar junction to obtain full depletion of the epitaxial layer and charge collection by drift, while maintaining a small collection electrode with a small sensing node capacitance (~2.5 fF) essential for a low power pixel design. The process modification has been tested with the Investigator pixel chip[4], a sensor characterization device designed in the framework of the monolithic sensor development for ALICE ITS. It implements different pixel geometries giving direct access to the sensing node transient voltage to study signal collection characteristics and detection efficiency. $^{90}$Sr source measurements show charge collection is virtually unaffected by non-ionizing energy loss up to $10^{15}$ 1 MeV $n_{eq}/cm^2$. Beam test measurements show no efficiency loss after irradiation.

This opened the way to the design of two large scale demonstrators for the ATLAS ITk outermost pixel layers, where the expected hit rate is 0.4 to 2 MHz/mm$^2$. MALTA contains a 512×512 pixel matrix of 36.4 μm pitch featuring a 1 μW frontend with in-pixel discrimination based on ALPIDE[5] with a time response < 20ns. The full asynchronous readout without clock distribution over the matrix reduces digital power. TJ-Monopix implements the same front-end as MALTA combining it with the well-established column drain architecture[6]. Charge collection and test beam results and an outlook on the chip development will be presented.

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Presenter: KUGATHASAN, Thanushan (CERN)

Session Classification: ASIC

Track Classification: ASIC
We report on the design and performance of UFSD (Ultra-Fast Silicon Detectors) and their challenge for electronics systems. UFSD are segmented thin Low-gain Avalanche Detectors (LGAD) with measured time resolution of 30ps. The combined accurate measurement of time and position for charged particle in UFSD offers unique physics capabilities such that they are being considered for use in the HL-LHC by ATLAS and CMS because of their ability to suppress backgrounds from high-luminosity pile-up.

We describe the status of the R&D involving three manufacturers (CNM, FBK, HPK) and radiation campaigns up to a neutron fluences of $6e15 \text{n/cm}^2$ permits and assess the special challenges their use in HL-LHC would entail.

**Summary**

1. **Description of Low-gain Avalanche Detector (LGAD) technology**

   We are describing the basics of the LGAD, which are ordinary silicon sensors with an added p-layer to generate internal charge multiplication.

2. **Simulation program Weightfield 2 (WF2)**

   The design, operation and future development is aided by WF2, (presented in another TWEPP contribution). WF2 permits prediction of sensor performance as a function of geometry (area, thickness) and radiation levels and different readout options.

3. **Production of UFSD**

   The production program of three manufacturers is described and their product compared. The results of an irradiation campaign with fluences up to $6e15 \text{n/cm}^2$ have permitted to quantify the radiation damage and start a mitigation program.

4. **Gain and Timing resolution**

   We show that the doping profile of the p-layer determines the gain, and identify the gain as the parameter ruling the timing resolution. The gain and timing resolution have been measured in many beam and $\beta$-source tests for a variety of LGAD doping levels, geometries and radiation levels.

5. **Challenges for the readout electronics**

   Challenges for the readout electronics and options for the application at the HL-LHC are discussed briefly (they are presented in another TWEPP contribution).

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**Session Classification:** Other

**Track Classification:** Other
A Compact Tiled Readout for Hamamatsu H13700 PMTs with 256 Pixels

Wednesday, 13 September 2017 16:45 (15 minutes)

Recent advances in light detectors has led to the introduction of a number of highly pixelated but compact photomultiplier tubes. These PMTs require compact readout electronics that directly couple to the PMTs, are high performance and can provide timing resolution on par with the PMT. In this paper we propose a compact readout device for the Hamamatsu H13700 PMT with 256 pixels. The design is based on the TARGETX waveform sampling chip developed at the University of Hawaii. The proposed electronics allow for tile assembly and operation for multiple of such PMTs.

Summary

One of the factors that impacts the accuracy of tracking particles is the number of detector channels. Higher channel count and larger area coupled with good timing accuracy are some of the proposed specifications for new detectors or upgrades to existing detectors. Recent advances in light detectors such as MCP-PMTs show promising performance in high speed photon detection while providing a dense array of pixels. The main problem with the new detectors is developing compact readout electronics that can match the high channel density of the PMTs in a form factor that allows tiling and abutting of the PMTs to cover a larger area. One traditional approach is to attach pre-amp boards to the PMT, amplify and condition the signal and then send analog signals via special cables to legacy crate based readout electronics in an electronics hut. This solution quickly adds to the cost, power draw and will create thermal issues.

We propose a full waveform sampling compact readout electronics that attaches directly to such PMTs. The H13700 PMT is a 256 channel device with a ~2”x2” footprint. The readout electronics are based on the already developed TARGETX waveform sampling ASIC developed at the University of Hawaii. We used 16 TARGETX chips to readout 256 channels of the PMT. The TARGETX is has an internal storage of 16384 samples equivalent to ~16us of memory when operating at 1GSa/s. This long buffer will allow operation in long latency large detector operations. The analog signal is brought into the readout chip directly eliminating the need for preamps and impedance matching which leads to tremendous power savings. The form factor of the readout PCB and vertical integration allows for abutting the PMTs and operation in tile configuration. Use of full waveform sampling and built in feature extraction in the front end electronics makes this design attractive for large detectors. Potential applications include the particle identification (PID) detector for Electron Ion Collider.

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Presenter: MOSTAFANEZHAD, Isar (Nalu Scientific, LLC)

Session Classification: POSTER Session
Track Classification: Systems, Planning, Installation, Commissioning and Running Experience
The NaNet Project: Heterogeneous Real-Time Stream Processing in the Low Level Trigger of the NA62 Experiment

Wednesday, 13 September 2017 16:45 (15 minutes)

Our work aims at improving the performances of the NA62 low-level trigger implementing a real-time stream processing architecture based on an orchestrated combination of heterogeneous computing devices (CPUs, FPGAs and GPUs).
To enable it we devised NaNet, a FPGA-based PCI-Express Network Interface Card with processing and GPUDirect capabilities, which supports multiple link technologies (1/10/40GbE and custom ones).
We have demonstrated the effectiveness of the method by retrofitting the RICH detector to generate refined physics-related primitives.
Results obtained during the first months of 2017 run are presented and discussed, along with a description of the latest developments in the NaNet architecture.

Summary

Over the last few years several works have demonstrated the effectiveness of the integration of GPU-based systems in high level trigger of different experiments. On the other hand the use of GPUs in the low level trigger systems, characterized by stringent real-time constraints, such as tight time budget and high throughput, poses several challenges. In the NA62 experiment at CERN streams of raw data primitives produced in the detectors are transmitted to a centralized processing system that is in charge of generating the low level trigger signal within 1 ms time budget.
Our approach aims at improving the low level trigger performances distributing this processing over the whole chain starting from the earliest possible stages, i.e. the detectors, by operating in real-time on the data streams with an orchestrated combination of heterogeneous computing devices (CPUs, FPGAs and GPUs).
To enable such distributed real-time computing architecture we devised NaNet, a FPGA-based PCI Express Network Interface Card with processing and GPUDirect capabilities, which supports multiple link technologies (1/10/40GbE and custom ones).
We have demonstrated the effectiveness of the method by harvesting the computing power of last generation nVIDIA Pascal GPUs and of the FPGA hosted by NaNet to build in real-time refined physics-related primitives for the RICH detector, as the the knowledge of Cerenkov rings parameters allows to build more stringent conditions for data selection at low trigger level (L0). Indeed the refined RICH primitives can be also profitably employed in the software trigger levels.
In the standard configuration the online PC farm, devoted to process the events in two steps (L1 and L2) in order to decide if the events are interesting for permanent storage, do not build rings starting from the RICH raw data, due to limitation in computing power. We are working to send this information also to the PC farm for the required events, under a rate of 100 kHz and a latency small enough to accomplish all the requests before the start of the next burst (order of 5 s). We believe that this will give a not negligible contribution to the total rejection and that the physics potential of the experiment will benefit from it. Results obtained during the first months of 2017 NA62 run are presented and discussed, along with a detailed description of the latest developments in the NaNet architecture.
Primary authors:  LONARDO, Alessandro (Sapienza Universita e INFN, Roma I (IT)); VICINI, Piero (Sapienza Universita e INFN, Roma I (IT)); BIAGIONI, Andrea (Universita e INFN, Roma I (IT)); PONTISSO, Luca (Sapienza Universita e INFN, Roma I (IT)); CRETARO, Paolo (INFN - National Institute for Nuclear Physics); LAMANNA, Gianluca (INFN e Laboratori Nazionali di Frascati (IT)); SOZZI, Marco (Universita di Pisa & INFN (IT))

Presenter:  LONARDO, Alessandro (Sapienza Universita e INFN, Roma I (IT))

Session Classification:  POSTER Session

Track Classification:  Trigger
Readout Electronics for the First Large HV-MAPS Chip for Mu3e

Wednesday, 13 September 2017 16:30 (15 minutes)

Mu3e is an upcoming experiment searching for charged lepton flavor violation in the rare decay $\mu \rightarrow eee$. A silicon pixel tracker based on 50 um thin high voltage monolithic active pixel sensors (HV-MAPS) in a 1T magnetic field will deliver precise vertex and momentum information. The MuPix HV-MAPS chip combines pixel sensor cells with integrated analog electronics and a complete digital readout. For the characterization of the first large MuPix system on chip a dedicated readout system was developed.

The dedicated readout chain and the first results from the characterization of the large scale MuPix prototype will be presented.

Summary

The Mu3e experiment searches for charged lepton flavor violation in the rare decay $\mu \rightarrow eee$. In the standard model the decay $\mu \rightarrow eee$ is extremely suppressed with a BR $<10^{-54}$, so that any observation would be a clear sign of new physics. The goal of the first phase of the Mu3e experiment is to reach a branching ratio sensitivity of $10^{-15}$, which requires the observation of $10^8$ muons decays per second over several years of runtime. In order to reject both physics and combinatorial background, decay vertex, particle momenta and decay time have to be precisely measured. The hit resolution of the tracking detector of the Mu3e experiment is dominated by multiple Coulomb scattering. Therefore the decay vertex position and the particle momenta are determined with the help of an ultra-thin pixel detector in a 1T magnetic field.

The pixel detector is based on high voltage active monolithic pixel sensors (HV-MAPS) thinned to 50 um. The HV-MAPS developed for the Mu3e experiment, called MuPix, is a system on chip combining sensor diode, digitization including precise time-stamp, zero-suppression, fast on-chip serialization and high speed differential data output. In the last two years the first prototype with full system on chip capabilities was very successfully tested. This year the first large MuPix prototype with full pixel column length will be under investigation. This new MuPix8 has about 1cm times 2cm active area, which is half the area of the final sensor used for the Mu3e experiment.

For the sensor characterization of this complex ASIC, a dedicated readout chain was developed. It’s based on an ASIC test board with ultra clean power distribution and a commercial FPGA board. The ASIC test board provides low voltage, high voltage, temperature measurement and test-pulse and is connected to the FPGA card via LVDS links. The FPGA card controls the MuPix chip via a SPI protocol and receives the continuous serial data stream from the MuPix at 1.25 GBit/s. The system has been successfully integrated in laboratory test setups and was used to build test beam telescopes with four to eight MuPix planes.

The dedicated readout chain and the first results from the characterization of the large scale MuPix prototype will be presented.

Primary author: WIEDNER, Dirk (Ruprecht-Karls-Universitaet Heidelberg (DE))

Presenter: WIEDNER, Dirk (Ruprecht-Karls-Universitaet Heidelberg (DE))
**Session Classification:** POSTER Session

**Track Classification:** Systems, Planning, Installation, Commissioning and Running Experience
Design and Performance of the Upgrade of the CMS L1 Trigger

Thursday, 14 September 2017 14:50 (25 minutes)

The upgraded CMS Level-1 trigger is designed to improve the performance at high luminosity and large number of simultaneous inelastic collisions per crossing (pile-up). During the technical stop at the beginning of 2016, all the electronic boards of the CMS Level-1 trigger have been replaced and the upgraded electronics tested, and commissioned with data. The upgrade of both the Stage-1 and Stage-2 happened during the shutdown of the LS1. Smarter, more sophisticated, and innovative algorithms are now the core of the first decision layer of CMS. The upgrade reduces the trigger rate and improves the trigger efficiency for a wide variety of physics signals. In this presentation the upgraded CMS Level-1 trigger design and its performance are described.

Summary

During its second run of operation, the LHC delivered proton-proton collisions at a centre-of-mass energy of 13 TeV with a peak instantaneous luminosity of $1.5 \times 10^{34} cm^{-2}s^{-1}$, almost double the peak luminosity reached during Run1 and far larger than the design value. To maintain acceptance for proton and heavy ion collision events of interest without exceeding the 100 kHz limit, the CMS Level-1 (L1) trigger has been being upgraded. The upgraded system makes use of new Xilinx Virtex-7 based AMC cards form the microTCA technology.

The L1 calorimeter trigger, which finds electrons, photons, tau leptons, jet candidates and computes energy sums has been upgraded implementing isolation requirement, multivariate regression, and pile-up mitigation techniques in order to reach acceptable performance.

The CMS muon detector was designed for preserving the complementarity and redundancy of three separate muon detection systems, Cathode Strip Chambers (CSC), Drift Tubes (DT) and Resistive Plate Chambers (RPC), until they were combined at the input to the Global Trigger. The upgrade of the muon trigger aimed at exploiting the redundancy of the three muon detection systems earlier in the trigger processing chain in order to obtain a high-performance trigger with higher efficiency and better rate reduction, implementing pattern recognition and MVA (Boosted Decision Tree) regression techniques directly in the trigger boards.

In addition, the new global trigger is capable of evaluating complex selection algorithms such as those involving the invariant mass of trigger objects.

The talk will cover the technological aspects of the Run II calorimeter trigger system. Results of its performance during the 2016 collisions of the LHC will be presented.

Primary author: BORTIGNON, Pierluigi (University of Florida (US))

Presenter: FOUNTAS, Costas (University of Ioannina (GR))

Session Classification: Trigger

Track Classification: Trigger
Opening

Opening from TWEPP Chairman

Summary

**Presenter:** MARCHIORO, Alessandro (CERN)
Welcome

from Alex Grillo, Chairman Local

Summary

Presenter: GRILLO, Alex (University of California, Santa Cruz (US))
Readout Electronics Systems for Liquid Argon TPCs in Neutrino Experiments

Wednesday, 13 September 2017 10:15 (45 minutes)

R&D studies of readout electronics systems for accelerator based neutrino experiments have been carried out since 2008. The CMOS based cryogenic readout electronics is the enabling technology for giant (> 10kT) LAr TPC (Liquid Argon Time Projection Chamber) in neutrino experiments, which also has potential to be used in other noble liquid TPC based experiments (dark matter search, neutrino- less double beta decay, etc.). The readout integrated with active detector is an important concept being followed in the development of readout electronics systems in LAr TPC experiments.

The readout electronics system for neutrino experiments in Short Baseline Neutrino Program (MicroBooNE and SBND) and Long Baseline Neutrino Program (DUNE) will be presented, where CERN Neutrino Platform has significant involvement in both programs. The readout electronics system for ProtoDUNE-SP currently being installed in EHN1 at CERN will be described in detail. Performance studies of cryogenic readout electronics systems will be presented.

Summary

Primary author: CHEN, Hucheng (Brookhaven National Laboratory (US))

Presenter: CHEN, Hucheng (Brookhaven National Laboratory (US))

Session Classification: Invited Talk
Design and Radiation Tests on a LED Based Emergency Evacuation directional light

Wednesday, 13 September 2017 17:45 (15 minutes)

A LED (Light Emitting Diode) based directional lighting has been designed to indicate the best evacuation direction for applications like the LHC tunnel. The design includes constraints for redundancy required by safety systems and for components selection by radiation effects. Prototype lighting units were irradiated in CERN’s CHARM facility and were operational up to a Total Integrated Dose (TID) of 870 Gy. This paper describes the basic design and the irradiation effects.

Summary

Directional lighting that guide the personnel present in confined spaces is used in some safety systems, but this type of equipment is not qualified to operate in a radiation environment. The use of directional lighting was investigated during the tests performed in 2014 simulating an accidental liquid helium release into the 27 km circumference LHC tunnel that lies about 100 m below ground and has 9 access shafts. The LHC safety system provides, in its present status, excellent protection to the personnel present in the tunnel although a directional lightning system would be a useful addition to avoid personnel going initially towards the wrong exit shaft when an evacuation alarm is present.

The LHC tunnel curvature imposes a maximum distance between directional lights of 320 m in order to indicate the personnel whether to go to the left or right in case of an evacuation procedure. The light design shall be visible from up to at least the line of sight while limiting the amount of glare to which the personnel is exposed when working in close proximity.

The light emitting elements are red and green LEDs XLamp® XP-E2 model manufactured by Cree®. The LED light is concentrated by using a lens model IRIS-M manufactured by Ledil made of PMMA material and with a viewing angle of 29°.

At the nominal LED current of 350 mA, the red and green LEDs produce an approximate luminous flux of respectively 60 lm and 100 lm. These luminous flux through the IRIS lens would be far too bright resulting in glare that exceed the upper vision tolerance threshold (about 300’000 cd/m²) and may present a hazard to the personnel working in close proximity to the light source.

To address glare, the XLamp LEDs are used with a very strong derating (current of 5 mA and 2.5 mA respectively for the red and green LED) and by using per color up to five Ledil IRIS lenses in parallel to increase the light emittance area to about 57 cm².

The relatively low currents permit easily to design a robust radiation scheme for which both the dc power supply and the safety control equipment stays in a radiation-protected area and only the passive components (resistors and diodes) are located in the hazardous area.

Per color, a cluster of ten LEDs and its associated IRIS lens was irradiated in the CHARM test facility. During the irradiation, five samples for each color were kept respectively ON and OFF; and their luminance was measured during the six CHARM technical stops. The total accumulated dose was 870 Gy and no failure occurred. No darkening was observed on the PMMA material of the lenses.

The luminance of the red LEDs decreased by about 80% after the irradiation, however from a physiological point of view the luminance stayed constant as the human eye compensated this variation.
The luminance of the green LEDs decreased by less than 40%.

**Primary authors:** CASAS-CUBILLOS, Juan (CERN); TRIKOUPIS, Nikolaos (CERN)

**Presenter:** TRIKOUPIS, Nikolaos (CERN)

**Session Classification:** POSTER Session

**Track Classification:** Radiation Tolerant Components and Systems
High-performance analog-to-digital converters (ADCs) are becoming essential building blocks in many applications including optical communications, high-speed test equipment such as real-time oscilloscopes, and high-energy particle physics, etc. While several ADC architectures have been proposed, SAR (Successive Approximation Register) has become the de facto preferred design, because of its low power, small silicon area, and scalability with advanced CMOS technologies. Time-interleaving architecture is a promising way to further improve the conversion rate in a given technology and push it to 100GS/s. This talk will give an overview of high-speed time-interleaved SAR ADC design, the working principle, design challenges and possible solutions. In the end, a 64 GS/s 8-bit time-interleaved ADC implemented in a 28 nm CMOS process will be presented as an example, including the proposed design techniques, calibration methods, and silicon measurement results.

Summary

**Presenter:** GUI, Ping (Southern Methodist University (US))

**Session Classification:** Invited Talk
LCLS-II: A High Repetition Rate X-Ray Laser Facility

The Linac Coherent Light Source (LCLS) is in the midst of a major upgrade called LCLS-II \(^1\). This upgrade will add a 4 GeV continuous-wave superconducting electron accelerator to the LCLS complex, delivering a 10,000-fold increase in repetition rate and average x-ray brightness. Currently scheduled to achieve first light in 2020, LCLS-II will enable a broad range of experiments over a 0.2 to 5 keV photon energy range presently not possible to date\(^2\). These experiments will be conducted in three newly developed x-ray instruments. The scope, projected capabilities and status of the LCLS-II project and associated x-ray instruments will be presented as well as exemplary science applications.

References
\(^1\) J. N. Galayda, Proceedings of the 5th International Particle Accelerator Conference (IPAC’14), 15-20 June 2014, Dresden, Germany

Summary

Presenter:  FRITZ, David M. (SLAC National Accelerator Laboratory)

Session Classification:  Invited Talk
Advance Node Impact on Physical Design and Resulting Tool Support - Electrically Aware Design Flow

Friday, 15 September 2017 09:30 (1h 30m)

- New devices (FinFETs) and fluid guardrings
- Double/ Multiple Patterning aka coloring
- Gridded/ track based placement and routing methodology
- In-design dynamic/ post-edit DRC checking to support new constraints including color and grid checks

Abstract

Continuous advancement in process technology following Moore’s law over the past few decades has greatly increased IC design complexity, not just for designers but also for EDA tools. The drive to reduce feature size beyond optical resolution of visible and ultra-violet light has led to multiple masks/patterns for same layer to allow for a more compact layout. Need for greater scaling and manufacturing accuracy has led to a self-aligned fabrication process requiring gridded, unidirectional interconnects. At the same time, new devices such as tri-gate finFETS have been introduced to address power, leakage and variability associated with these processes. In addition to more restrictive and complex design rules for manufacturability and process characteristics, EDA tools need to account for changes in design methodology such as highly gridded placement and routing. This presentation will cover these tool enhancements and changes to meet the process technology requirements of these nodes, for both devices and interconnects, with focus on physical implementation.

Summary

Presenter: NAIR, Sravasti (Cadence Design Systems)

Session Classification: TUTORIAL
2. Electrically Aware Design Flow

- In-design extraction and analysis of parasitics, EM/IR and LDE parameters
- Resimulation with parasitics and LDE parameters from a layout in-progress (prior to sign-off)
- Using electrical constraints to verify and meet design requirements

Abstract

Advanced nodes have introduced many new design challenges including significantly greater impact of parasitics and other electrical effects, and design iterations are becoming increasingly costly as well. It is no longer possible to push out analyzing the effect of parasitics and checking for reliability issues till the very end of the design cycle i.e. during sign-off. It is now almost imperative to perform electrical analysis, specifically simulating with parasitics and layout dependent device parameters derived from layout, and checking for Electro-migration issues and IR Drops. This presentation covers such an in-design methodology which also helps designers meet design requirements through electrical constraints, and verify that these constraints are being followed in the physical implementation. Once identified, issues such as Electro-migration violations can be fixed easily with guidance and assistance from the tool, and the design can be re-verified quickly while the layout is still in progress, without waiting till sign-off.

Summary

Presenter: NAIR (CADENCE DESIGN SYSTEMS), Sravasti

Session Classification: TUTORIAL
Moore’s Law has entered a new frontier as device scaling continues to excel in 10nm and beyond. As the physical dimension of devices and interconnect are being shrunk, the design rules and the design flow, for both design community and EDA community, face unprecedented complexity. Conventional design optimization techniques also need to take the novel process technologies, such as multi-gate devices (e.g., FinFET), spacer technology, and self-aligned multiple patterning lithography, into account to achieve the best possible performance, power, and area for a design with more and more functionalities integrated into one single chip.

In this presentation, first, we will talk about simulation technologies to handle special effects introduced by advanced process nodes, such as high transistor speed, high transistors/RC capacities and reliability effects etc. with reasonable speed and performance while maintaining spice simulation accuracy. Secondly, we will also discuss about advanced integrated simulation environment targeting for different design phases to meet the tight design window. Finally, we will touch upon the importance of system integration for advance process nodes and bring up the solution for the system integration, which include IC/Package/PCB, from both implementation and analysis point of views.

Advanced Process Nodes Simulation Strategy
a. Simulation challenge for advanced process nodes.
   b. Simulation technology overview
   c. Reliability simulation
      i. Aging simulation
      ii. Self-heating simulation
      iii. EMIR Simulation
   d. Summary

Advanced integrated Simulation environment
a. Why we need integrated simulation environment?
   b. Environment for individual block
   c. Environment for block integration.
   d. Environment for verification and regression.
   e. Summary
   f. System integration: integrated IC/package/PCB together
      a. Implementation flow
      b. Analysis flow

Summary

Presenter: CHEN, Ping (Cadence Design Systems)
Session Classification: TUTORIAL
Advanced Integrated Simulation Environment

a. Why we need integrated simulation environment?
b. Environment for individual block
c. Environment for block integration.
d. Environment for verification and regression.
e. Summary

Summary

Presenter: CHEN (SR. STAFF APPLICATION ENGINEER CUSTOM IC & SIMULATION - CADENCE DESIGN SYSTEMS), Ping

Session Classification: TUTORIAL
System Integration: Integrated IC/Package/PCB Together

a. Implementation flow
b. Analysis flow

Summary

Presenter: CHEN (SR. STAFF APPLICATION ENGINEER CUSTOM IC & SIMULATION - CADENCE DESIGN SYSTEMS), Ping

Session Classification: TUTORIAL
Advances in Image Sensors Technologies

Tuesday, 12 September 2017 10:15 (45 minutes)

Image sensor innovation continues after more than 50 years of development. New image sensor markets are being developed while old markets continue to grow. Higher performance and lower cost image sensors are enabling these new applications. Although CMOS image sensors dominate the market, CCDs and other novel image sensors continue to be developed. In this talk we discuss trends in image sensor technology and present results from selected workshop papers. Moreover, we will discuss developments in small pixels, stacked die image sensors, time of flight image sensors, SPAD image sensors, low light level sensors, wide dynamic range sensors and global shutter image sensors.

Summary

Presenter: Dr FOWLER, Boyd (Omnivision)

Session Classification: Invited Talk
Trends in Radiation Effects for sub-65 nm Technologies

Tuesday, 12 September 2017 14:00 (45 minutes)

Radiation-induced degradation and soft errors in electronics are important reliability issues for various space, defense and commercial applications. The continual miniaturization of CMOS technologies and the introduction of multi-gate device structures to mitigate short channel effects have had mixed consequences for radiation tolerance. The aim of this presentation is to review the current radiation-effects trends dominating sub-65 nm technologies for space and defense applications. Device structure and doping levels determine sensitivity to Total Ionizing Dose (TID) effects (e.g. sub-threshold leakage, threshold voltage shifts). Thinner insulators and higher dopings associated with scaling have reduced TID effects; however, fully-depleted silicon-on-insulator (FDSOI) devices, typically used to mitigate transient effects, have been shown to exacerbate TID effects due to trapped charge in the buried oxide. Typically parts are tested up to a maximum dose of 1 Mrad and special considerations should be made for the validity of these trends at the high doses of interest in the LHC community. Beyond TID effects, Scaling has resulted in increased sensitivity to Single Events (soft errors). This trend is attributed to the reduced operating voltages, decreased feature sizes, and higher packing densities, which result in low critical charge per node and more nodes within a region of influence of a single event. There is an increased interest in the use of commercial-off-the-shelf (COTS) parts in radiation environment because of accessibility and cost; here, the primary concern for radiation effects when using COTS is Single Event Latchup sensitivity which is tested using two photon absorption techniques. A brief discussion on radiation tolerance of beyond CMOS and other emerging technologies will be provided.

Summary

Presenter: WEEDEN-WRIGHT, Stephanie (Lipscomb University)

Session Classification: Invited Talk
Beyond 100Gbps High-Speed Optical Data Interconnects

Wednesday, 13 September 2017 14:00 (45 minutes)

Modern data acquisition techniques employed in particle physics create large amounts of digital data that must be transmitted to remote electronics and computers for further processing. Increasingly, bandwidth requirements preclude the use of PCB traces and traditional copper cabling, even for modest interconnection length. Fortunately, novel copper and optical flyover solutions are being developed to go around the limits of traditional PCB and cabling, enabling transport of data at rates exceeding 28 Gb/s per lane over a range of distances. We will describe advances in miniature, very high speed connectors, micro-coax and micro-twinax cabling, and on board optical transceivers that can meet present and future interconnect challenges. We will show how they can be customized to the harsh environment and limited space requirements that are typical of these applications.

Summary

**Presenter:** VERDIELL, Marc (Samtec Optical Group)

**Session Classification:** Invited Talk
CMOS Biochips: The Good, the Bad, and the Hype

Thursday, 14 September 2017 10:15 (45 minutes)

In the past two decades, there has been numerous attempts to take advantage of semiconductor solutions, broadly defined, to create high-performance biosensors and bio-molecular detection devices. The goal has always been to create molecular diagnostics technologies that offer the cost efficiency, miniaturization capabilities, and manufacturing robustness of consumer electronics devices. The outcome so far, has not been very exhilarating and unfortunately there has been few impactful products based on such efforts.

In this talk, we will discuss the use of CMOS processes and IC’s for biotechnology in the form of integrated biochips. The focus will be not only the design, manufacturing, and the packaging tradeoffs of biochips, but also on the applications requirements and ideal use models in molecular biology. We will also discuss, in detail, the recently implemented CMOS biochips for nucleic acid (DNA/RNA) testing applications.

Summary

Presenter:  HASSIBI, Arjang (InSilixa)
Session Classification:  Invited Talk
Opening

Summary
Opening

Monday, 11 September 2017 09:00 (25 minutes)

Summary

Presenter: MARCHIORO, Alessandro (CERN)
Session Classification: Opening and Welcome
Welcome

Monday, 11 September 2017 09:25 (25 minutes)

Summary

Presenter: GRILLO, Alex (University of California, Santa Cruz (US))
Session Classification: Opening and Welcome
SmartFusion2 and Arty7 radiation test results for the new developments

Wednesday, 13 September 2017 14:50 (15 minutes)

Summary

Primary author: DANZCA, Salvatore (CERN)
Co-author: TSILIGIANNIS, Georgios (Universita e INFN, Napoli (IT))
Presenter: DANZCA, Salvatore (CERN)
Session Classification: Working Group
First results on KINTEX-7 FPGA testing in mixed field radiation at CHARM facility

Wednesday, 13 September 2017 15:05 (15 minutes)

Summary

Presenter:  PLACINTA, Vlad-Mihai (Horia Hulubei National Institute for R&D in Physics and Nuclear Engineering (IFIN-HH RO))

Session Classification:  Working Group
Methodology, experimental testing and results for the evaluation of Kintex-7 operation in radiation environment

Wednesday, 13 September 2017 15:20 (15 minutes)

Summary

Presenter: BONORA, Matthias (University of Salzburg (AT))
Session Classification: Working Group
High speed links in AMC40/PCIe40

Wednesday, 13 September 2017 15:35 (15 minutes)

Summary

Presenter: CACHEMICHE, Jean-Pierre (Centre National de la Recherche Scientifique (FR))
Session Classification: Working Group
Welcome to SCIPP - Research at SCIPP and at UCSC

Monday, 11 September 2017 10:20 (45 minutes)

Summary

Presenter: Prof. NIELSEN, Jason
Session Classification: Invited Talk

Monday, 11 September 2017 11:05 (45 minutes)

Neurons in the brain interact with each other through electrical and chemical signals. These interactions determine how the brain detects and processes information. Simultaneous detection of the activity of many neurons is crucial for understanding the brain function. I will describe electrical and optical methods of interacting with neural networks developed with SCIPP’s participation. I will also discuss some of the neuroscience findings obtained obtained with the developed methods.

Summary

Presenter: Prof. SHER, Alexander (UCSC)
Session Classification: Invited Talk
MUG Agenda

Wednesday, 13 September 2017 14:50 (1h 15m)

- General news from the CERN Foundry Service Team (10min)
- Single Event Latchup in 130nm circuits (10min)
- Stability of the TID response of 130 and 65nm technologies (5min)
- Total Ionising Dose response of 65nm MOSFETs irradiated to ultra-high doses (40min)
- Plans for the simulation of irradiated transistors in 65nm CMOS (5min)
- Plans for the evaluation of the TID effects in 40 and 28nm CMOS (5min)

Summary

Presenter: FACCIO, Federico (CERN)
Session Classification: Working Group
Power Working Group

Wednesday, 13 September 2017 14:50 (1h 15m)

10 to 15 mns contribution + discussion

Summary

Presenters:  GRILLO, Alex (University of California, Santa Cruz (US)); VASEY, Francois (CERN); HANSEN, Magnus (CERN); FARTHOUAT, Philippe (CERN)

Session Classification:  Working Group