TWEPP 2017 Topical Workshop on Electronics for Particle Physics

Tuesday, 12 September 2017

POSTER Session: 1 - ASIC - Porter College Dining Hal (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

[id] title	presenter	board
[4] Low Jitter, Radiation Hardened by Design, 2.56 Gbps LVDS/SLVS Based Receiver for Analog Time Transmission	Mr FAES, Bram	B2
[6] ALICE SAMPA-ASIC Second-Prototype Qualification Studies for LHC Run 3 and Beyond	Dr TAMBAVE, Ganesh Jagannath	B3
[19] Multi-Gigabit Wireless Data Transfer for High Energy Physics Applications	Mr SOLTVEIT, Hans Kristian	B4
[25] ASICs and Readout System for a High Resolution UV Single Photon Imagining Detector	Dr SELJAK, Andrej	B5
[32] Prototype Chip for a Control System in a Serial Powered Pixel Detector at the ATLAS Phase II Upgrade	LEHMANN, Niklaus	B6
[34] Characterization of SLVS Driver and Receiver in a 65 nm CMOS Technology for High Energy Physics Applications	DE CANIO, Francesco	B7
[36] Time-to-Digital Converter with Adjustable Resolution Using a Digital Vernier Ring Oscillator	Ms AMINA, ANNAGREBAH	B8
[43] MATISSE: a Low Power Front-End Electronics for MAPS Characterization	Mr OLAVE, Elias Jonhatan	C1
[60] CACTμS : High-Voltage CMOS Monolithic Active Pixel Sensor for Tracking and Time Tagging of Charged Particles	GUILLOUX, Fabrice	C2
[74] Development of a Waveform Sampling ASIC with Femtosecond Timing for a Low Occupancy Vertex Detector	Mr OREL, Peter	C3
[90] A 4-Channel Parallel 56 Gb/s CMOS Optical Receiver for VCSEL-Based Optical Links	Dr GAO, Chaosong	C4
[94] A Digital Processing Unit of a Highly Integrated Receiver Chip for PMTs in JUNO	Ms MURALIDHARAN, Pavithra	C5
[108] Development of 4 × 28-Gbps and 4 × 14-Gbps VCSEL Array Drivers in 65 nm CMOS for HEP Applications	Dr GUO, Di	C6
[110] A 3.2 Gbps Serial Link Transmitter for CMOS Pixel Sensors in 0.18 μm CMOS Technology	Dr SUN, Quan	C7
[169] LAPA, a 5 Gb/s Modular LVDS Driver in 180 nm CMOS with Capacitively Coupled Pre-Emphasis	CARDELLA, Roberto	C8
[115] A Micropower Readout ASIC for Pixelated Liquid Ar TPCs	KRIEGER, Amanda	D1
[118] Two High-Speed Dual-Channel VCSEL Driver	ZHOU, Wei	D2
[138] The Latency Validation of the Optical Link for the ATLAS Liquid Argon Calorimeter Phase-I Trigger Upgrade	Dr GONG, Datao	D3
[139] The Characterization of a Low-Power, Low-Latency, Dual-Channel Serializer ASIC for Detector Front-End Readout	Dr GONG, Datao	D4
[119] Performance of the CATIA ASIC, the APD Readout Chip Foreseen for the CMS Barrel ECAL Electronics Upgrade at the HL-LHC	GUILLOUX, Fabrice	D5

[156] A 65 nm Macro-Pixel Readout ASIC (MPA) for the Pixel-Strip (PS) Module of the CMS Outer Tracker Detector Upgrade at HL-LHC	CERESA, Davide	D6
[157] Short-Strip ASIC (SSA): A 65nm Silicon-Strip Readout ASIC for the Pixel-Strip (PS) Module of the CMS Outer Tracker Detector Upgrade at HL-LHC	CARATELLI, Alessandro	D7
[155] Development of a Front-End ASIC for 1D Detectors with 12 MHz Frame-Rate	ROTA, Lorenzo	D8
[159] Radiation tolerant serial links for high-speed data transfer in High Energy Physics experiments	Mr MAGAZZU, Guido	E1
[167] A Low-Noise CMOS Pixel Direct Charge Sensor, Topmetal-IIa, for Low Background and Low Rate-Density Experiments	Mr AN, Mangmang	E2
[113] Design and Test of a 65nm CMOS Front-End with Zero Dead Time for Next Generation Pixel Detectors	BRAGA, Davide	E3
[170] A Monolithic HV/HR-MAPS Detector with a Small Pixel Size of 50 µm x 50 µm for the ATLAS Inner Tracker Upgrade	CASANOVA MOHR, Raimon	E4
[171] A Full Custom ASIC for Large Area 4-Dimensional Tracking	CARTIGLIA, Nicolo	E5

POSTER Session: 1 - Optoelectronics and Links - Porter College Dining Hall (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

POSTER Session: 1 - Other - Porter College Dining Hall (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

[id] title	presenter	board
[80] DQM4HEP - A Generic Online Monitor for Particle Physics Experiments	COATES, Tom	A2
[81] The Calorimeter Control Card Unit	Mr DUARTE, Olivier	A3
[162] An FPGA-Based Sampling-ADC for the Crystal Barrel Calorimeter	Mr MÜLLERS, Johannes	A4

POSTER Session: 1 - Packaging and Interconnects - Porter College Dining Hall (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

POSTER Session: 1 - Power, Grounding and Shielding - Porter College Dining Hall (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

[id] title	presenter	board
[18] ATLAS ITk Short-Strip Stave Prototype Module with Integrated DCDC Powering and Control	GREENALL, Ashley	A5
[78] Low Voltage Powering of On-Detector Electronics for HL-LHC Experiments Upgrades	BOBILLIER, Vincent	A6
[160] Gallium Nitride DC-to-DC Converter	MIKKOLA, Esko	A7

POSTER Session: 1 - Production, Testing and Reliability - Porter College Dining Hall (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

[id] title	presenter	board

[140] The Quality Assurance Test of a VCSEL Driver ASIC for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade	LIU, Tiankuan	E6
[141] The Quality Assurance of a Low-Latency, Low-Overhead, Dual-Channel Transmitter ASIC for the ATLAS Liquid Argon Calorimeter Phase-I Upgrade	LIU, Tiankuan	E7
[8] Characterization of a Prototype Batch of Long Polyimide Cables Designed for Fast Data Transmission on ATLAS ITk Strip Staves	FADEYEV, Vitaliy	F5
[44] A Multi-Channel PCI Express Readout Board Proposal for the Pixel Upgrade at LHC	Prof. GABRIELLI, Alessandro	F6
[72] Electro-Migration Driven Failures on Miniature Silver Fuses at the Large Hadron Collider	TRIKOUPIS, Nikolaos	F7
[133] Electrical and Functional Characterisation with Single Chips and Module Prototypes of the 1.2 Gb/s Serial Data Link of the Monolithic Active Pixel Sensor for the Upgrade of the ALICE Inner Tracking System.	BONORA, Matthias	F8
[173] Quad Module Hybrid Development for the ATLAS Pixel Layer Upgrade	DUNNE, Katherine	F9

Wednesday, 13 September 2017

POSTER Session: 2 - Programmable Logic, Design Tools and Methods - Porter College Dining Hall (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

[id] title	presenter	board
[17] Design and Implementation of Custom DMA Controller for the ALICE CRU, to Optimize Data Transfer Reducing the CPU Utilization	IMREK, Jozsef	A2
[68] The New Version of the LHCb SOL40_SCA Core to Drive Front-End GBT-SCAs for the LHCb Upgrade	VIANA BARBOSA, Joao Vitor	A4
[87] Studies on the Readout of the ATLAS Inner Tracker Using Commercial Networking Hardware	DÜLSEN, Carsten	A5
[96] The FEROL40, a MicroTCA Card Interfacing Custom Point-To-Point Links and Standard TCP/IP.	GIGI, Dominique	A6
[145] Upgrade of the YARR DAQ System for the ATLAS Phase-II Pixel Detector Readout Chip	WHALLON, Nikola Lazar	A7
[164] FED Firmware Interface Testing with Pixel Phase 1 Emulator	KILPATRICK, Matthew	A8

POSTER Session: 2 - Radiation Tolerant Components and Systems - Porter College Dining Hall (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

[id] title	presenter	board
[20] Irradiation Test Results of the ALICE SAMPA ASIC	MAHMOOD, Sohail Musa	D1
[37] Concentration Card Prototype SOLAR and Readout Electronics Principle for ALICE Muon Tracking Chambers Upgrade	GRABAS, Aude Marie	D2
[71] Rad-Hard Fibre Optics Cabling Design for LHC Detectors Upgrades	BLANC, Jeremy	D3
[106] The End-Of-Substructure Card for the ATLAS ITk Strip Tracker	GOETTLICHER, Peter	D4
[124] Development of a Monolithic Low Power, High Speed Pixel Sensor for Particle Tracking in High Energy Physics Experiments	Dr LAUXTERMANN, Stefan	D5
[147] A SEU-Immune Self-Tuned Pixel Chip Architecture	HEIM, Timon	D6
[163] General-Purpose Solution for Timepix3 – Katherine Readout	Dr BURIAN, Petr	D7
[189] Design and Radiation Tests on a LED Based Emergency Evacuation directional light	TRIKOUPIS, Nikolaos	D8

POSTER Session: 2 - Systems, Planning, Installation, Commissioning and Running Experience - Porter College Dining Hall (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

[id] title	presenter	board
[12] ATCA Thermal Management Study for the ATLAS Phase-II Upgrade	Dr BORTOLIN, Claudio	B1
[40] Development of Telescope Readout System Based on FELIX for Testbeam Experiments	WU, Weihao	B2
[45] Commissioning of ROD Boards for the Entire ATLAS Pixel Detector	Prof. GABRIELLI, Alessandro	B3
[49] Upgrade of the ATLAS Monitored Drift Tube Frontend Electronics for the HL-LHC	HU, Xueye	B4

[52] Simulation of the ATLAS New Small Wheel Trigger System	SAITO, Tomoyuki	B5
[76] Readout Electronics System of the CASCA Front-End Chip for the TPC Based X-Ray Polarimeter	Mr HENGSHUANG, Liu	B6
[84] ATLAS Phase-II-Upgrade Pixel Data Transmission Development	NIELSEN, Jason	B7
[92] The TrainBuilder Data Acquisition System for the European-XFEL	Dr COUGHLAN, John	B8
[111] Development of ATLAS Liquid Argon Calorimeter Readout Electronics for the HL-LHC	HORN, Philipp	C1
[114] Commissioning Experience and Upgrade Plans of the Pixel Luminosity Telescope for Luminosity Measurement at CMS	DELANNOY SOTOMAYOR, Andres Guillermo	C2
[116] Electronics and Firmware of the Belle II Silicon Vertex Detector Readout System	THALMEIER, Richard	C3
[121] Design of the New Front-End Electronics for the Readout of the Upgraded CMS Electromagnetic Calorimeter for the HL-LHC	GUILLOUX, Fabrice	C4
[122] Design Studies for the Off-Detector Electronics of the Upgraded CMS Electromagnetic Calorimeter for the HL-LHC	GOADHOUSE, Stephen	C5
[137] Data Acquisition Board for a Beam-Tagging Hodoscope Used in Hadrontherapy Monitoring	AMINA, ANNAGREBAH	C6
[142] Next Generation ATCA Control Infrastructure for the CMS Phase-2 Upgrades	SMITH, Wesley	C7
[154] KALYPSO: a 1D Detector for High-Repetition Rate Experiments at Light Sources	ROTA, Lorenzo	E2
[181] A Compact Tiled Readout for Hamamatsu H13700 PMTs with 256 Pixels	MOSTAFANEZHAD, Isar	E3
[184] Readout Electronics for the First Large HV-MAPS Chip for Mu3e	WIEDNER, Dirk	E4

POSTER Session: 2 - Trigger - Porter College Dining Hall (16:30 - 18:00)

-Conveners: Mitchell Franck Newcomer

[id] title	presenter	board
[5] A Multi-Level Triggering System for the Mini-EUSO UV Telescope	Mr FAUSTI, Federico	F2
[95] BDTs in the Level 1 Muon Endcap Trigger at CMS	LOW, Jia Fu	F3
[31] Hardware Trigger Processor for the ATLAS MDT System	COSTA DE PAIVA, Thiago	F3
[24] Development of the New Trigger Processor Board for the ATLAS Level-1 Endcap Muon Trigger for Run-3	MIZUKAMI, Atsushi	F4
[29] The Development of the Global Feature eXtractor (gFEX) for the ATLAS Level 1 Calorimeter Trigger at the LHC	TANG, Shaochun	F5
[64] Data Analysis at Level-1 Trigger Level	Mr WITTMANN, Johannes	F6
[9] ALICE Trigger System for LHC Run 3	KRIVDA, Marian	F7
[47] Simulations of Busy Probabilities in the ALPIDE Chip and the Upgraded ALICE ITS Detector	NESBO, Simon Voigt	F8
[104] Functionality and Performance of the ALFA_CTPIN Module	IWANSKI, Wieslaw	F9
[183] The NaNet Project: Heterogeneous Real-Time Stream Processing in the Low Level Trigger of the NA62 Experiment	LONARDO, Alessandro	F10