TWEPP 2017 Topical Workshop on Electronics for Particle Physics

Tuesday, 12 September 2017

Programmable Logic, Design Tools and Methods - Earth and Marine Sciences (E&MS) building (08:30 - 09:45)

-Conveners: Magnus Hansen

time	[id] title	presenter
08:30	[117] SEE Tolerant Standard Cell Based Design While Guaranteeing Specific Distance Between Memory Elements	MIRYALA, Sandeep
08:50	[63] Clock and Trigger Distribution for ALICE Using the CRU FPGA Card	IMREK, Jozsef
09:10	[89] DRM2: the Readout Board for the ALICE TOF Upgrade	FALCHIERI, Davide

Thursday, 14 September 2017

Programmable Logic, Design Tools and Methods - Thimann I Lecture Hall (11:05 - 12:20)

-Conveners: Angelo Rivetti

time	[id] title	presenter
11:05	[176] FPGA Based Wireless Time Interval Measurement System with Picosecond Resolution	Mr SRINIVASAN, Balaji
11:25	[131] New Slow Control FPGA IP for GBT Based Systems and Status Update of the GBT-FPGA Project	MENDEZ, Julian Maxime
11:45	[146] Characterization and Verification Environment for the 65 nm Pixel Readout-Chip RD53A	VOGT, Marco