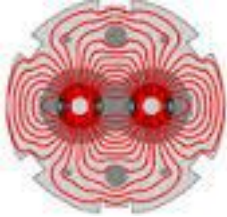
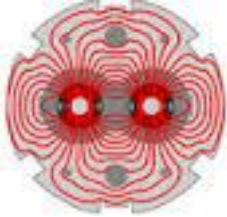


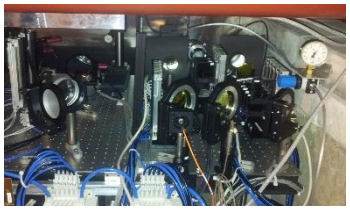
LHC Interlock BPM

BE-BI-QP

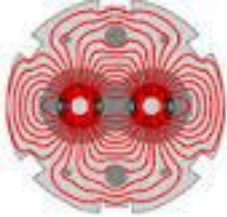
Outline



- Status of Interlock BPMs (IP6)
  - Performance & Limitations
  - Failure scenario
- New hardware system under design
  - Proposed architecture
  - Reviewing Specifications

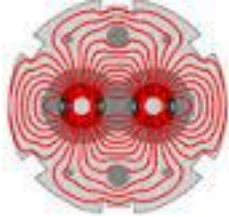


Status of Interlock BPMs



- Hardware modifications during LS1 to improve the dynamic range of the monitors
  - New 50Ω terminated strip-line pick-ups and low-pass absorptive filters (suppressing signal reflections)
- New Firmware / FESA3 / expert GUI to improve the diagnostics
  - Increased Post-mortem buffer memory with beam positions of all bunches during the 154 last turns
- Improved long-term stability with BPM acquisition electronic in water-cooled racks

Interlock BPMs
New dynamic ranges



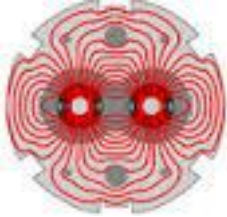
	Run 1	Run 2
High Sensitivity	1.5E9 – 3E10	1.5E9 - 1.3E11
Dynamic range improved by more than 10dB		
Low Sensitivity	*2E10 - >2E11*	*1.5E10 - >2E11*

This value is an Operational choice / compromise

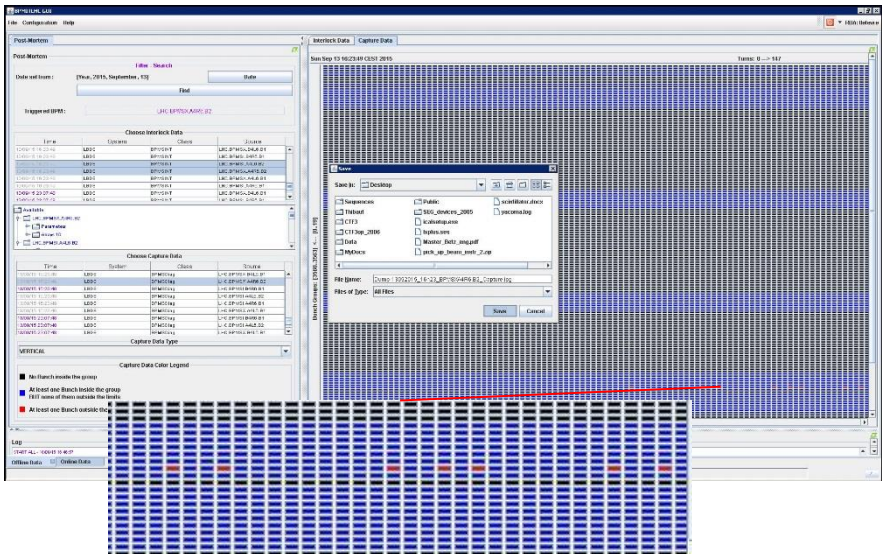
! System limited in sensitivity to 1.5E9 charge !

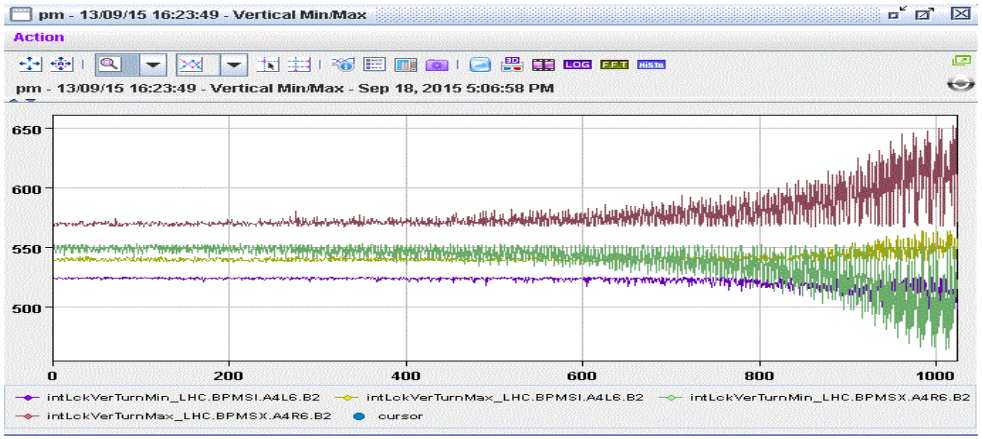
Interlock BPMs

Post-mortem data

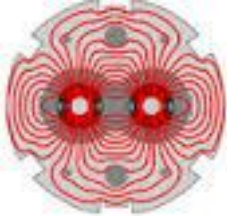


- Storing the last 154 turns of all bunches (limited by on-board memory)
  - Can be used to see which bunches become unstable
- Storing min/max positions for the last 1024 turns
  - Can be used to measure rise time of instability



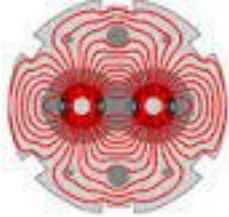


Interlock BPMs



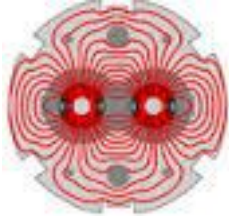
- Improving Sensitivity by adding an amplification stage at the input of the analogue circuitry
  - Initiated by a request from LHC-heavy ions team
  - System designed, built, installed, removed, forgotten…(in 5weeks)
    - 24dB improved sensitivity - down to 1E8 charges
    - Implementation could be improved to still allow a full system redundancy if necessary…..probably not ?

Interlock BPMs



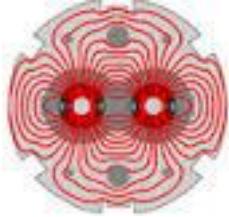
- Failure scenarios
  - If both FE power supplies died during a fill, the system do not see beam signals anymore but it is understood as if the beam was not present – no interlock fired
  - Mitigated by a software check/interlock

Interlock BPMS
Issues with Doublets (1/2)

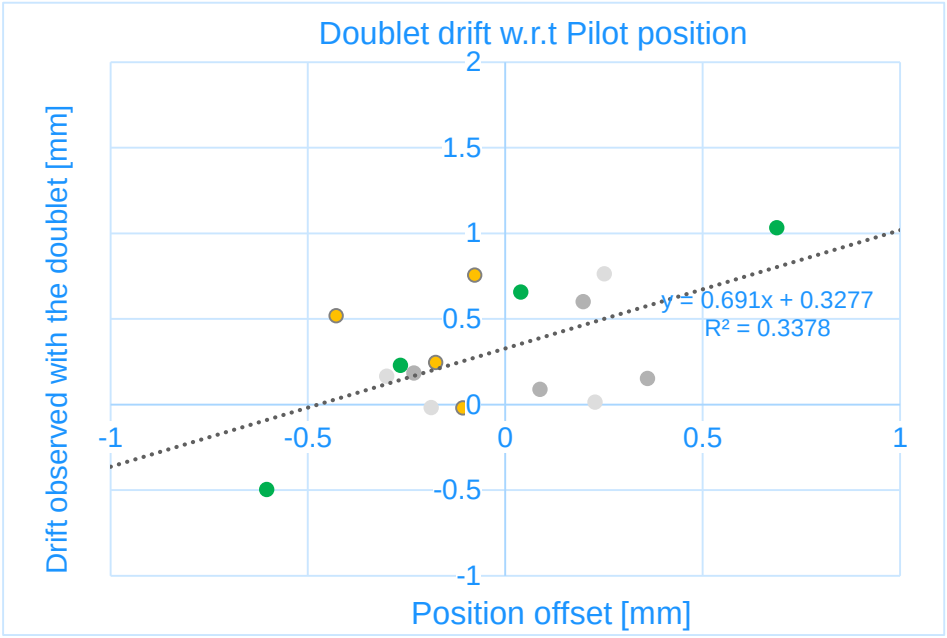


- BPM electronics not designed to work with bunch spacing shorter than 25ns (worst case for 5ns !)
  - Orbit data with doublet is distorted (RMS at 700um)

Interlock BPMS
Issues with Doublets (2/2)

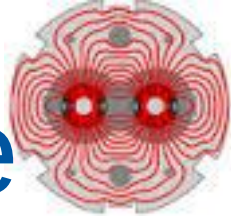


- BPM electronics not designed to work with bunch spacing shorter than 25ns (worst case for 5ns !)
  - B/B Offset and fluctuations up to 2 mm



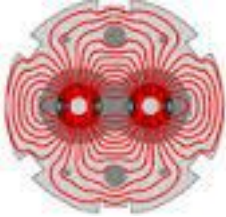
- No solution in the short term, apart from increasing the limit
  - Launched the development of a new B-b-B electronic read-out

LHC Interlock BPM challenge

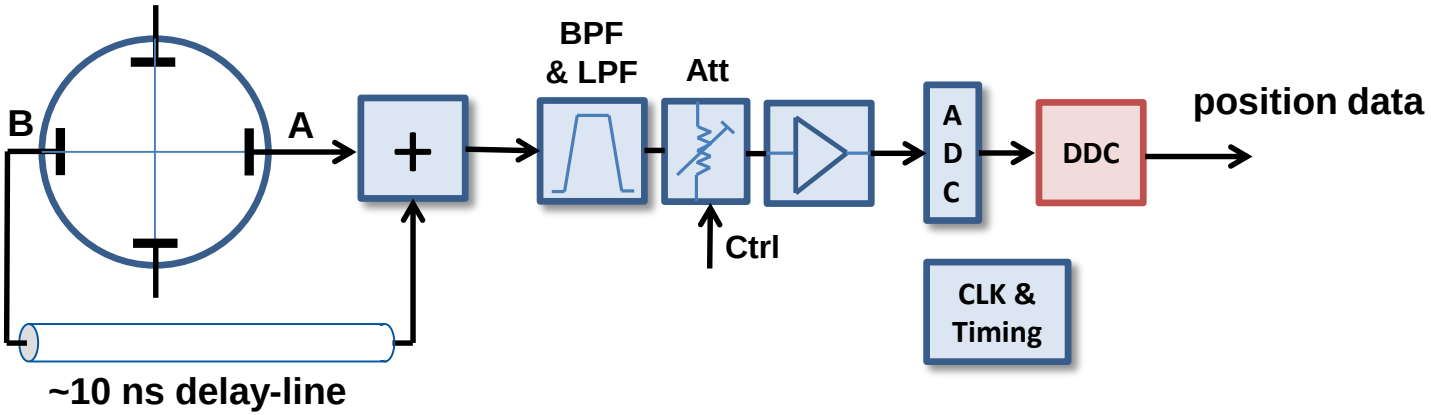


- High dynamic range
  - Typical 2e9 – 3e11
- Bunch-by-bunch observation
  - ”normal” bunch spacing 25 ns.
  - ”scrubbing” bunch doublets 5 ns.
- High reliability
  - Part of the technical interlock
  - No false beam dumps allowed
- Moderate requirements in terms of resolution, etc.
  - ~50 µm range

BPM Signal Processing Schema

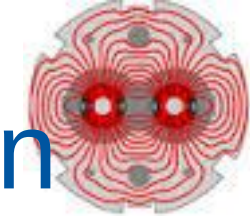


Time-multiplexed BPM electrode signal processing (based on DESY HERA-e principles)

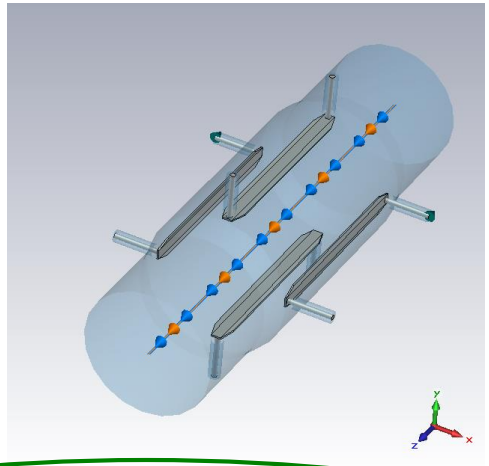


- Single channel, time-multiplexed BPM electrode signal conditioning and processing schema
  - Drifts, aging, LF noise, and many other unwanted effects cancel
  - ADC and DDC require min. 10 – 1200 MHz BW, min. 2.5 GSPS
    - Acquisition using 3.2GSPS, 12bit commercial mezzanine on BI custom VME board (VFC)
  - Dynamic range needs to cover SB intensity range, and sufficient beam position range, typically a total of 64 dB:
    - ~44 dB for the bunch intensity, e.g. 2e9 – 3e11
    - ~20 dB for the beam position, -12.7 – +12.7 mm (BPMSX: 0.79 dB/mm)

EM and Analog Circuit Simulation



Circuit simulation based on EM simulation pickup signals



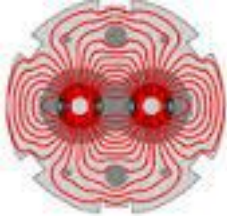
BPMSX
Wakefield solver
1e9 protons / bunch
σ = 50 mm
hor. beam offset = 1 mm

delay-line

beam pickup
with or w/o doublets
(70 % intensity)

4-stage analog FIR filter
(based on delay-lines)
1.2 GHz Butterworth LPF
(anti-aliasing)
550 MHz Bessel LPF
(cable dispersion)

DSP Simulation

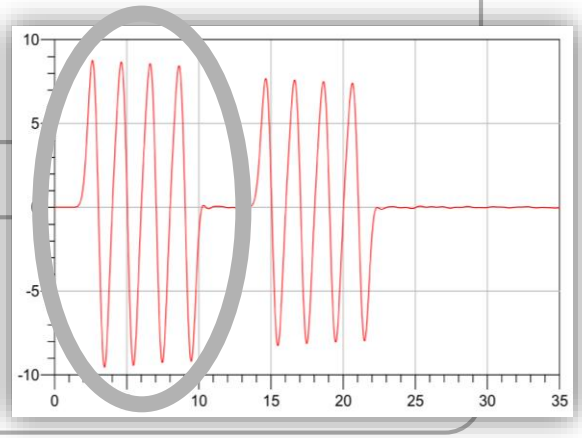


Signal Generation

- Based on output from simulation (100 GSa/s)
- Amplitude quantization
- Modifiable: amplitude, sampling phase, noise

Algorithm Under Test

- Single electrode, single bunch amplitude extraction
  - Square Averaging (AVG)
  - Frequency Domain Analysis (FDA)

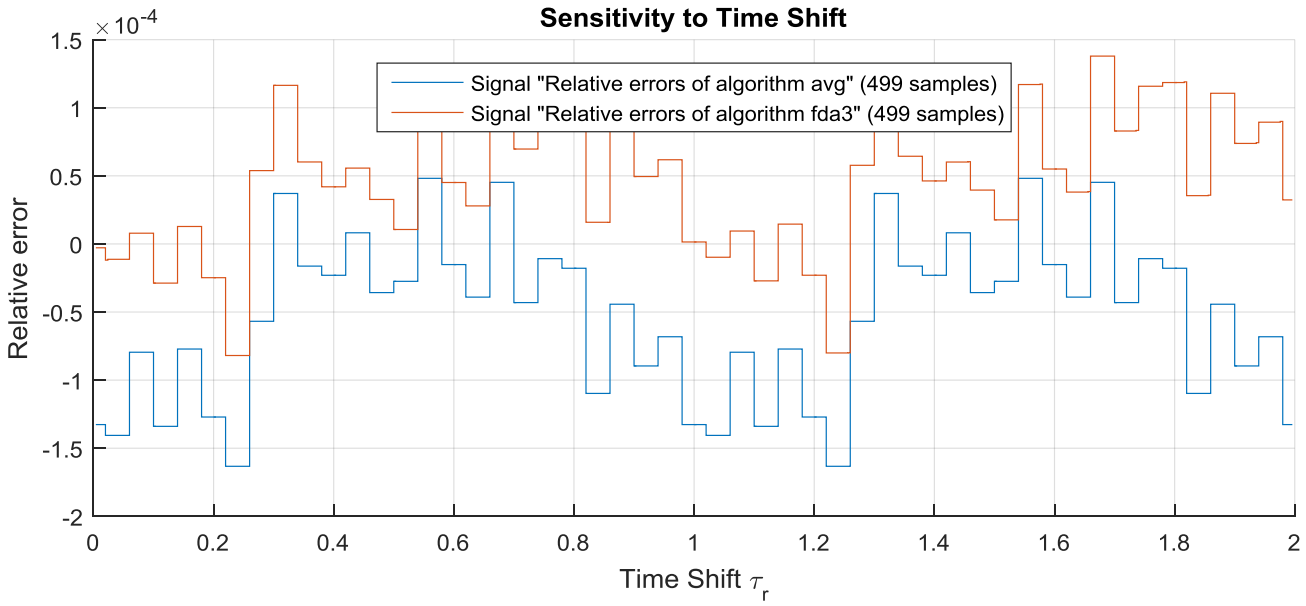


Results Evaluation

- Graph generation
- Results save

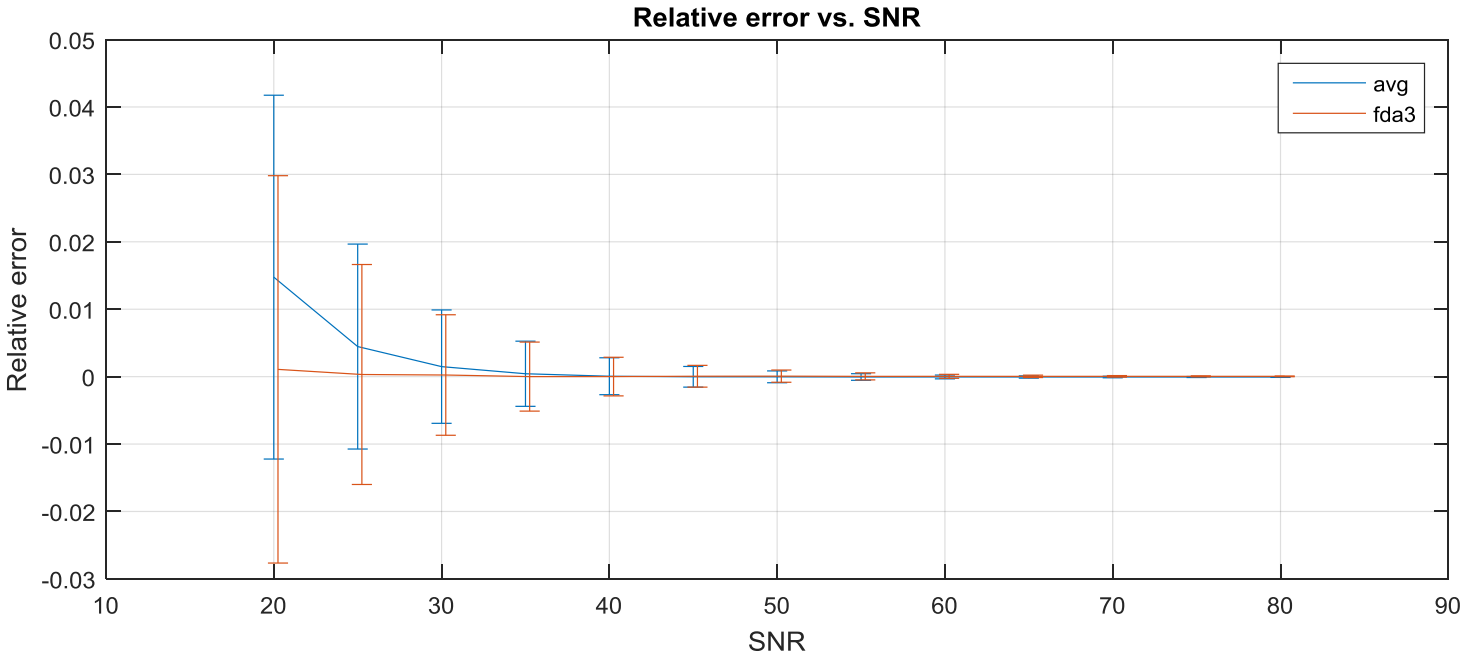
Sampling Phase Sensitivity

- 500 signals tested, full amplitude, no noise
- Sampling phase tested: 0-2 samples
- Nearly no sensitivity observed

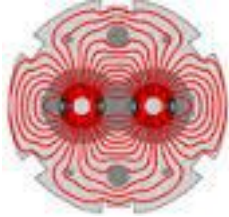


Noise Sensitivity

- 5000 signals tested, full amplitude, random sampling phase $\langle 0;2)$
- SNR tested: 13 values from 20 to 80 dB

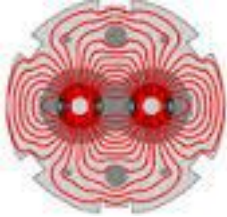


Design of a new acquisition system for Interlock BPMs



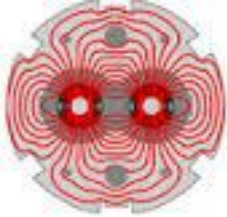
- Review specifications
  - System would provide both position and intensity of each bunches
    - Could we use bunch intensity to level the fault count ?
  - Energy dependent threshold ?
    - Allowing relaxed triggering conditions at injection energy
    - Drawback : System dependent on receiving external information from BST
  - Necessity for more beam diagnostics / XPOC / Postmortem buffer
    - There will be more memory available ….

Conclusions

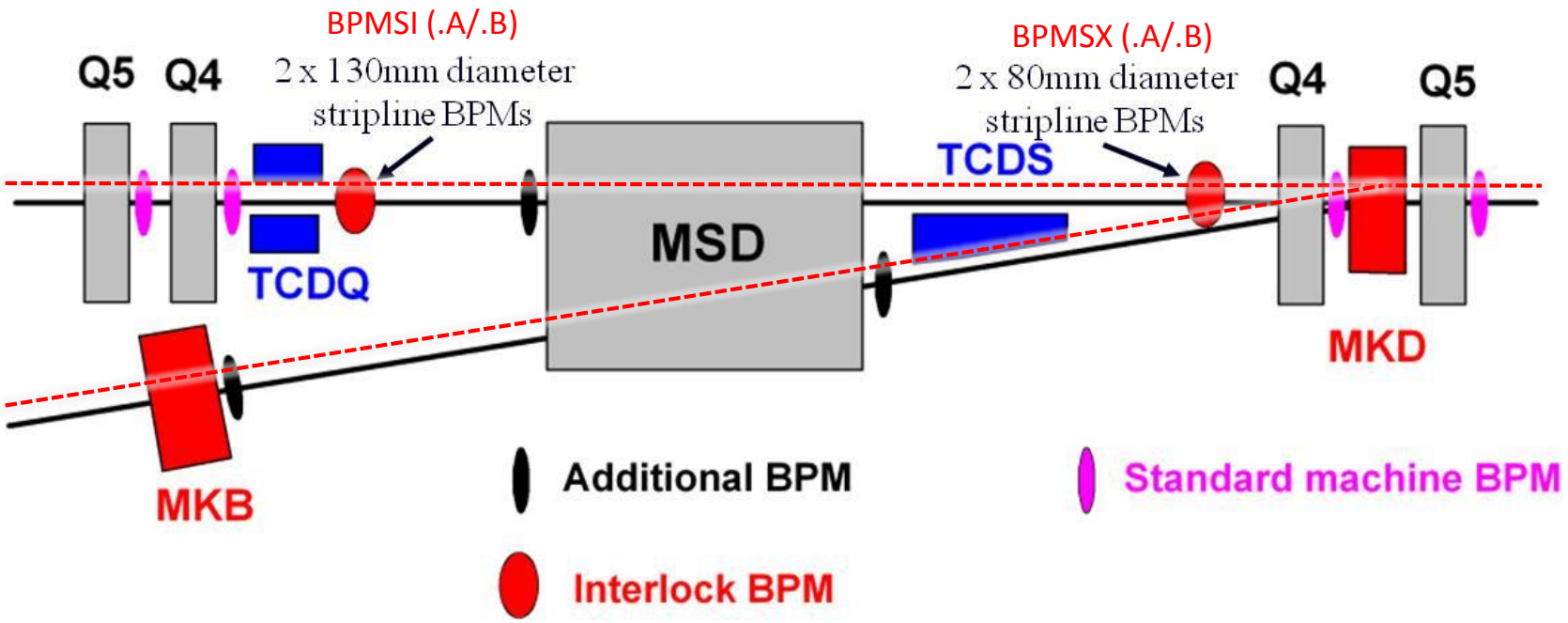


- Interlock BPMs have been working reliably in 2016
  - No modification foreseen during this EYETS17/18
- New system under development to cope with known limitations and adding new functionalities
  - Compatibility with doublet bunches operation
  - Information of Bunch intensity
  - Larger signal processing capability and larger memory
- Prototyping is advancing well
  - Good timing to review the specifications
  - Possible test with beam (SPS/LHC) during Summer/Fall 2017

Spare Slides

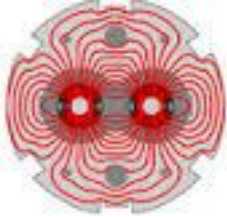


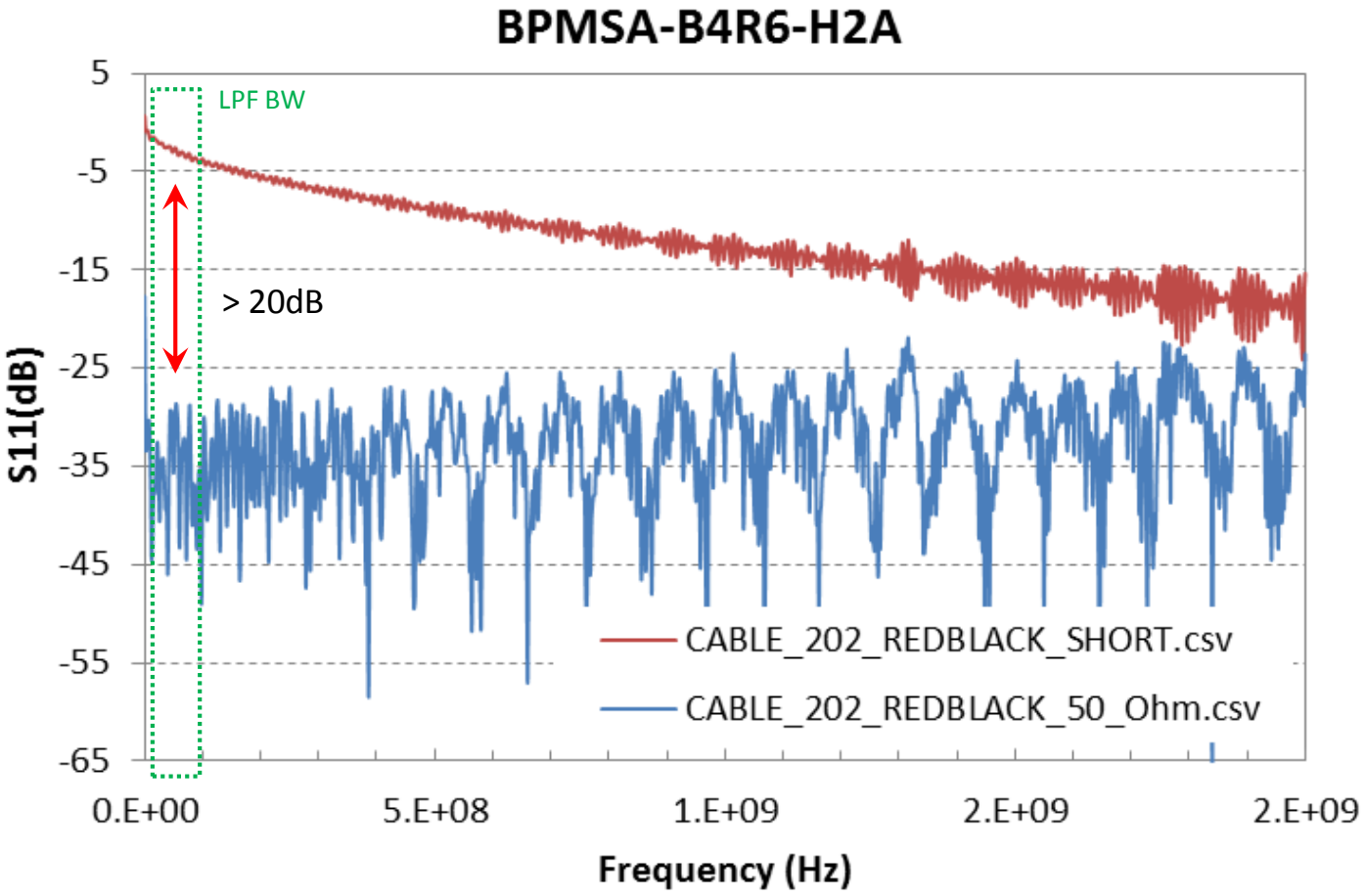
Dump Channel



The main aim of these BPMs is to avoid large orbit offsets leading to high losses on the septum protection during a dump

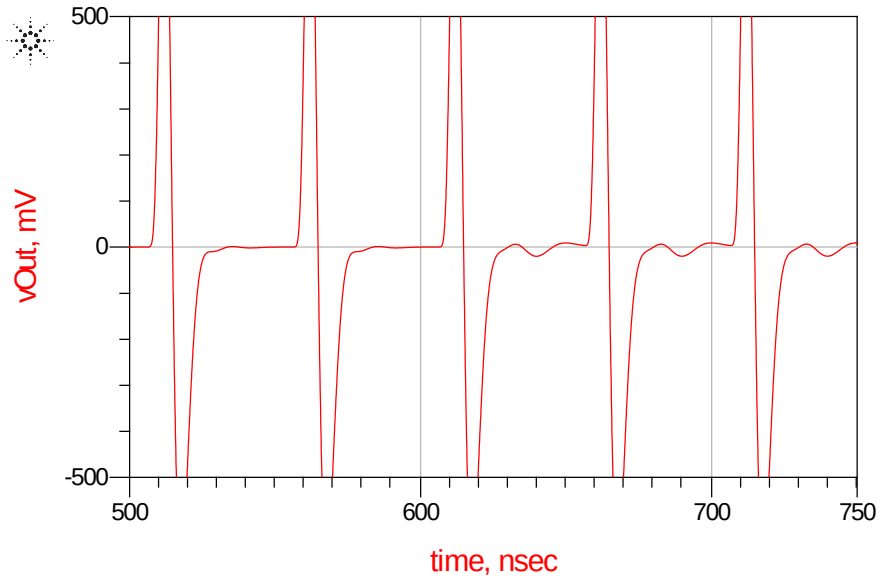
BPMs Reflections

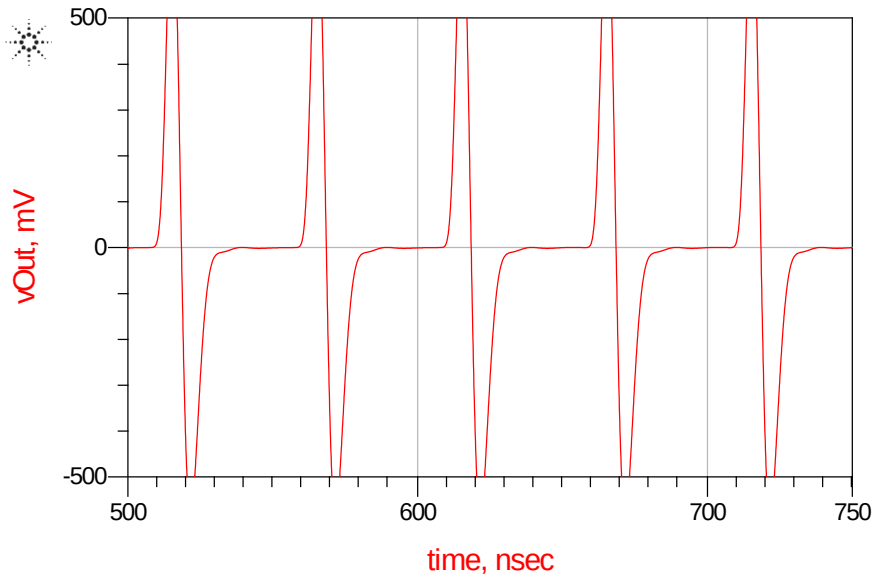




More than a factor 10 improvement on the Pick-up

Reflections in time domain



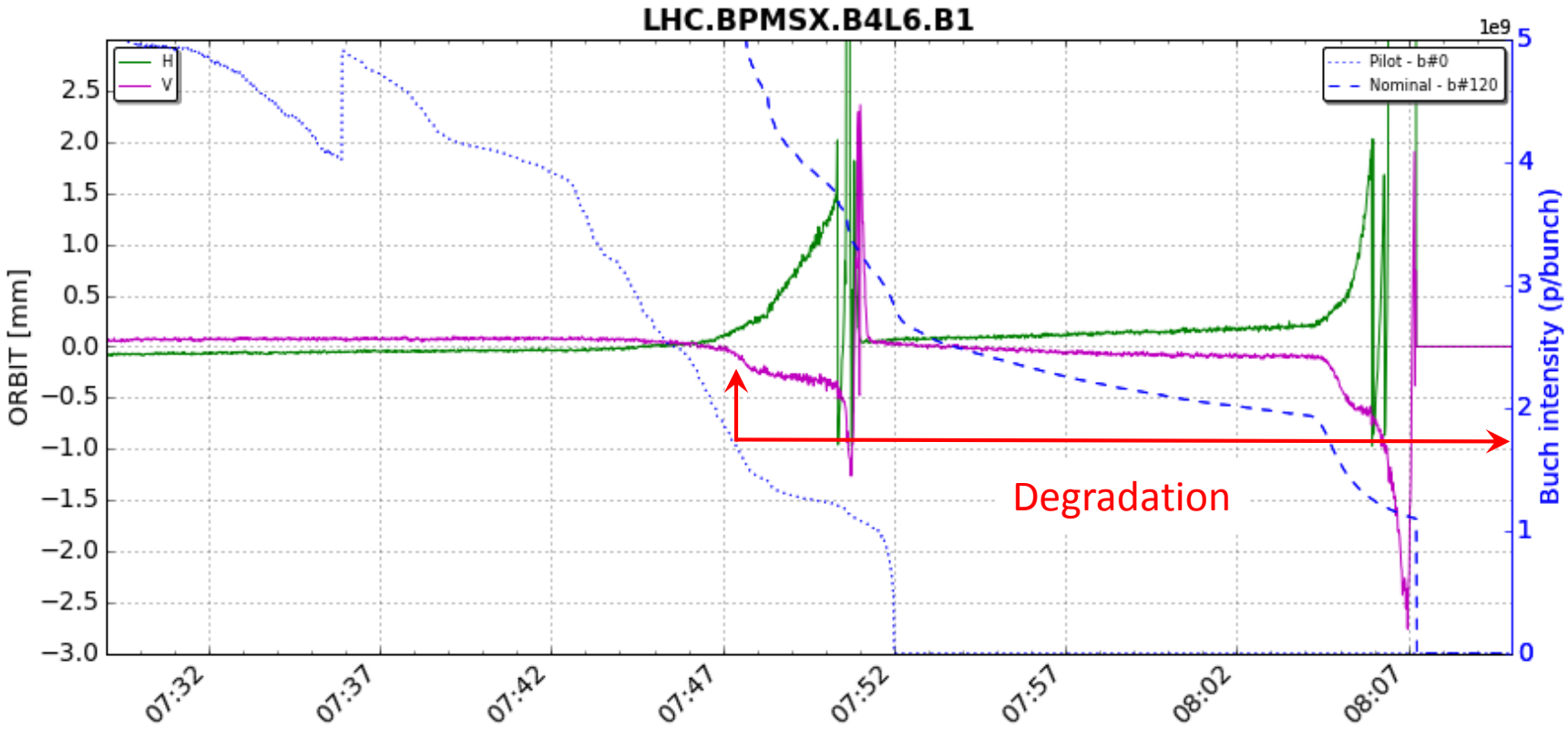


Shorted strip-lines reflections
Measurement: -27 dB
Simulation: -34 dB

Terminated strip-lines with LPF:
Simulations: <-46 dB

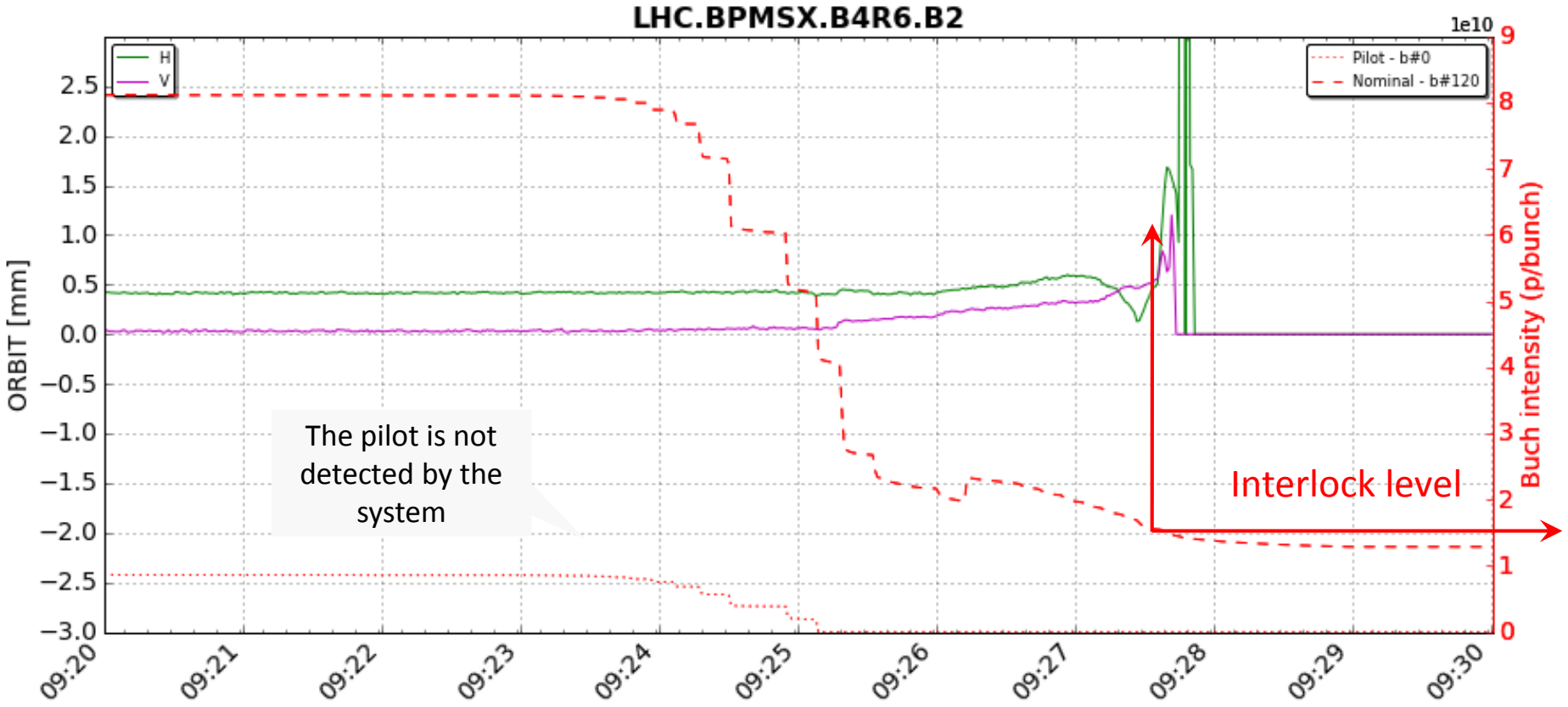
LHC IBPM Re-commissioning

Scrapping one Pilot and one Nominal in **High sensitivity** mode

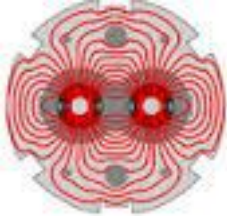


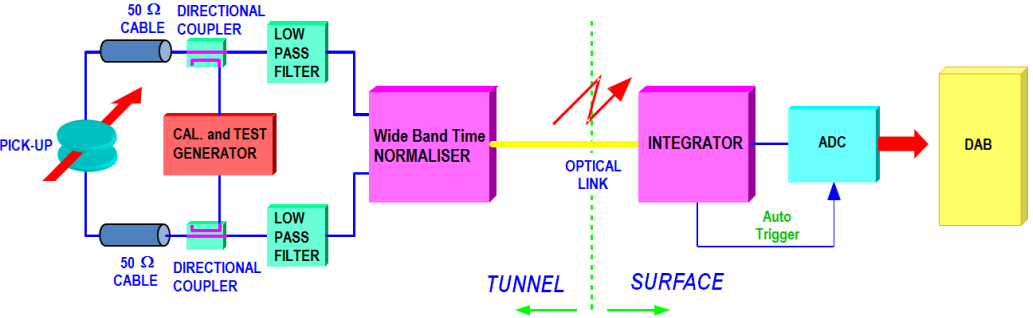
LHC IBPM Re-commissioning

Scrapping one Pilot and one nominal in **low sensitivity** mode

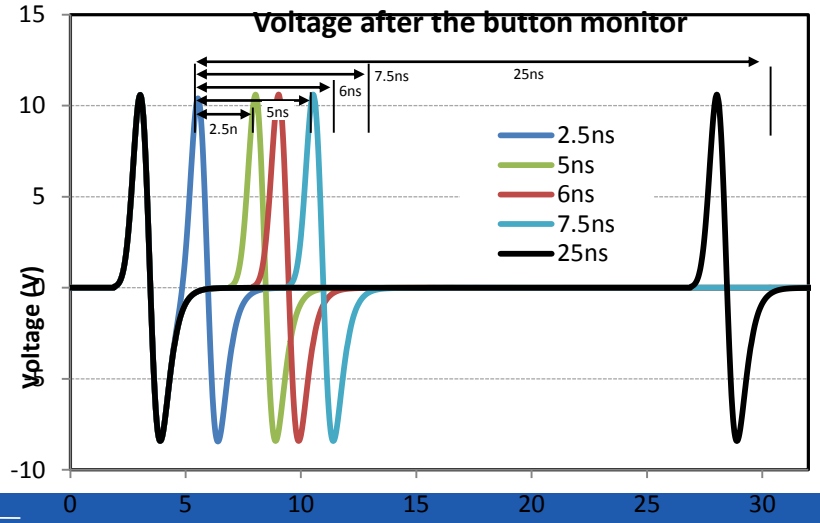


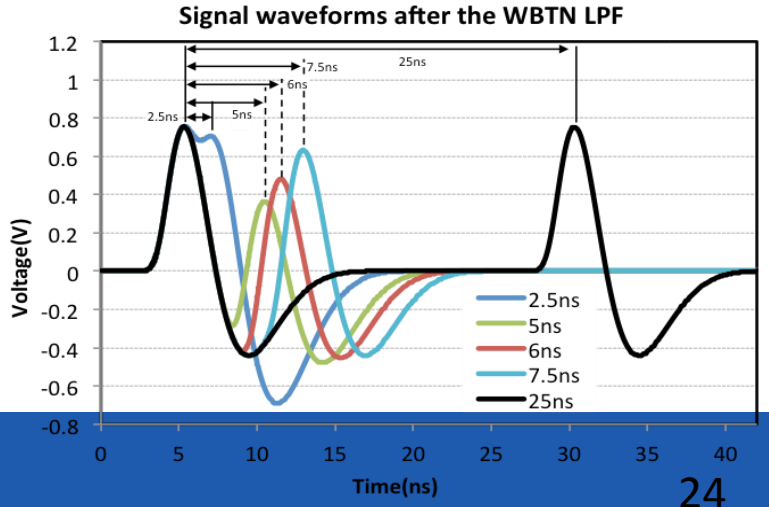
LHC BPM - WBTN



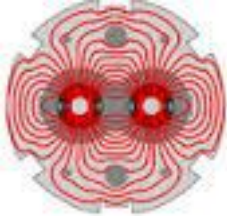


- Amplitude to Time conversion
- 70MHz LPF at the input of the electronic (bunch length independent)
- Depending on the bunch spacing , the signal will overlap in different ways.
- The system will provide a single measurement for bunches which are spaced by less than ~20ns.

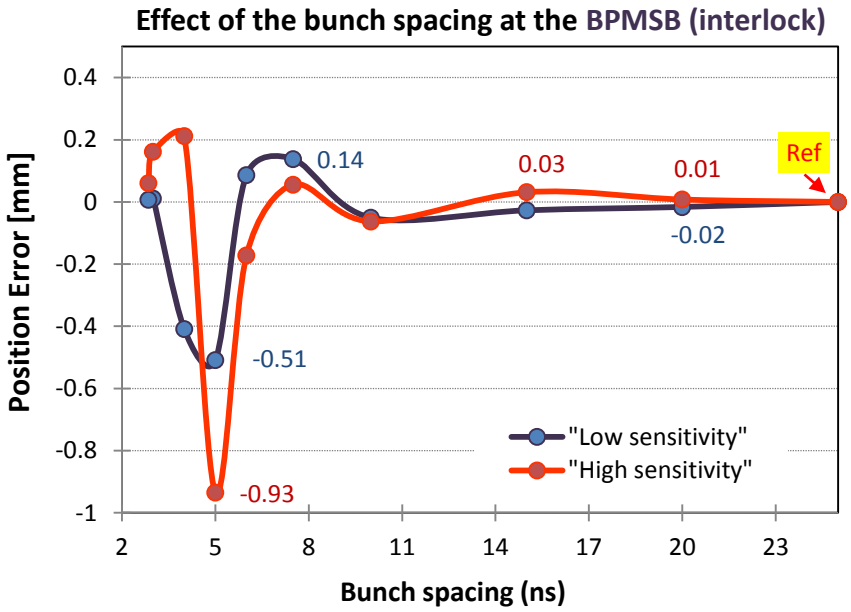


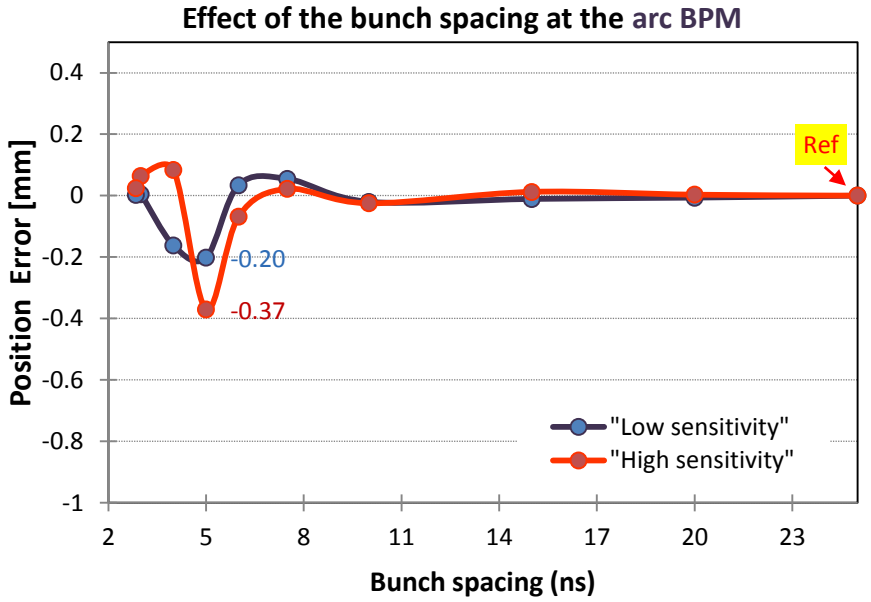


Scrubbing doublets



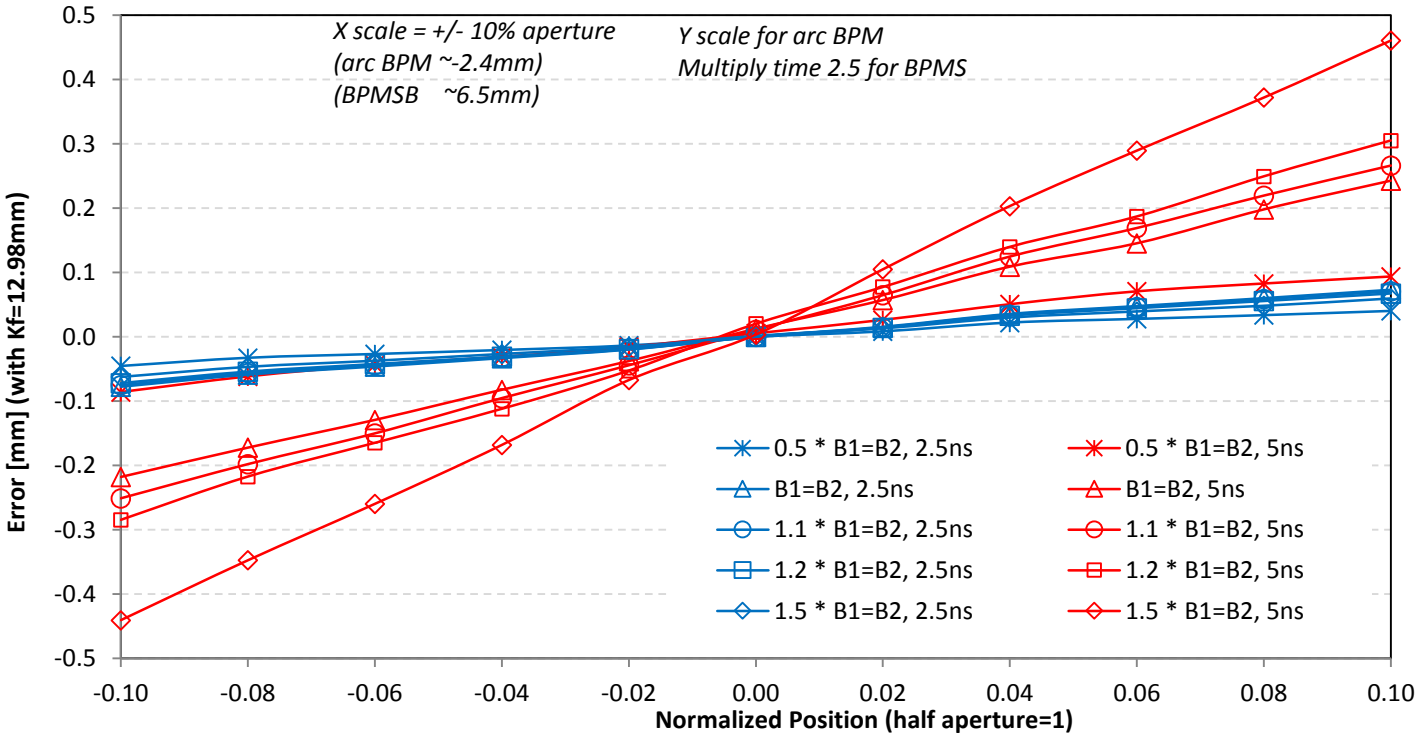
Beam “simulator” tests (beam signal replaced by pulse generator)
May be possible to test on SPS with beam



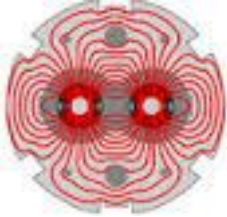


Doublets simulations 1

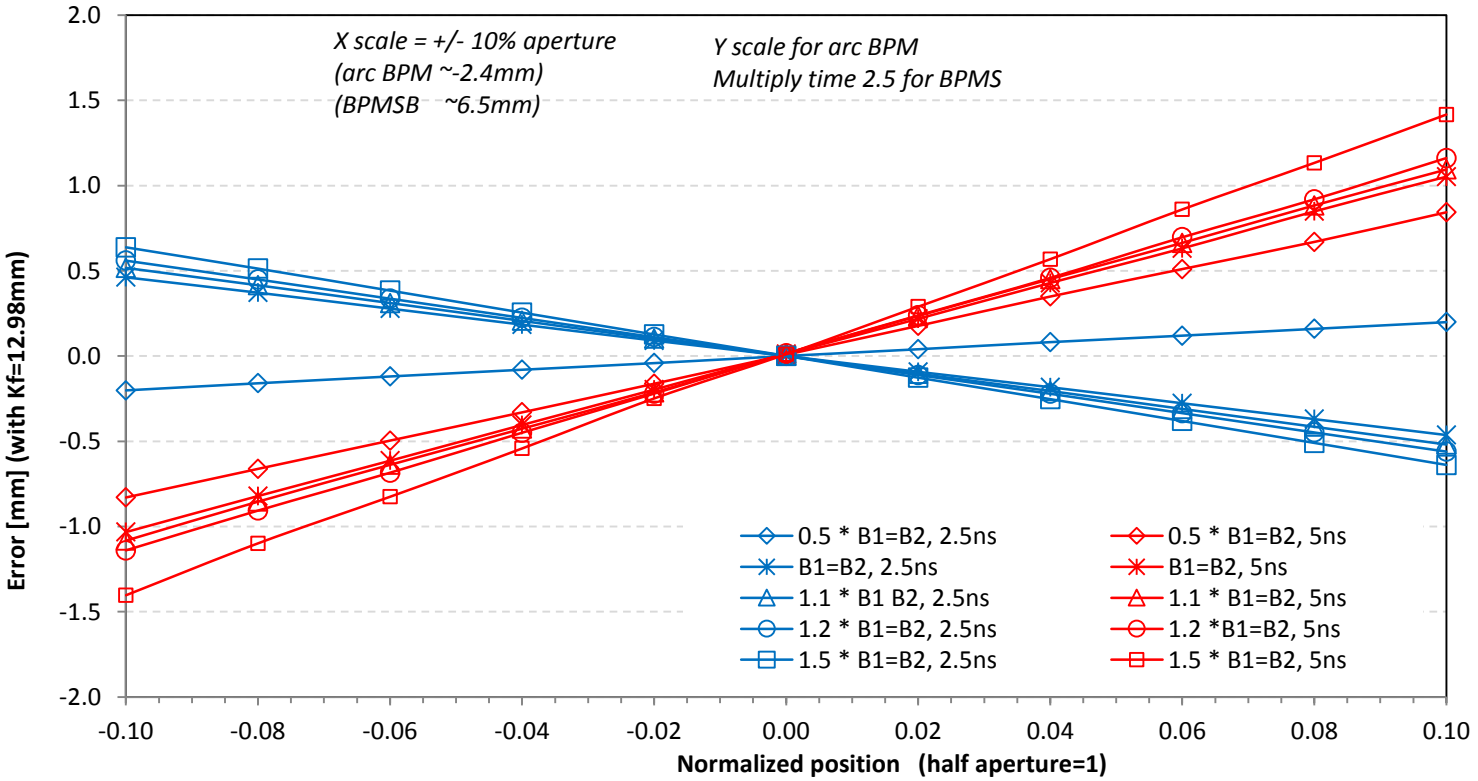
Bunch 1 and bunch 2 with same position



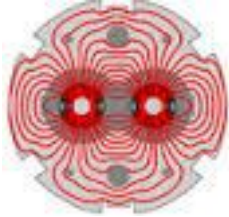
Doublets simulations 2



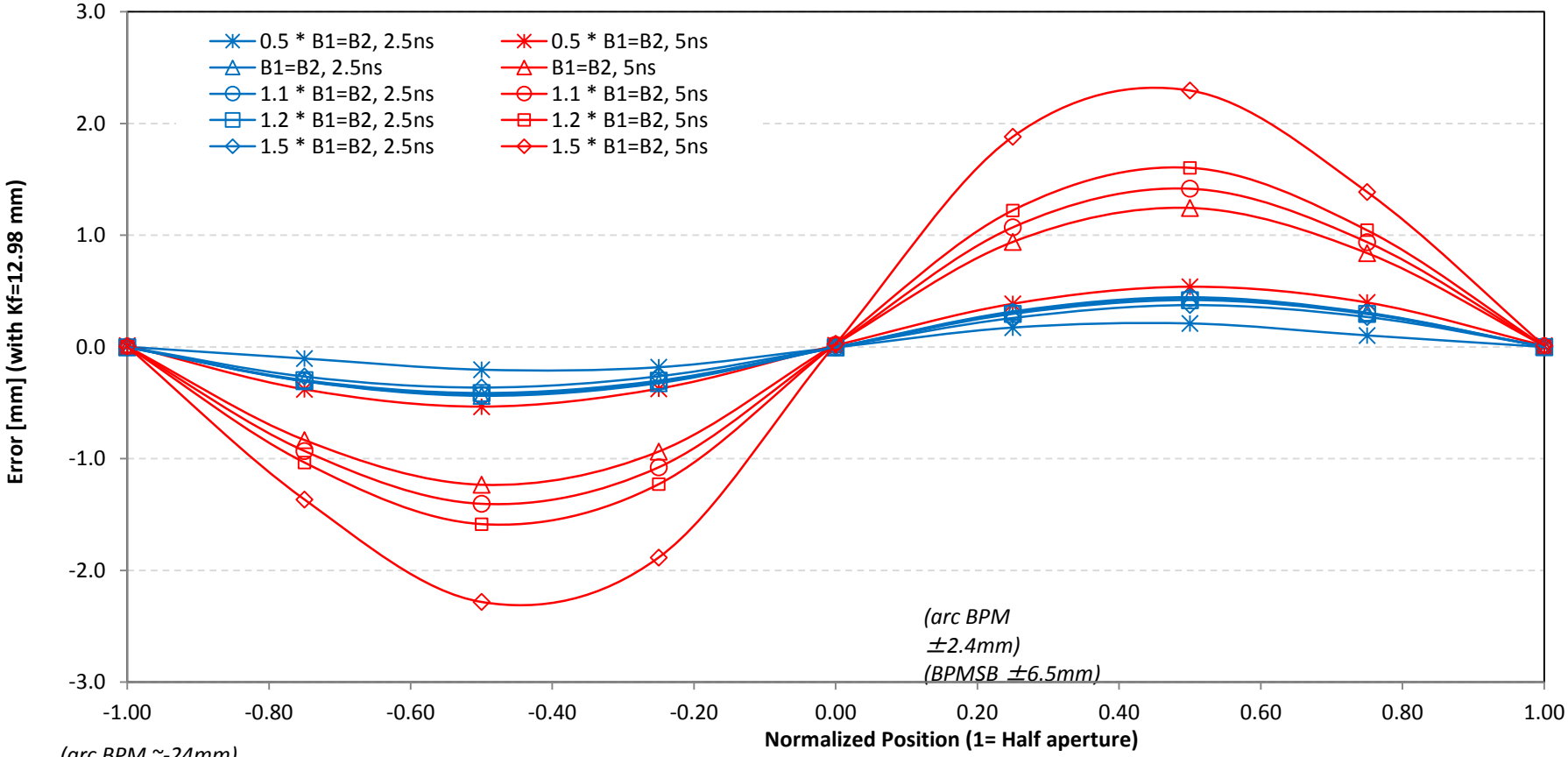
Bunch 2 always centred



Simulations with Pspice



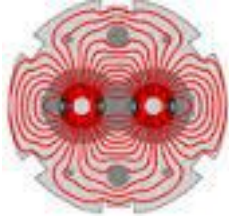
- **Bunch 1 and 2 can have different intensities : ‘(Un)Balanced Doublet’**
- Normalizer model circuit and signals are “ideal”
- Realistic Bunch length



(arc BPM ~-24mm)
(BPMSB ~65mm)

Note : Half Aperture of arc BPM = 24mm
Half Aperture of BPMSB = 65 mm

Simulation Results



single BPM electrode, single bunch

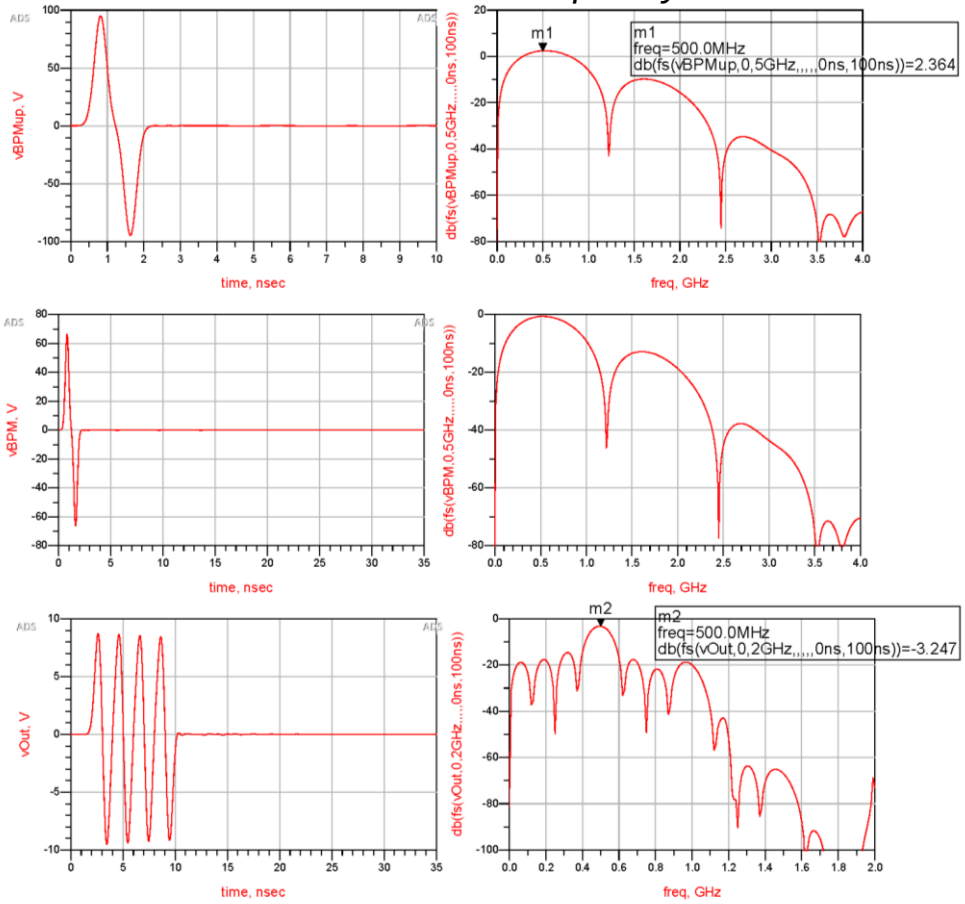
both BPM electrodes, single bunch

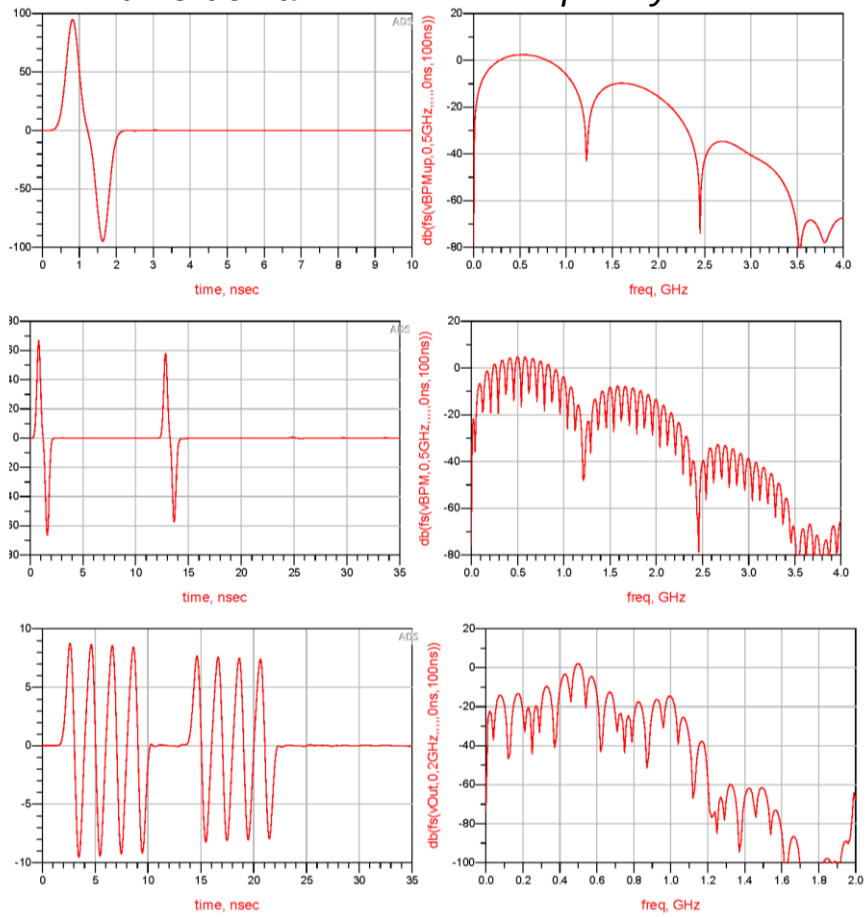
time-domain

frequency-domain

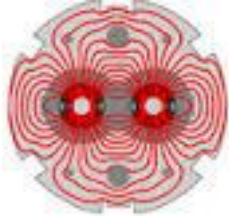
time-domain

frequency-domain



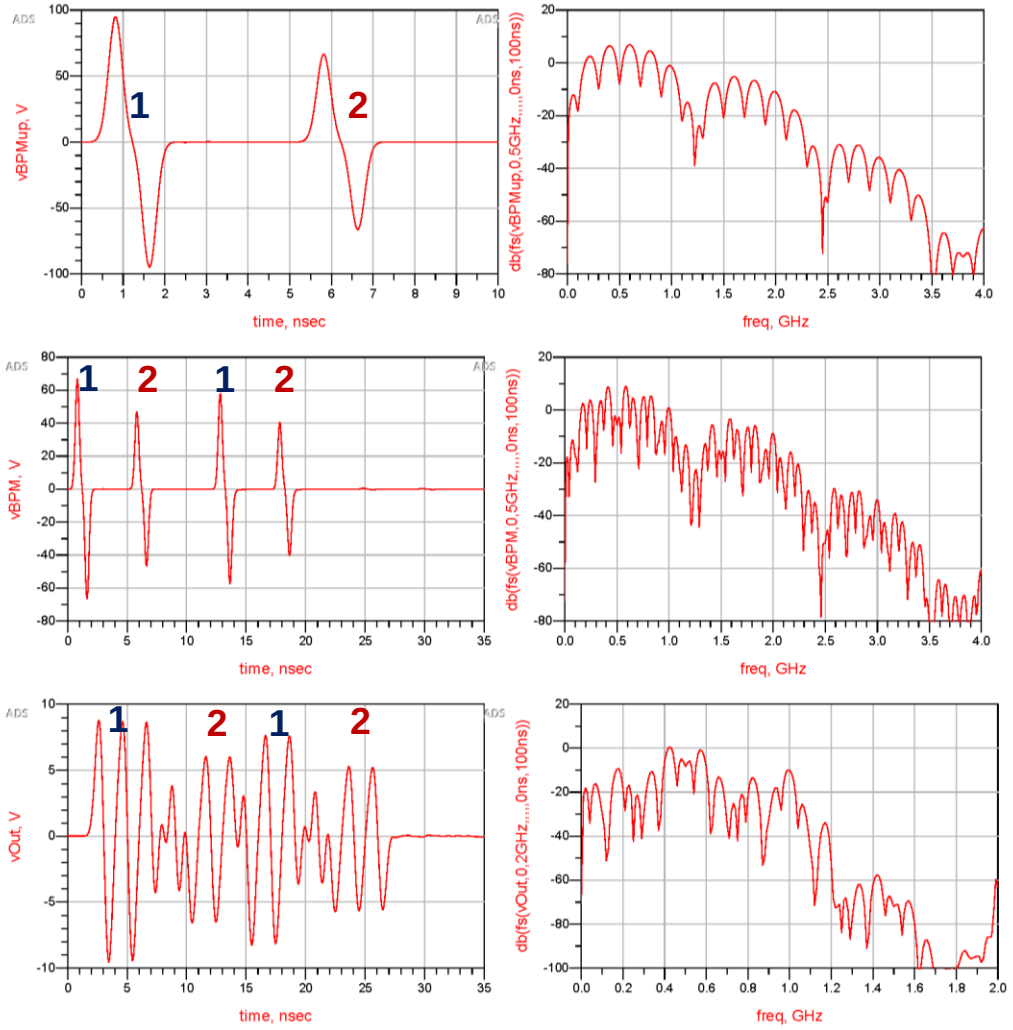


Simulation Results, cont.



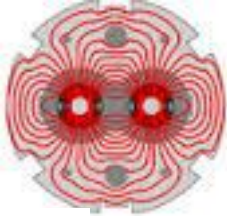
both BPM electrodes, doublet bunch 1 & 2

time-domain *frequency-domain*



- Simulation hints feasibility, BUT:
  - 1.2 GHz analog BW
  - Minimize reflection effects in the analog sections
    - Sufficient signal levels!
  - State-of-the-art ADC and digital section

12-bit, 4 GSPS ADC



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TEXAS INSTRUMENTS

ADC12J4000

SLAS989C – JANUARY 2014 – REVISED JULY 2015

ADC12J4000 12-Bit 4 GSPS ADC With Integrated DDC

1 Features

- Excellent Noise and Linearity up to and beyond F_{IN} = 3 GHz
- Configurable DDC
- Decimation Factors from 4 to 32 (Complex Baseband Out)
- Usable Output Bandwidth of 800 MHz at 4x Decimation and 4000 MSPS
- Usable Output Bandwidth of 100 MHz at 32x Decimation and 4000 MSPS
- Bypass Mode for Full Nyquist Output Bandwidth
- Low Pin-Count JESD204B Subclass 1 Interface
- Automatically Optimized Output Lane Count
- Embedded Low Latency Signal Range Indication
- Low Power Consumption
- **Key Specifications**
  - Max Sampling Rate: 4000 MSPS
  - Min Sampling Rate: 1000 MSPS
  - DDC Output Word Size: 15-Bit Complex (30 bits total)
  - Bypass Output Word Size: 12-Bit Offset Binary
  - Noise Floor: −149 dBFS/Hz or −150.8 dBm/Hz
  - IMD3: −64 dBc (F_{IN} = 2140 MHz ± 30 MHz at −13 dBFS)
  - FPBW (−3 dB): 3.2 GHz
  - Peak NPR: 46 dB
  - Supply Voltages: 1.9 V and 1.2 V
  - Power Consumption
    - Bypass (4000 MSPS): 2 W
    - Decimate by 10 (4000 MSPS): 2 W
    - Power Down Mode: <50 mW

analog BW > 3 GHz

4 GSPS

2 Applications

- Wireless Infrastructure
- RF-Sampling Software Defined Radio
- Wideband Microwave Backhaul
- Military Communications
- SIGINT
- RADAR and LIDAR
- DOCSIS / Cable Infrastructure
- Test and Measurement

3 Description

The ADC12J4000 device is a wideband sampling and digital tuning device. Texas Instruments' giga-sample analog-to-digital converter (ADC) technology enables a large block of frequency spectrum to be sampled directly at RF. An integrated DDC (Digital Down Converter) provides digital filtering and down-conversion. The selected frequency block is made available on a JESD204B serial interface. Data is output as baseband 15-bit complex information for ease of downstream processing. Based on the digital down-converter (DDC) decimation and link output rate settings, this data is output on 1 to 5 lanes of the serial interface.

A DDC bypass mode allows the full rate 12-bit raw ADC data to also be output. This mode of operation requires 8 lanes of serial output.

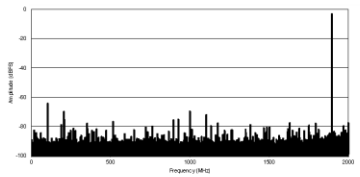
The ADC12J4000 device is available in a 68-pin VQFN package. The device operates over the Industrial (−40°C ≤ T_A ≤ 85°C) ambient temperature range.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC12J4000	VQFN (68)	10.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Bypass — Spectral Response
f_S = 4 GHz, F_{IN} = 1897 MHz



Electrical Characteristics (continued)

Unless otherwise noted, these specifications apply for $V_{(VA12)}$ = $V_{(VD12)}$ = 1.2 V, $V_{(VA19)}$ = 1.9 V, VIN full scale range at default setting (725 mV_{PP}), VIN = −1 dBFS, differential AC-coupled sinewave input clock, $f_{(DEVCLK)}$ = 4 GHz at 0.5 V_{PP} with 50% duty cycle, $R_{(RBIAS)}$ = 3.3 kΩ ±0.1%, after a foreground (FG) mode calibration with timing calibration enabled. Typical values are at T_A = 25°C.(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DDC BYPASS Mode							
SNR1	Signal-to-noise ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, −1 dBFS, 12-bit DDC bypass mode			55		dBFS
		F_{IN} = 600 MHz, −1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		54.8		
			T_A = T_{MIN} to T_{MAX}	52.5			
			T_A = 25°C, calibration = BG		53.9		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	49.4			
		F_{IN} = 1500 MHz, −1 dBFS, 12-bit DDC bypass mode			51.2		
		F_{IN} = 2400 MHz, −1 dBFS, 12-bit DDC bypass mode			48.7		
SNR2	Signal-to-noise ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs excluded	F_{IN} = 600 MHz, −1 dBFS, 12-bit DDC bypass mode	T_A = 25°C(3)		55		dBFS
			T_A = T_{MIN} to T_{MAX}(3)	53			
			T_A = 25°C, calibration = BG(3)		55		
			T_A = T_{MIN} to T_{MAX}, calibration = BG(3)	53			
SINAD1	Signal-to-noise and distortion ratio, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, −1 dBFS, 12-bit DDC bypass mode			54.8		dBFS
		F_{IN} = 600 MHz, −1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		54.7		
			T_A = T_{MIN} to T_{MAX}	52.3			
			T_A = 25°C, calibration = BG		53.8		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	49.2			
		F_{IN} = 1500 MHz, −1 dBFS, 12-bit DDC bypass mode			51.1		
		F_{IN} = 2400 MHz, −1 dBFS, 12-bit DDC bypass mode			48.7		
SINAD2	Signal-to-noise and distortion ratio, integrated across DDC output bandwidth Input frequency-dependent interleaving spurs excluded	F_{IN} = 600 MHz, −1 dBFS, 12-bit DDC bypass mode	T_A = 25°C(3)		54.9		dBFS
			T_A = T_{MIN} to T_{MAX}(3)	52.7			
			T_A = 25°C, calibration = BG(3)		54.9		
			T_A = T_{MIN} to T_{MAX}, calibration = BG(3)	52.7			
ENOB1	Effective number of bits, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, −1 dBFS, 12-bit DDC bypass mode			8.8		Bits
		F_{IN} = 600 MHz, −1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		8.8		
			T_A = T_{MIN} to T_{MAX}	8.4			
			T_A = 25°C, calibration = BG		8.7		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	7.9			
		F_{IN} = 1500 MHz, −1 dBFS, 12-bit DDC bypass mode			8.2		
		F_{IN} = 2400 MHz, −1 dBFS, 12-bit DDC bypass mode			7.8		
ENOB2	Effective number of bits, integrated across entire Nyquist bandwidth Input frequency-dependent interleaving spurs excluded	F_{IN} = 600 MHz, −1 dBFS, 12-bit DDC bypass mode	T_A = 25°C(3)		8.8		Bits
			T_A = T_{MIN} to T_{MAX}(3)	8.5			
			T_A = 25°C, calibration = BG(3)		8.8		
			T_A = T_{MIN} to T_{MAX}, calibration = BG(3)	8.5			
SFDR1	Spurious-free dynamic range Input frequency-dependent interleaving spurs included	F_{IN} = 350 MHz, −1 dBFS, 12-bit DDC bypass mode			67.4		dBFS
		F_{IN} = 600 MHz, −1 dBFS, 12-bit DDC bypass mode	T_A = 25°C		70.7		
			T_A = T_{MIN} to T_{MAX}	60			
			T_A = 25°C, calibration = BG		69.4		
			T_A = T_{MIN} to T_{MAX}, calibration = BG	51.8			
		F_{IN} = 1500 MHz, −1 dBFS, 12-bit DDC bypass mode			59.8		
		F_{IN} = 2400 MHz, −1 dBFS, 12-bit DDC bypass mode			57.2		
SFDR2	Spurious-free dynamic range Input frequency-dependent interleaving spurs excluded	F_{IN} = 600 MHz, −1 dBFS, 12-bit DDC bypass mode	T_A = 25°C(3)		73		dBFS
			T_A = T_{MIN} to T_{MAX}(3)	61.6			
			T_A = 25°C, calibration = BG(3)		74		
			T_A = T_{MIN} to T_{MAX}, calibration = BG(3)	62.8			

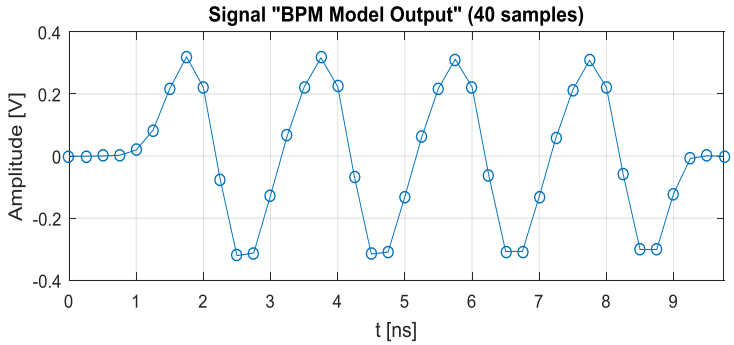
60 dB @ 1.5 GHz

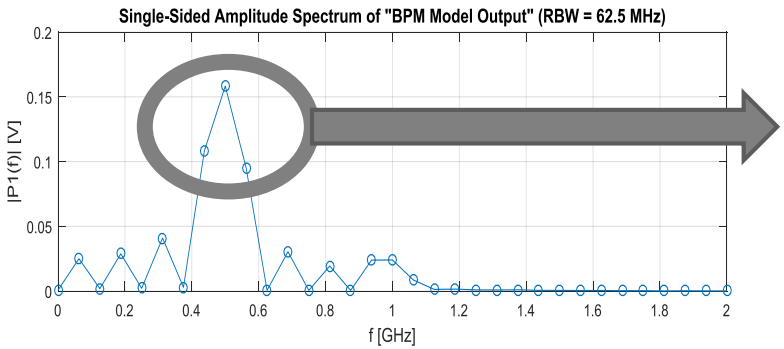
(3) Interleave related spurs at f_S / 2 – F_{IN}, f_S / 4 + F_{IN} and f_S / 4 – F_{IN} are excluded from these performance calculations. The magnitude of these spurs is provided separately.

CERN

DSP Algorithms Being Studied

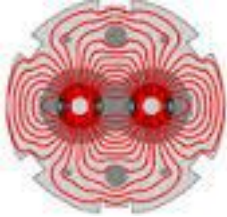
- Square Averaging
  - $A = M \cdot \sqrt{\frac{1}{40}\sum_{i=1}^{40} s_i^2}$ M – scaling factor
  - Weighted average / integration
  - Samples squared
- Frequency Domain Analysis





Average of 3 points around carrier is calculated → amplitude of original signal

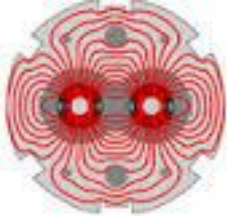
Monte Carlo Error Analysis



ADC full scale input voltage: 0.725 V

- 5000 signals tested:
  - Random amplitude $\langle 0.05; 0.6/2 \rangle$ V
  - $\sigma_{noise} = 725\ \mu\text{V}$
    - Noise of ADC according to measurements, roughly 4 bins
  - Random sampling phase $\langle 0; 2 \rangle$
- Error contribution breakdown – 3 more tests with
  - Just amplitude random
  - Just sampling phase random
  - Just noise

Relative Error



Test	AVG		FDA	
	μ	σ	μ	σ
MC Error Analysis	$0.7 \cdot 10^{-5}$	$16.48 \cdot 10^{-4}$	$4.5 \cdot 10^{-5}$	$17.04 \cdot 10^{-4}$
Amplitude random	$-7.6 \cdot 10^{-5}$	$1.12 \cdot 10^{-4}$	$4.7 \cdot 10^{-5}$	$1.19 \cdot 10^{-4}$
Time shift random	$-5.1 \cdot 10^{-5}$	$0.57 \cdot 10^{-4}$	$4.7 \cdot 10^{-5}$	$0.51 \cdot 10^{-4}$
Noise	$-13.4 \cdot 10^{-5}$	$6.61 \cdot 10^{-4}$	$0.6 \cdot 10^{-5}$	$6.95 \cdot 10^{-4}$