

eurorib'10

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Front end electronics and Data acquisition of Fazia detector.

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The development of the Fazia FEE design will be presented, concerning the main problems that have been attacked. In order to minimize noise and signal distortion the solution of the digitizer back-to-back the preamplifier inside the vacuum chamber has been adopted. With the digitizing ADCs (6 for each telescope composed of two Silicon detectors of 300 and 500 micron followed by a CsI) each FEE board will host FPGAs to perform online trapezoidal shaping and to handle the communication through optical fibers with a system of regional cards outside the scattering chamber. The online fast shaped signals are aimed at generating fast logic signals to produce a global trigger validation. The high-speed bidirectional optical fibers (≥ 3 Gbit/s) will transmit both data for the acquisition and logic information to a common general device. It will include a programmable trigger unit which, following the experiment demands, will generate and send back to all telescope of the apparatus a fast trigger validation. The data to be acquired, when separated, are sent through an ethernet network to a PC farm for storage and online analysis.

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