

DE LA RECHERCHE À L'INDUSTRIE



# READOUT ELECTRONICS FOR T2K-II TPCS:

## SETTING UP A WORKPLAN

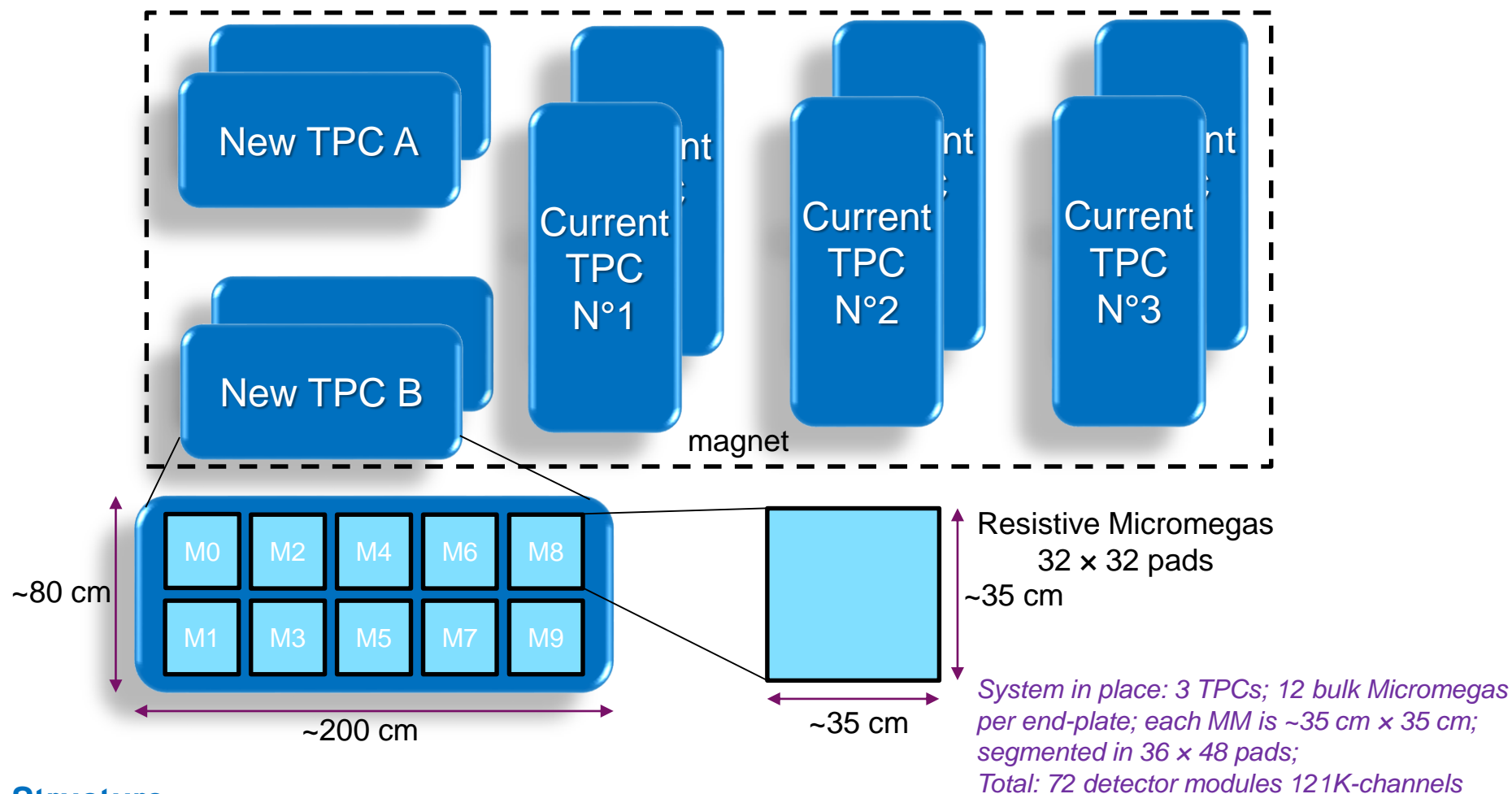
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# HYPOTHESIS ON TPCS TO BE BUILT



## Structure

- 2 TPCs, each composed of 2 end-plates supporting 10 Micromegas modules segmented in 32 x 32 pads
- Total of 40 detector modules; 40K-channels (40.960)

Front-end ASIC  
(design),  
production, test

Front-End Card  
design, production,  
test

Front-End Mezz.  
design, production,  
test

Front-End  
Mezz.  
firmware

Front-end ASIC  
Prod. test-bench

Front-end card  
Prod. test-bench

Front-end mezz.  
Prod. test-bench

*on-detector*  
-----  
*off-detector*

Back-end Board  
design, production,  
test

Embedded  
Firmware &  
Software

DAQ  
hardware  
& software

Power supplies  
Cabling, ...

Mechanics,  
Cooling

Detector  
test & calib.  
Test-bench

*Services and specific functions*

## Project structure

- Various building blocks; mostly electronic hardware and software, but also mechanical components
- Interface to detector, cooling, system, etc.



Quantity required for 40K ch.  
including 10% spares: 704  
Estimated cost: 0€ to 65 k€

## AFTER

- Designed and used in T2K. Current stock of tested and encapsulated chips: ~780 (53K-channel)
- Can produce more wafers, but package obsolete – no solution found for encapsulation so far.
- Pros: low risk, ready now, no manpower, no cost up to ~40K-ch. Cons: limited stock, end of life product

## AGET

- Also a proven chip. Current stock too low. Same problem of package obsolescence as AFTER
- Pros: fresher design than AFTER. Cons: 64 channels rather than 72; no stock; package issue

## DREAM

- Also a proven chip but not directly compatible with AFTER-AGET
- Pros: smaller size, packaging OK. Cons: 64 channels, need new production, less re-use from existing

## ASTRE

- Space grade version of AGET, also supports longer peaking time (up to 8  $\mu$ s)
- Pros: most versatile chip. Cons: features not needed in T2K. Package issue. Cost of masks for mass prod.

## New chip designed at lrfu

- Ideas of improvements: include the ADC on-board (seems too much work)
- Improve the characteristics under saturation: limit influence on adjacent channels (in discussion)  
(but is resistive Micromegas less prone to make the kind of saturations seen on present TPCs?)

## Other chip (either existing or planned)

- Suggestions?

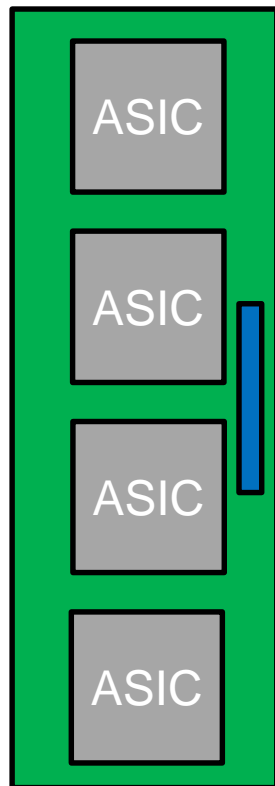
## Proposed strategy

- lrfu could take responsibility of this building block
- Study the possibility to make improvements on one of our existing chips
- Consider the use of AFTER/AGET/ASTRE/DREAM as it is
- Minimal scheme: AFTER from the existing stock (if it sufficient)

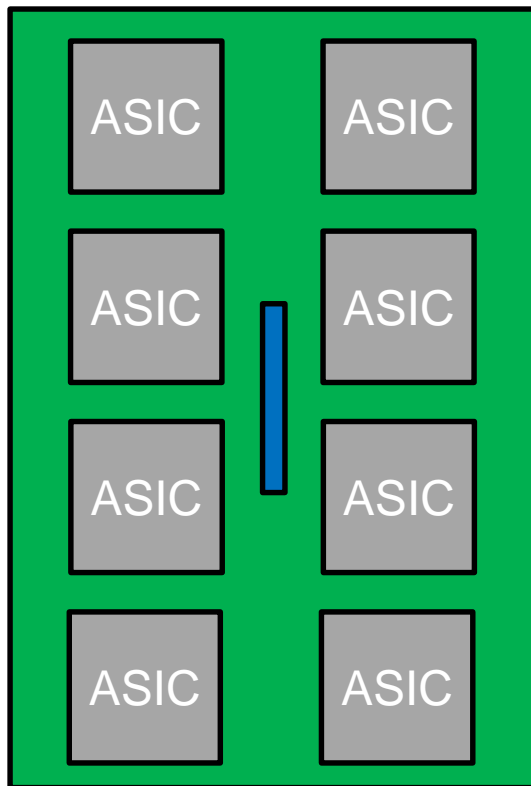
→ Final choice on the ASIC can probably be delayed to ~end 2018



288<sup>ii</sup>-channel FEC  
(AFTER) built in 2010  
for ILC-TPC R&D

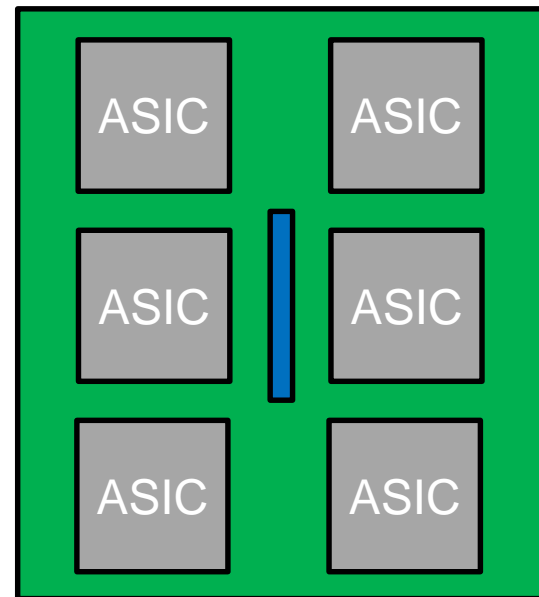


256<sup>i</sup>(288<sup>ii</sup>) -channel FEC



512<sup>i</sup>(576<sup>ii</sup>)-channel FEC

Quantity required for 40K ch.  
including 10% spares:  
176 assuming 4 ASIC's per card  
88 assuming 8 ASIC's per card  
Estimated cost: 88\*400=35 k€



384<sup>i</sup>(432<sup>ii</sup>)-channel FEC

## Design principles

- Minimal complexity – no protection circuits (resistive MM), no local FPGA, may be not even ADC (multiplexed analog out), only ASICs (packaged...), connectors, simple clock/control fan in/out, power
- If card small enough could be mounted parallel to detector, otherwise perpendicular (like current TPCs)

<sup>i</sup>: with 64-channel ASICs

<sup>ii</sup>: with 72-channel ASICs

## Proposed strategy

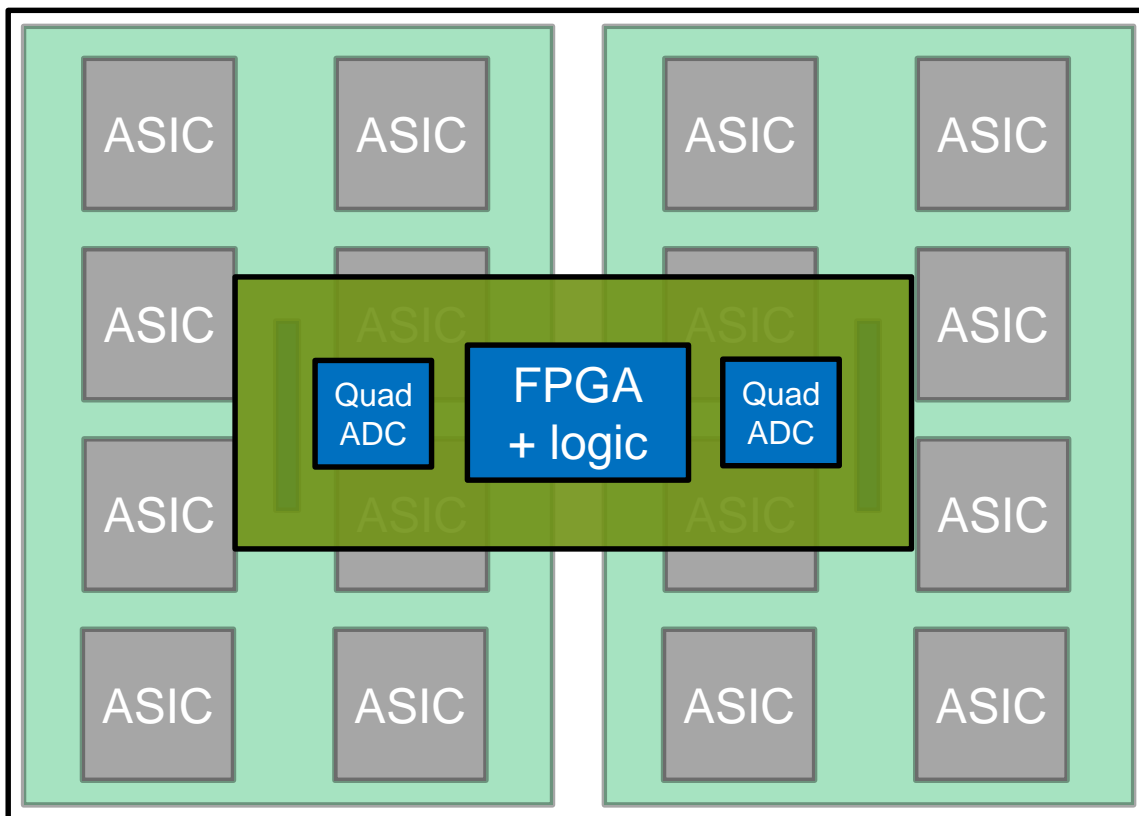
- Discuss and agree connector interface to detector
- Discuss and agree interface to front-end Mezzanine card (see next building block) – independent of ASIC, or capable of supporting several types (within the possible candidate chips)
- First prototyping can use existing chips until final device is chosen

## Work package outline

- Front-end card design, prototyping and validation
- Build easy-to-use test bench for card production
- Mass production and test
- Installation and commissioning

→ Possible interest of Lpne group for taking responsibility of this building block. Other candidates?

Quantity required for 40K ch.  
including 10% spares: 44  
Estimated cost:  $44 \times 600 = 27$  k€



## Design principles

- ADCs (if not on FECs) + local intelligence in FPGA + additional components; single fiber optical readout to back-end electronics for clocking, trigger, configuration, data and slow control
- Embedded firmware only, probably no need for embedded processor

## Proposed strategy

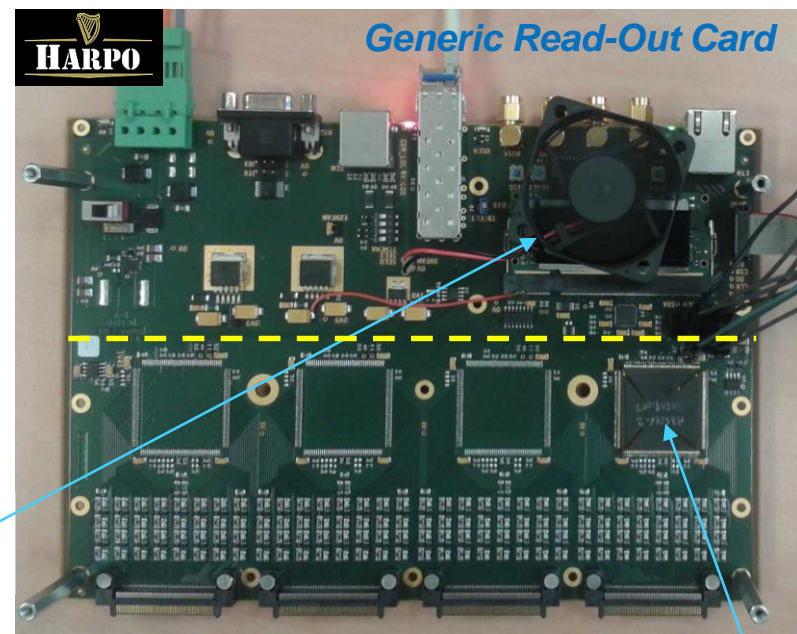
- Partial re-use (FPGA firmware, part of schematics, knowledge) and adaptation of the “**Generic Read-Out Card – GROC**” in development at Lrfu for the Harpo project
- Main tasks: drop the front-end side; rework logic (bigger FPGA) and firmware to drive 16 ASICs instead of 4, re-layout PCB

Commercial FPGA module  
Enclustra Mars MX3  
(Xilinx Artix 7 FPGA)

## Work package outline

- Front-end Mezzanine card design, prototyping and validation
- Develop embedded firmware
- Build easy-to-use test bench for card production
- Mass production and test
- Installation and commissioning

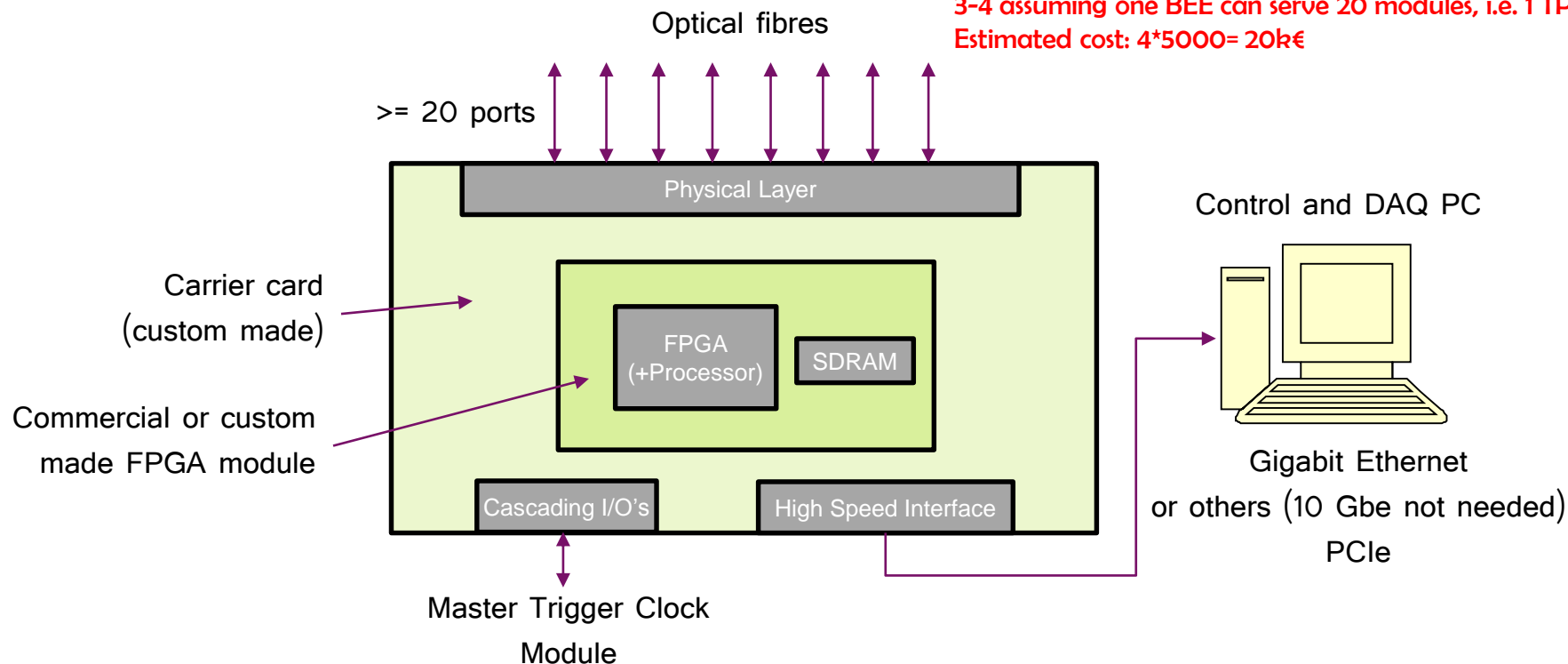
→ Interest of Lrfu for board design, firmware and production. Interest of Warsaw group for design of production test bench and board production



6U form factor 256-channel generic readout card  
(supports AFTER, AGET and ASTRE)

ASTRE  
chip

Quantity required for 40K ch. including spares:  
3-4 assuming one BEE can serve 20 modules, i.e. 1 TPC  
Estimated cost:  $4 \times 5000 = 20\text{k€}$



## Design principles

- Carrier card + System-On-Module (preferably commercial) + sufficient number of optical transceiver + Gigabit Ethernet interface to local control and DAQ PC + I/O's for clock and trigger
- FPGA firmware and on-board processor with embedded software – bare metal or Linux

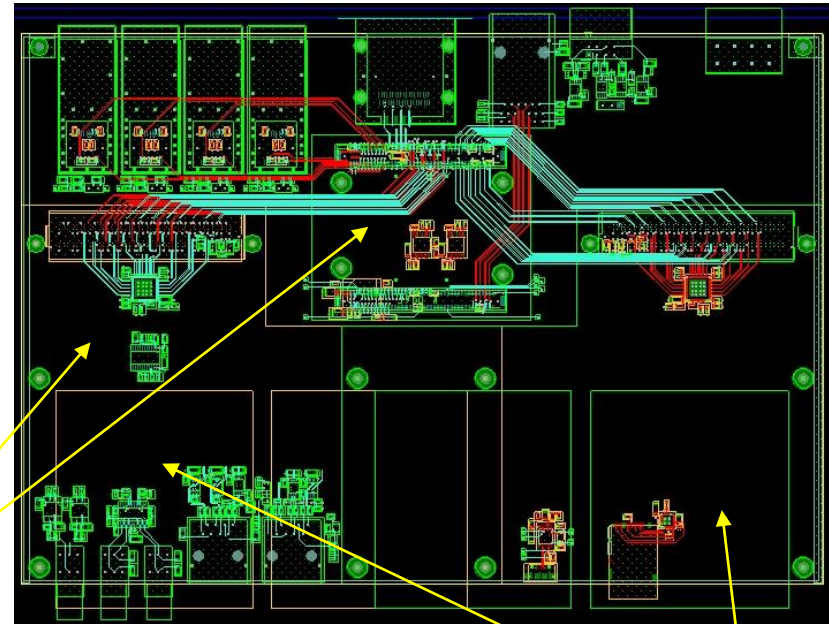
## Strategy

- Direct hardware re-use and large part of firmware/software re-use of the **“Trigger & Data Concentrator Module - TDCM”** under development at Lrfu for PandaX-III experiment
- The TDCM supports the control and readout of up to 32 front-ends (e.g. G-ROC)



6U form factor custom carrier  
(layout in progress)

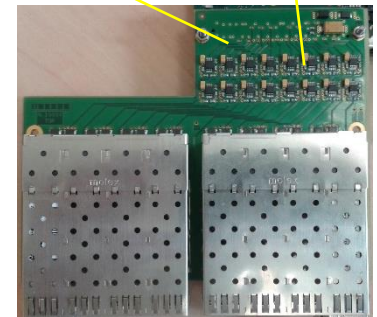
Commercial System-On-Module  
Mercury ZX1 (Xilinx Zynq 7045)



## Work package outline

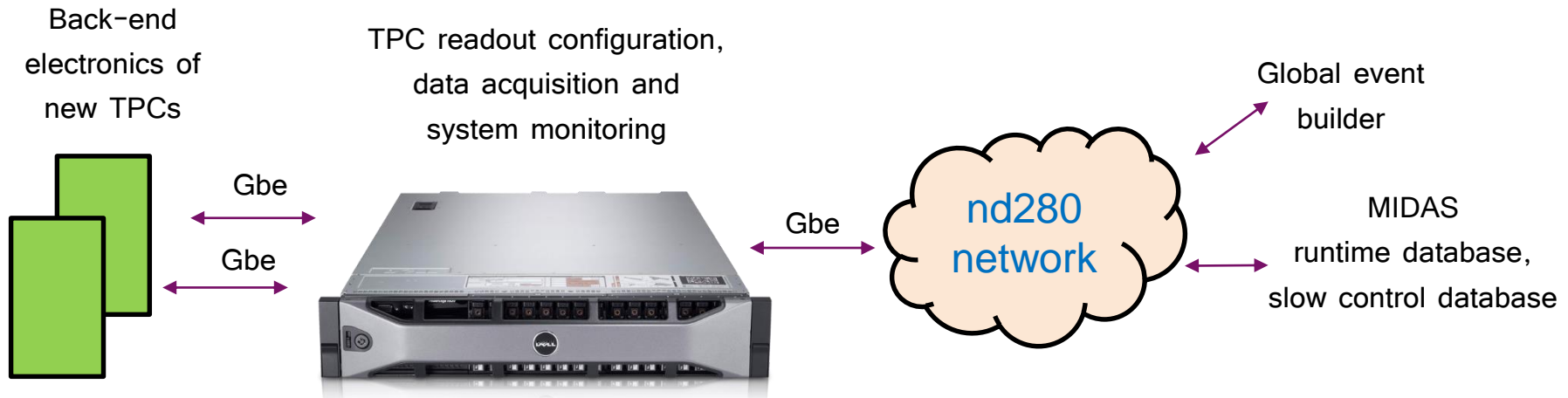
- Back-end board design, prototyping and validation
- Embedded firmware; embedded software
- Test bench not needed due to small production volume (manual testing)
- Production, validation with other building blocks
- On-site installation and commissioning

→ Interest of Lrfu for board design, firmware, embedded software, board production, etc.



16-optical ports  
Mezzanine card

Quantity required: 1 + 1 spare  
Estimated cost: 8k€



## Proposed strategy and work package outline

- Entirely based on commercial hardware
- Develop on-line software to bridge new TPC readout system to current MIDAS based DAQ

→ open to contributors

## Power supplies

- LV for front-end electronics; LV for back-end electronics
- Cables and optical fibers

→ Shared between groups responsible of front-end and back-end electronics

## Mechanics and cooling

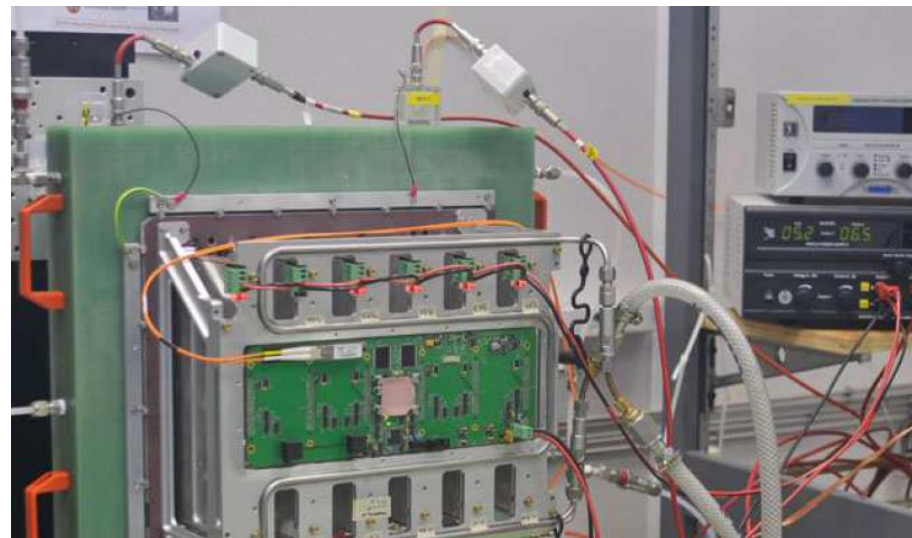
- Support plates for front-end electronics, provides mechanical support, protection, shielding & cooling
- Water cooling system needed for front-end; ventilated crate for back-end

→ Separate tasks from the electronics itself (but close interaction)

Open to collaborators – potential interest of Irfu not yet discussed internally

## Purpose & tools

- Test all the detectors of the new TPC
- Robot arm to move radioactive source and scan detector
- Gas box, HV, LV, readout electronics for 1 module and small DAQ cooperating with robot arm



Test bench for production of detectors T2K phase 1  
(IFAE/CERN/IRFU)

## Proposed strategy

- Probably difficult to re-use or adapt system used 10 years ago (obsolete, dismantled?)
- Mostly new system; need not wait until final electronics of T2K-II is made (e.g. use GROCs + TDCM?)

→ Interest of Warsaw group to take responsibility for this system

| MM Module Segmentation  | 24 × 32 or<br>32 × 24 | 27 × 32 or<br>32 × 27 | 32 × 32               | 32 × 36 or<br>36 × 32 |
|-------------------------|-----------------------|-----------------------|-----------------------|-----------------------|
| Pad count per MM Module | 768                   | 864                   | 1024                  | 1152                  |
| ASIC count per FEC      | 6 (3)<br>× 64-channel | 6 (3)<br>× 72-channel | 8 (4)<br>× 64-channel | 8 (4)<br>× 72-channel |
| FEC count per MM module | 2 (4)                 |                       |                       |                       |

## Parameters not constrained by electronics

- Number of TPCs to build: choice between 1, 2, 3 or 4
- Number of detector modules per TPC end-plate: up to 16 (assuming 1 BE board per TPC)
- Detector module size: recommended size between 20 cm × 20 cm up to 50 cm × 50 cm
- Not forced to keep a 1:1 correspondence between a MM detector and a FEM + FEC block  
e.g. if 1 m × 40 cm MM modules are built, these could be read out by 2 blocks of 1 FEM + FECs.

## Present

- Proposed a tentative list of building blocks and responsible groups
- No firm commitment (at least from Lrfu) until proposed tasks are discussed internally, funding and manpower are identified
- Still several building blocks available to new contributors

## Future

- Possible goal for 2017: define precisely the new TPCs (size and segmentation), build the first prototype Micromegas detector and start testing it
- In 2018-2019: electronic board prototyping and validation
- 2020: production; 2021: installation & commissioning