ToF Electronics

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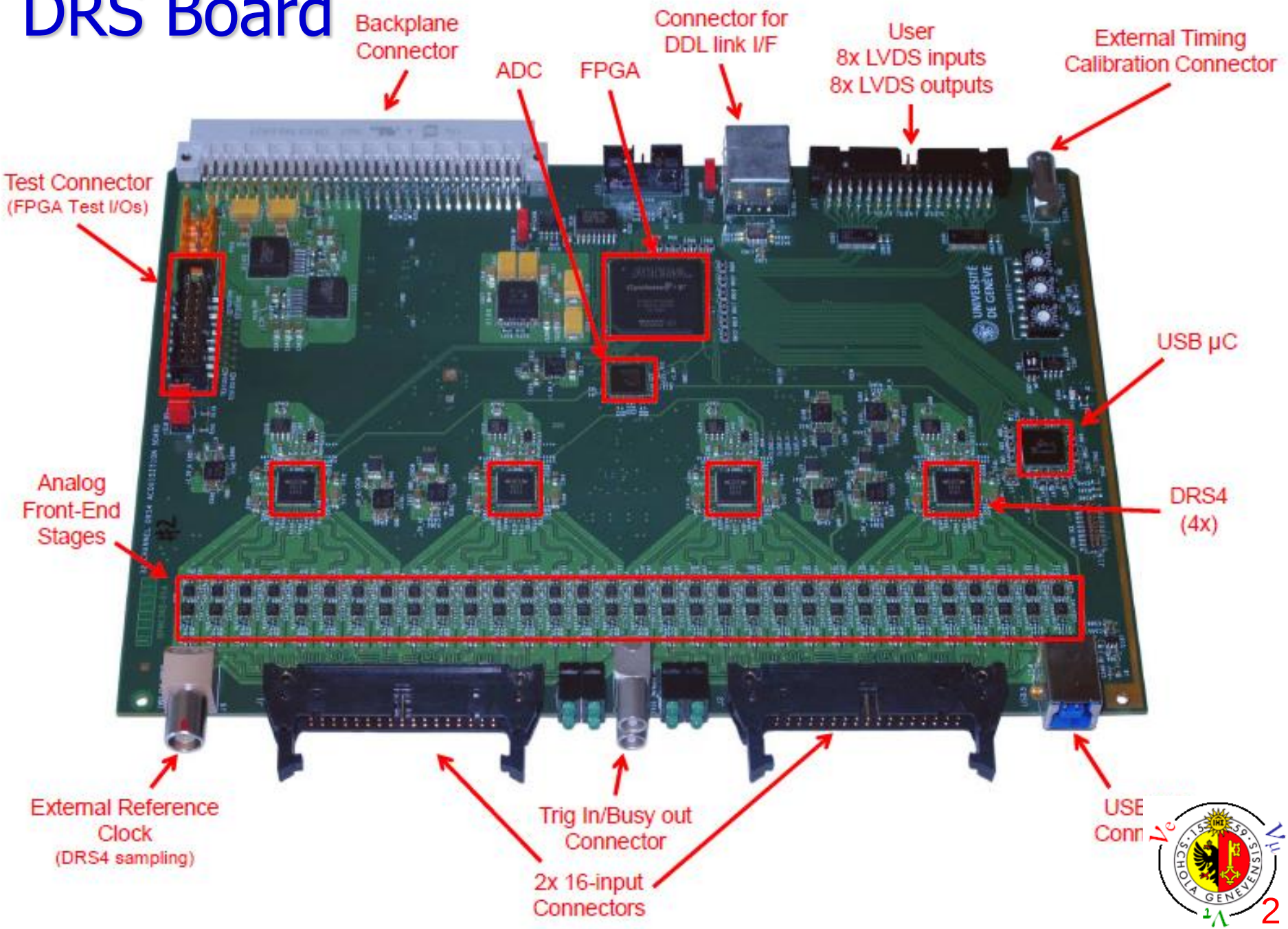
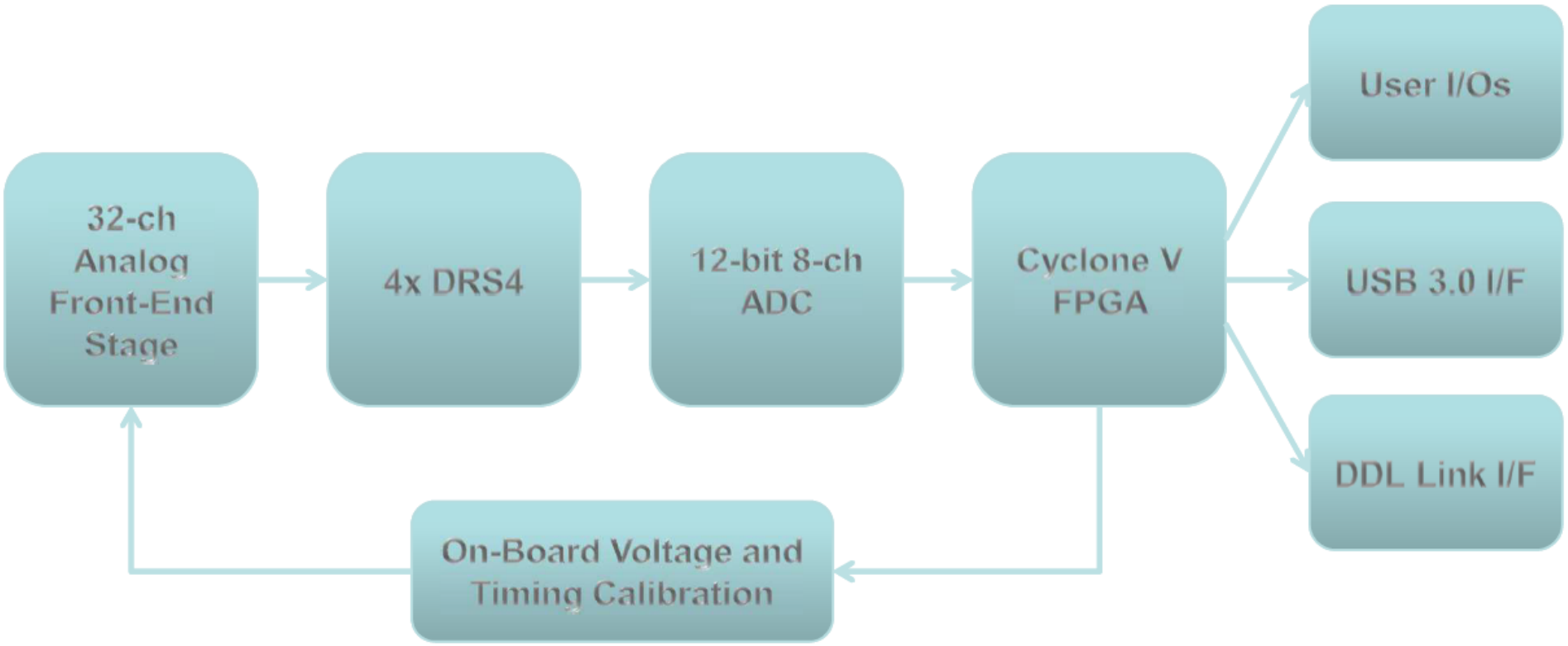
ND280 UPGRD
21 March '17

DRS Board

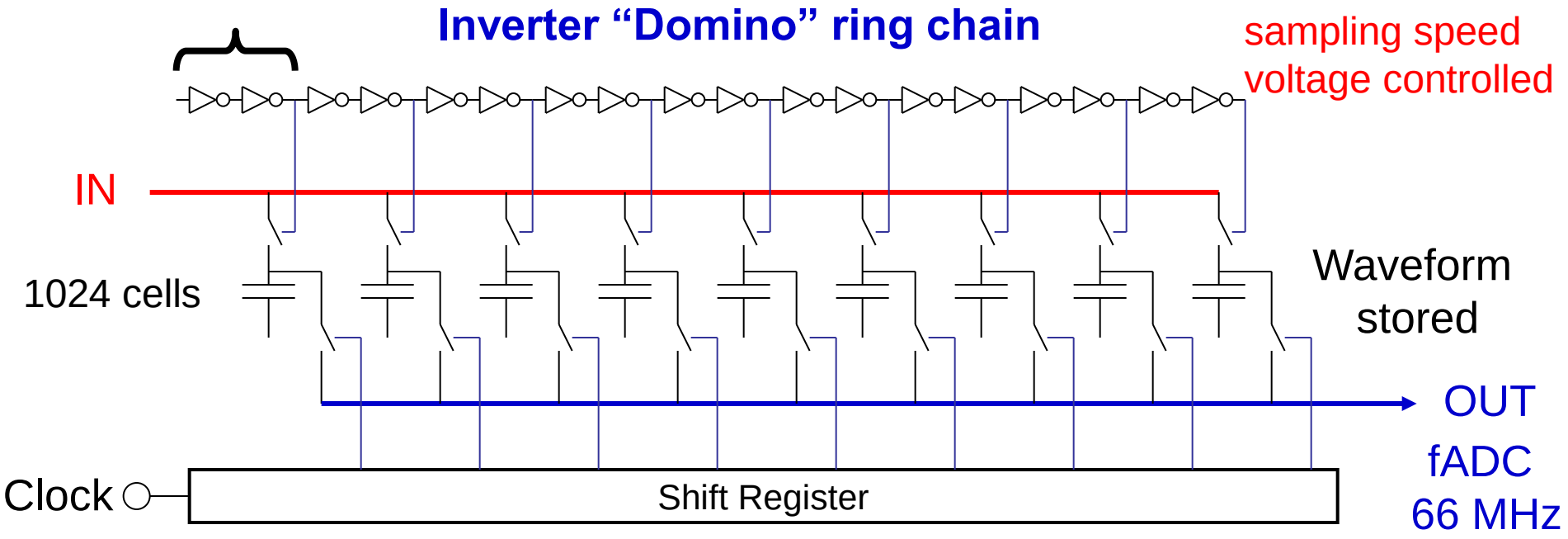

Backplane Connector
ADC
FPGA
Connector for DDL link I/F
User 8x LVDS inputs 8x LVDS outputs
External Timing Calibration Connector
Test Connector (FPGA Test I/Os)
USB µC
Analog Front-End Stages
DRS4 (4x)
External Reference Clock (DRS4 sampling)
Trig In/Busy out Connector
2x 16-input Connectors
USB Conn

Simplified Block Diagram



Switched Capacitor Array (the DRS solution)

5 GHz – 0.8 GHz: 0.2 – 1.25 ns sampling → 200 to 1250 ns deep buffer



it works like a time stretcher, but with no deterioration of signal / loss of information:

sampling ~ 5 GHz range

digitization ~ 50 MHz range

☺ cheap design !

☺ low power !

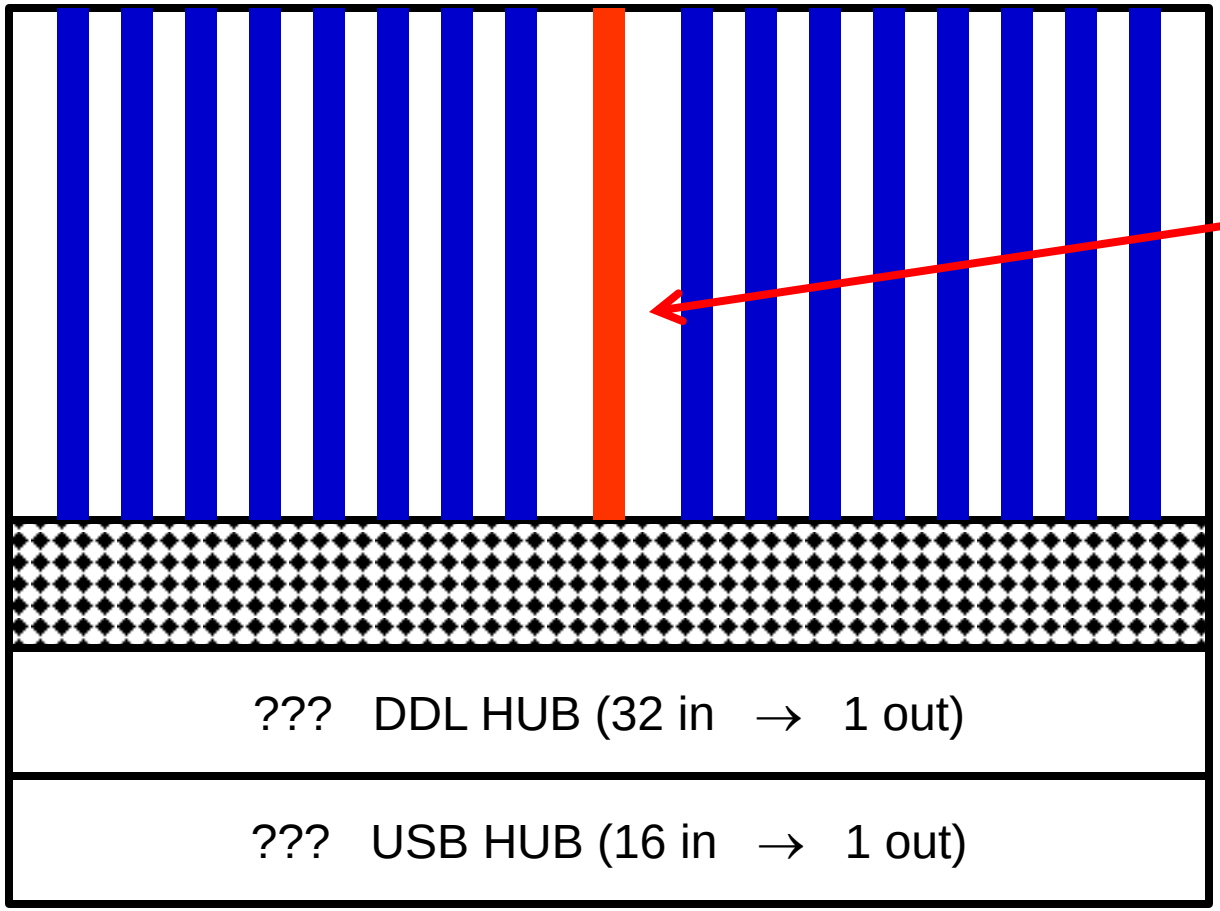
☹ one single array cannot sample during readout

→ deadtime (can be made as short as ~20 μs)!

DRS "Crate"

Standard 6U VME crate with custom backplane and +/- 6 V power supply (Wiener)

DRS boards DRS "controller" DRS boards



512 ch. / crate

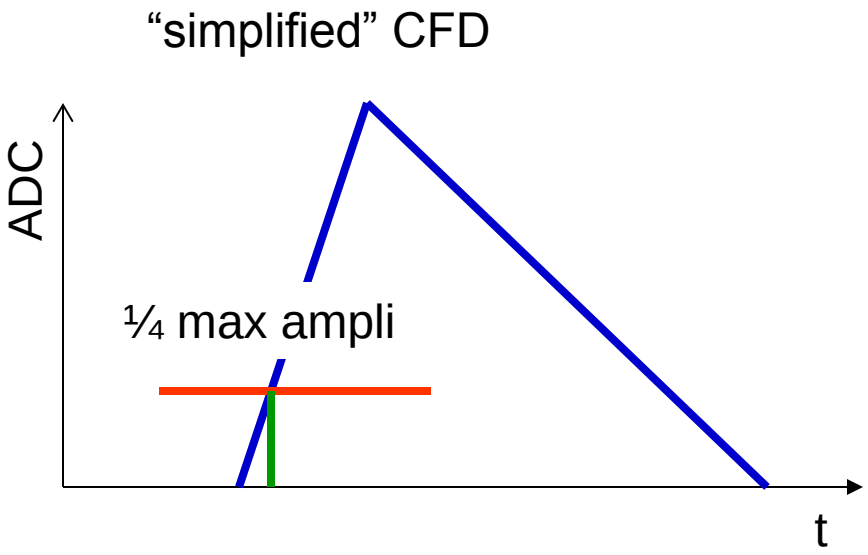
2 × 8 DRS boards

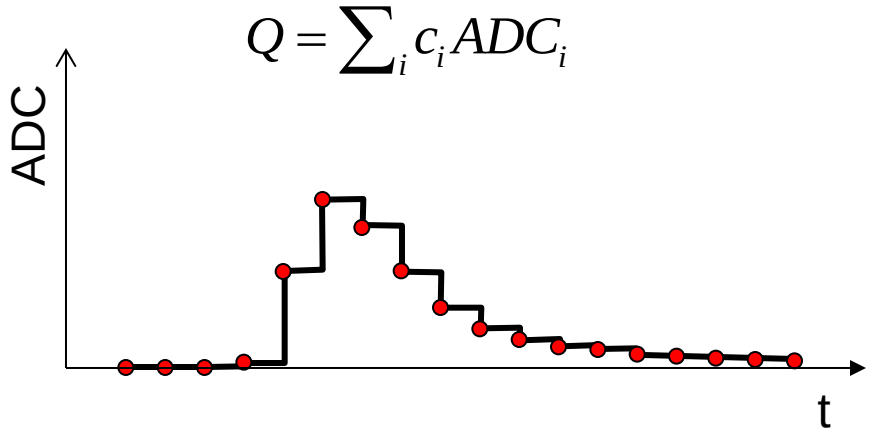
1 DRS controller
(slot 10 – middle)
clock distribution
trigger distribution
controls distribution
firmware uploading
…..

could be used also
for readout
(novel design)

with on board clock generation (controller) can have a stand alone system
with 512 synchronized channels
and USB 3.0 readout

Waveform Processing





Time resolution

1 GHz sampling

without doing anything
→ σ = 1000 ps / √12 ~ 300 ps

with "interpolation" can obtain
10 × better performance
→ σ < 50 ps

Charge resolution / dynamical range

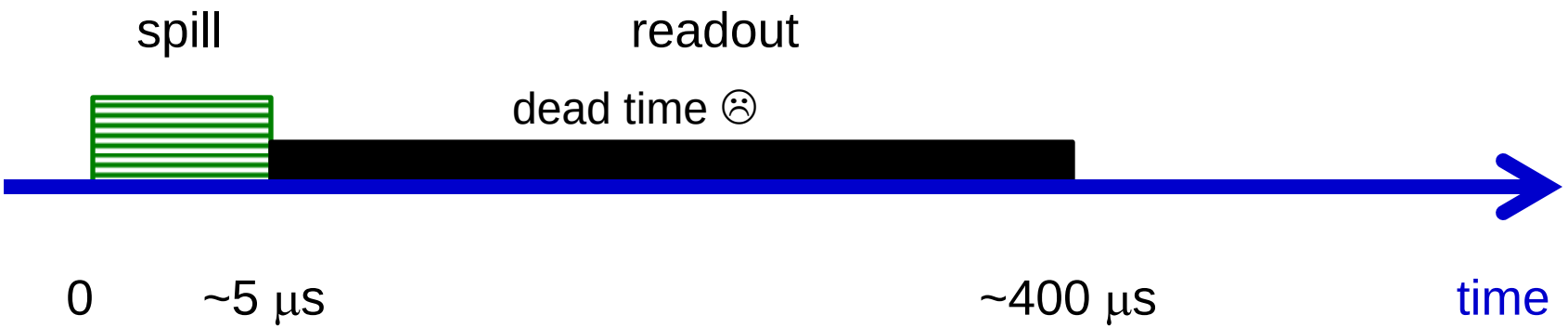
12 bit over 1 V
→ σ = 0.25 mV

waveform sampled several times i.e. ~20 ×
"effective" # of bits: 12 bit + ½ $\log_2$ n → 14 bit
→ σ = 0.25 mV / √n < 0.1 mV
(10^4 dynamical range)

Implementation in ND280

spill length ~ 5 μs
sample continuously the signals from the detectors during the spill, and digitize later
In NA61 design (serial readout of the DRS array – cheapest solution),
digitization lasts about 400 μs → deadtime), can sustain a few kHz rate
[deadtime can make as short as 20 μs]

With capacitor arrays cannot sample and digitize simultaneously → deadtime
For a low rate experiment the deadtime should not be an issue



Buffer depth and sampling time
driven by “active” window and
signal speed (for good timing, 4 or 5 samples on the rising edge)

ex. by daisy chaining 4 DRS arrays at a sampling rate of 800 MHz → 5.2 μs buffer

DRS Prototype Board

development board for NA61 readout (overkill !) and future projects
test different operation modes of the DRS ASIC
calibration procedures
firmware development

features of the board:

4 + 1 input channels

analog Front-End stage
> 500 MHz BW

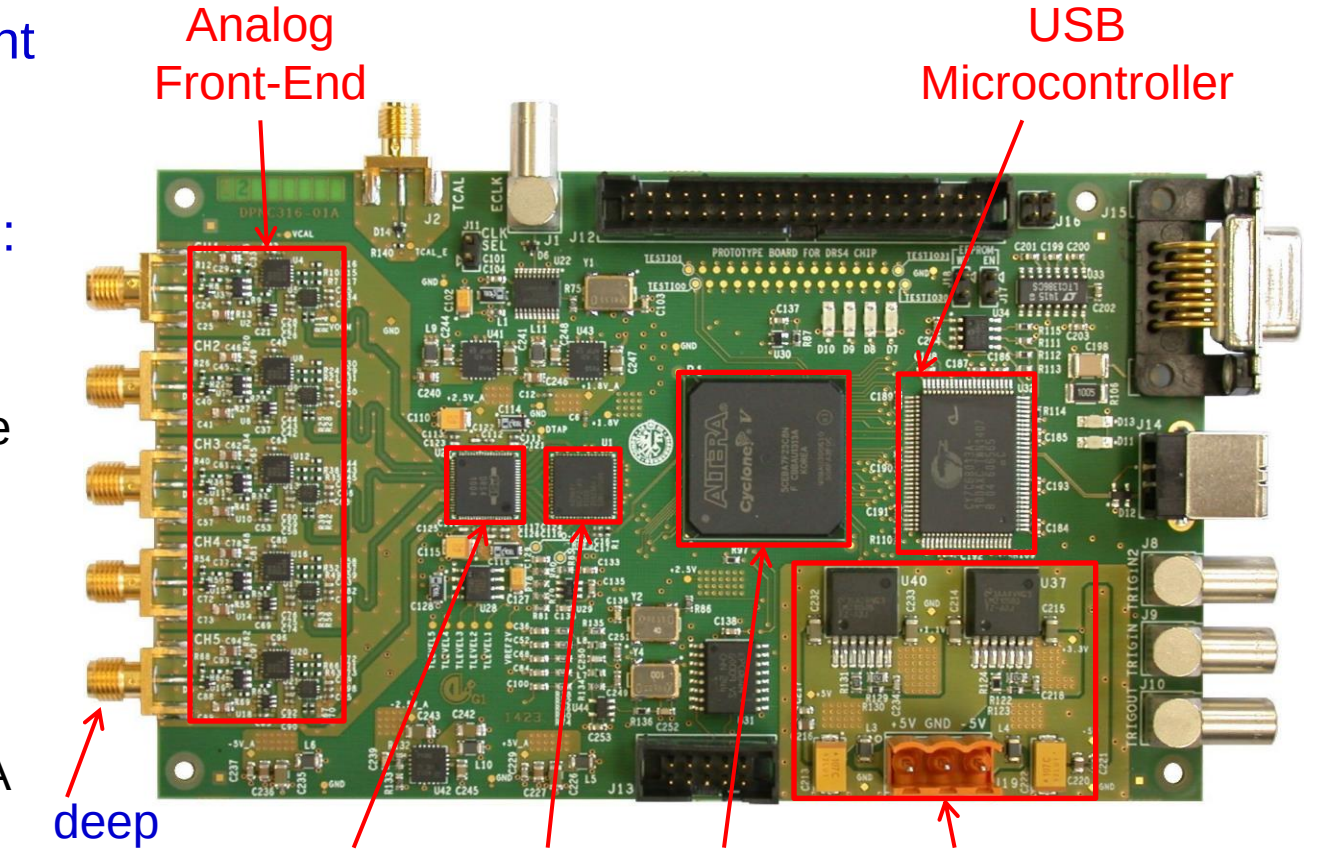
DRS4 ASIC

12-bit 8-channel ADC

Altera Cyclone V FPGA

USB Microcontroller

on-Board timing and
voltage calibration



Outlook

Can start from the existing (NA61) design
- keep the digital part (ADC, FPGA) with some modifications
- 16 ch. (8 DRS chips) / board (to contain costs)
- use same calibration scheme

About 9 months to develop such electronics
(can start working on this in fall 2017)

Need to develop the readout for the DRS boards
(unless we are happy with the USB 3.0)

Cost: too early, expect something around 100 $.