THE CONSTRUCTION OF THE PHASE 1 UPGRADE OF THE CMS PIXEL DETECTOR

Hannsjörg Weber
The pixel detector in CMS

- The CMS detector is one of the general purpose detectors at the Large Hadron Collider, recording the outcome of proton-proton collisions at highest energies.
- The silicon pixel detector is the inner most detector in the CMS experiment.
Outline

- Reason for the upgrade
- The new readout chip
- The new pixel module
- Cooling of the detector
- Service electronics of the detector
- Commissioning and status of the detector
Reasons for the upgrade

- The old detector was designed for $10^{34} \text{cm}^{-2}\text{s}^{-1}$ and 25 ns bunch spacing.
  - The LHC has exceeded the design instantaneous luminosity of $10^{34} \text{cm}^{-2}\text{s}^{-1}$.
- Dynamic inefficiencies / dead time caused by limited size of the readout bandwidth.
  - This effect was observed in data, and was expected to become worse in coming years.
The new pixel detector

- Installation during February/March 2017.
- **A smooth transition was needed** from installation to physics data taking: sensor technology, pixel size and module concept **very similar**.

- Move from analog to digital readout chip (ROC) → **reduced buffer overflow, avoid hit inefficiency**.
- Move closer to the beam (2.9 cm instead of 4.4 cm) → **improve vertex reconstruction**.
- Move from 3- to 4-hit coverage (one additional forward disk and barrel layer) → **increase redundancy and track finding efficiency**.
- New bi-phase CO$_2$ cooling system
- Move service electronics further away from interaction point. → **reduce material budget/mass**.
New readout chip design

- A 250nm CMOS ASIC with same column drain architecture as PSI46 used in the old detector.
  - Readout of 80×52 pixels
  - 26 double columns with buffers periphery (column drain).
- New features:
  - 40 MHz analog → 160 Mbit/s digital (8 bit ADC)
  - Increase of data (32→80) and timestamp (12→24) buffers.
  - Higher radiation tolerance.
  - Noise reduced: Threshold from 3200 e⁻ to 1800 e⁻.
- Special version for barrel layer-1 (580 MHz/cm²) with cluster readout:
  - readout clusters of 4 pixels instead of single pixel (dynamic cluster column drain)
New modules and production

- Sensor + 16 readout chips + printed circuit board (a high density interconnect):
  - 16 ROCs per module
  - The active area is a 280µm thick n⁺-in-n planar silicon sensor layer.
    - ~66000 pixels with 100×150 µm² each per module
  - The readout chips are bump-bonded to the silicon sensor.
  - The TBM on the HDI organizes the data stream of the readout chips.
- The detector is comprised out of 1856 modules.
  - The number of readout channels is increased by a factor of about 2 with respect to the old detector.
Quality control of modules

- All pixel modules underwent **rigorous testing**.
  - **Thermal stress** for assessing poor bumpbond or wirebond quality.
  - **X-ray exposure tests**: check high rate performance
  - **Series of calibration tests** at both room temperature and operation temperature of -20 °C.

For more details, see Dehua Zhu’s contribution.

### Pixel Turn-on Threshold

**Layer-1 barrel pixel ROCs**

- **High rate X-ray test**
  - >99% efficient

**PROC600v2 (sample P302) efficiency**

- Trimmed to: 45, edge masked
- WBC: 160
- Vdig: 6, lana: 24 mA
- Vwilsh=vwilpr: 150

**Forward pixel modules**

- **Grade C**
- **Grade B**
- **Grade A**
- **Installed**

![Graph showing pixel turn-on efficiency](image)
3 disk FPIX!

4 layer BPIX!

BPIX Supply Tube (4x)!

\[\approx 5.6 \text{ m} \]

module! connections! (connector PCB)!

optical links (DOH)!

DC-DC! LV-power conversion!

CO\(_2\) cooling loop!

FPIX Service Cylinder (4x)!
Cooling

• Moved from single-phase $\text{C}_6\text{F}_{14}$ to two-phase $\text{CO}_2$ at -20 °C.
  • Use latent heat
  • Thinner pipes (50 μm wall-thickness in active area)

• Benefitting from high thermal conductivity of Carbon Fiber/Thermal Pyrolytic Graphite → compact system: overall reduction of material
On-detector service electronics

- **Power boards**: Convert high voltage-low (direct) currents to low voltage-high currents.
  - **Reduce on-detector power losses** → needed due to ~doubling of readout channels, while reusing the same power cables.

- **Readout and control boards**:
  - Distribute power and bias voltages
  - Distribute LHC clock
  - Distribute calibration signals
  - Convert electric signals (including pixel hit data) to/from pixel modules to optical signals.
Detector installation

Forward Pixel

Barrel Pixel

photo by Michael Habeck@cern.ch
Commissioning of the pixel detector

- **Repeated calibration** done during module qualification to get the detector in optimal state prior to any data taking.
  - Greatly benefit from testing of pixel modules/electronics prior to construction.

- Used **cosmic data** for further commissioning testing.
  - Very coarse detector timing alignment (correct bunch crossing),
  - Coarse spatial alignment,
  - Rigorous testing of readout system.

- Used **first proton-proton collisions** for final commissioning, such as fine alignment.

For commissioning including pp collision data, see Viktor Veszpremi’s contribution.
Status of the pixel detector

- From previous detector expect 98% active pixels.
- 95.5% of all pixels are active.
  - Localized groups due to service failures.
- Due to increased redundancy, negligible impact on physics performance.

Recovered!

Problem in readout group

Problem in power group
Comparison old vs. new detector

- Hit efficiency vs. instantaneous luminosity

Old detector

New detector

Gained efficiency
Summary

• CMS replaced its pixel detector in early 2017.
• The new detector has been commissioned and is successfully taking data.
  • About 95.5% of pixels are fully functional.
• The new detector allows high quality physics data taking until the HL-LHC upgrades.
Backup
Performance comparison

\( \sqrt{s} = 13 \text{ TeV} \)

<table>
<thead>
<tr>
<th>Old detector</th>
<th>New detector</th>
</tr>
</thead>
<tbody>
<tr>
<td>CMS Preliminary 2015</td>
<td>CMS Preliminary 2017</td>
</tr>
<tr>
<td>Track ( p_T &gt; 12 \text{ GeV} )</td>
<td>Track ( p_T &gt; 12 \text{ GeV} )</td>
</tr>
<tr>
<td>( \sigma_r = 29.09 \mu m )</td>
<td>( \mu_r = 1.49 \pm 0.88 \mu m )</td>
</tr>
<tr>
<td></td>
<td>( \sigma_r = 13.34 \pm 1.19 \mu m )</td>
</tr>
<tr>
<td></td>
<td>RMS = 40.45 \mu m</td>
</tr>
</tbody>
</table>

\( x \times 10^3 \) vs. \( \Delta y \) [\mu m] for the Old detector, and \( x \times 10^3 \) vs. \( \Delta x \) [\mu m] for the New detector.
Timing alignment

- We aim to optimize the cluster size and cluster charge in order to achieve the best hit efficiency and cluster properties.
- There is timing difference between Layer 1 and 2 due to different readout speed, but only a common timing choice can be set (nominal setting is 6ns).
Timing alignment

- We aim to optimize the cluster size and cluster charge in order to achieve the best hit efficiency and cluster properties.
- There is timing difference between Layer 1 and 2 due to different readout speed, but only a common timing choice can be set (nominal setting is 6ns).

---

**Hit Efficiency**

- Disk 1
- Disk 2
- Disk 3

**Avg. On-Track Cluster Size (pixel)**

- Disk 1
- Disk 2
- Disk 3

**CMS Preliminary 2017**

\( \sqrt{s} = 13 \text{ TeV} \)
New detector’s (expected) performance

Expected improvement on b-tagging capabilities: ~10% for fixed misid. rate

Pixel matching to electron track in proton-proton collision data
Comparison current/upgraded detector

Phase 1 layout

<table>
<thead>
<tr>
<th>Layer</th>
<th>Current</th>
<th>Upgrade</th>
</tr>
</thead>
<tbody>
<tr>
<td>Depth</td>
<td>3 layers</td>
<td>4 layers</td>
</tr>
<tr>
<td>16.0 cm</td>
<td>2.9 cm</td>
<td>6.8 cm</td>
</tr>
<tr>
<td>10.9 cm</td>
<td>7.3 cm</td>
<td>10.2 cm</td>
</tr>
</tbody>
</table>

Present layout

<table>
<thead>
<tr>
<th>Layer</th>
<th>Current</th>
<th>Upgrade</th>
</tr>
</thead>
<tbody>
<tr>
<td>Depth</td>
<td>3 layers</td>
<td>4 layers</td>
</tr>
<tr>
<td>4.4 cm</td>
<td>7.3 cm</td>
<td>10.2 cm</td>
</tr>
</tbody>
</table>

1856 modules, 124M pixels
1440 modules, 66M pixels
Module production

2016-10-31

Barrel modules

FPiX Module Construction
Complete inner disks -Z: 6, +Z: 6 (out of 6 + 6)
Complete outer disks -Z: 6, +Z: 6 (out of 6 + 6)
- Bump bonded
- Assembled
- Detector grade (A only)
- Detector grade (A+B)
- Installed
- Forecast
Quality control of modules

- All pixel modules underwent **rigorous testing**.
  - **Thermal stress** for assessing poor bumpbond or wirebond quality.

Locations of faulty bump bonds in all modules for forward part

Locations of faulty bump bonds in installed modules for forward part

Reject modules that have a large number of faulty bumps. The number of rejected modules was initially quite high for the forward pixel modules. **Constant feedback/discussion with vendor helped to mitigate issue.**
Exploded view of full detector

- BPIX Supply Tube (4x)
- 4 layer BPIX!
- 3 disk FPIX!
- ~5.6 m
- module! connections! (connector PCB!)
- optical links (DOH!)
- DC-DC! LV-power conversion!
- CO₂ cooling loop!

FPIX Service Cylinder (4x)!
Layout of the PROC600

(1) **Pixel array**: 52 columns and 80 rows arranged in groups of 2 columns (26 double columns)

(2) **26 Double Column Interfaces**

(3) **Control Interface Block**: readout logic, DACs, I2C interface, voltage regulators, reference and pads
PROC600 parameters

Design parameters

• chip size: 7860μ x 10500μ
• 339 transistor/pixel
• pixel arrangement: 53 x 80
• DCCD transfer in DC at 40MHz
• Data Buffer Cells: 4 x 56
• Timestamp Buffer Cells: 40
• ROC Read-out Buffer Cells: 64
• total # of transistors: 2.2M
• analog pulse height: 8 bit ADC
• pixel hit rate: 600MHz/cm²
• expected rad. hardness: ~500MRad
• power consumption: <150mW/cm²

Taken from A. Starodumov (PIXEL2016)
PROCD600 features

- Main idea: readout cluster of 4 pixels instead of single pixels
  - Dynamic Cluster Column Drain mechanism (DCCD) introduced
  - allows up to 7 pending column read outs
  - major circuit redesign
- DCCD vs individual pixel readout
  - mean size of 2x2 cluster in double column is 1.95 pixels
  - mean number of clusters per event per double column is 1.2 at 600 MHz/cm² hence 2.34 pixels per column drain (CD)
  - Individual pixel readout (psi46dig chip): need \( \sim 2n+3 \) clocks per CD \((n=\text{#pixels})\): 7.7 clocks per CD
  - DCCD (PROC600): need \( m+2 \) clocks per CD \((m=\text{#clusters})\): 3.2 clocks per CD
  - gain of factor 2.4 in speed
  - new logic design of up to 7 pending CDs gives overall factor of 3
- Data Buffer:
  - trigger verified DB check-out for up to 4 pending read outs
  - no reset after read out

Taken from A. Starodumov (PIXEL2016)
PROC600: Functionality 1

First event at timestamp A

Search for 2x2 clusters

Drain first cluster
Second event at timestamp B

Inspired by A. Starodumov (PIXEL2016)
PROC600: Functionality 2

Drain second cluster
Hits of timestamp B are preserved

Search for 2x2 clusters

Drain next cluster

Inspired by A. Starodumov (PIXEL2016)
Data acquisition system

- The old system had been based on VME.
- New system is based on μTCA:
  - High-speed signal links up to 10 Gbits/s
- The new system can handle the data throughput for 2017 pp collisions.
- Still improvement needed for end-of-life of the detector (see backup).
Data acquisition system

Detector/pixels

On detector electronics

Readout of pixel data

Controller for configuration

Connection to CMS central DAQ

Detector

Service Cylinders

Portcard/DOH motherboard

DCDC

CCU

DOH

mDOH

POH

400Mbps read-out

“fast I2C” pixel link

CCU control link

Ethernet control

TCDS: clock, trigger, TTS

(672 + 1184)

(FPix + BPix)

12 Ch fiber ribbons

SFP+

12CH

(28 + 80)

(FPix + BPix)

2368 links

FED (CTA)

mFEC

(x4 links)

mFEC

(x4 links)

mFEC

(x4 links)

mFEC

(1 + 2)

mFEC

(4 + 8)

Pix FEC (CTA)

Tk FEC (CTA)

USC μTCA Crate

S-Link Express

FEROL

MCH

AMC13

Ethernet

C-DAQ

TCDS

DCDC

(672 + 1184)

(FPix + BPix)

400Mbps read-out

“fast I2C” pixel link

Ethernet control

TCDS: clock, trigger, TTS
Commissioning of the DAQ system

- Test FED data throughput using emulated/generated pixel hits
  - send 100kHz random triggers (simulating Level-1 trigger rate at CMS)
  - read out FED data through 10Gbits/s link
  - trigger rate gets dynamically throttled according to the FED status (e.g. if FED is too busy to process the incoming data)

- No issue for data throughput for 2017 pp collisions.
- Still improvement needed for later running.

FEROL Data Throughput

- CMS preliminary
- 10% trigger throttled at PU=130
- No trigger throttled at PU=70 (expected in 2017)
High Density Interconnects Challenges

- Problems encountered:
  - Wire bonding difficulties due to the insufficient thickness of Copper under the wire-bonding pads
  - High voltage breakdowns
  - Yield issues

- Solutions:
  - Improving visual inspections
  - Making thickness measurements on the thicknesses of layers on selective high density interconnects from each batch
  - Preventing high voltage breakdowns by improving the backing of the HDIs besides adding an additional layer of Kapton.
  - Making more batches, improving fabrication process (vendor)

Taken from M. Alyari (DPF2017)
Welding Challenges

- Welds were needed on each forward pixel CO$_2$ cooling loop
- Problem encountered:
  - Concerns over hot cracking were raised and it was decided to micrograph welds and investigate
- Lesson learned:
  - Material composition plays a role in final microstructure and cracking susceptibility
  - The weld pool mixture of ultra high purity 304L Stainless Steel + 316L Stainless Steel lowers susceptibility to cracking (refer to Stephanie Timpone’s talk at FTDM 2016 for more details)