Monolithic pixel development in TowerJazz 180nm CMOS for the outer pixel layers in the ATLAS experiment

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Outline

- Introduction

- Monolithic active pixel sensor characterisation
  - The TowerJazz Investigator chip
  - Charge collection measurements
  - Irradiation results
  - Beam test results

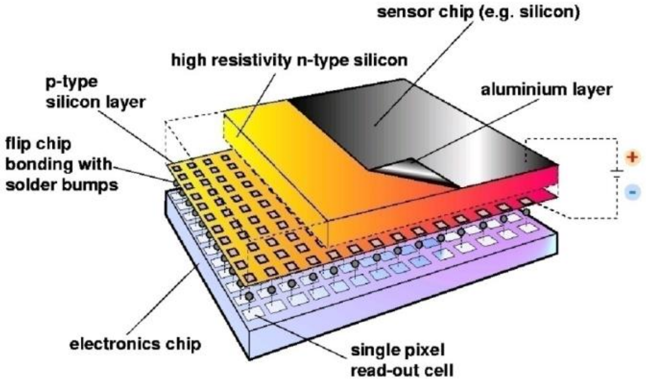
- Design of large-scale monolithic demonstrators
  - The “MALTA” chip
  - The “TJ-Monopix” chip

- Summary

Pixel detectors

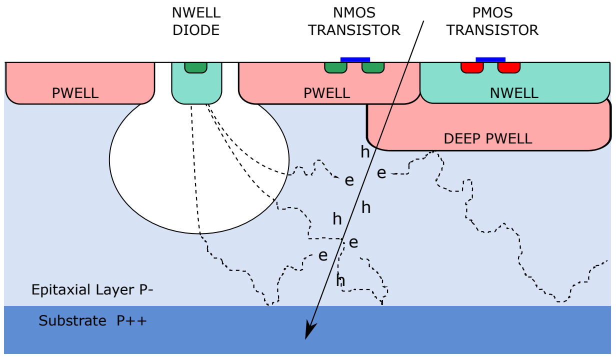
- The first measurement layers in ATLAS (closest to the particle collision point)
- Used to reconstruct charged particle tracks

- Hybrid pixel detectors



  - Used in the majority of presently installed systems
  - Sensor and readout circuitry on separate chips (can be optimised separately)
  - Fast, radiation hard, but complex assembly

- Monolithic pixel detectors



  - Sensor and readout integrated into the same chip
  - Potentially better power-performance ratio and strong impact on material budget
  - High resolution, low cost, recent progress in radiation hardness

Radiation hard monolithic sensors

- Target: development of CMOS sensors for potential use in ITK pixel layers
- Requirements:
    - fast time resolution (< 25 ns bunch crossing time)
    - short dead time because of high particle rates (< ~1 μs)
    - low power consumption
    - tolerance to ionising and non-ionising radiation

↓

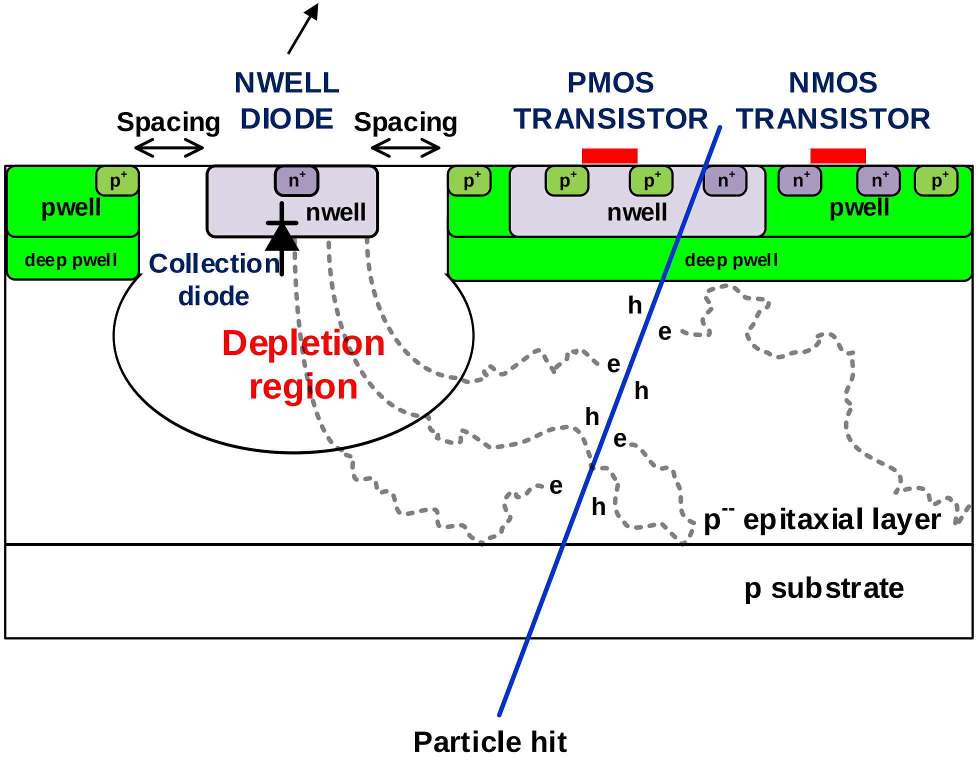
charge collection by drift rather than diffusion

	STAR	ALICE-LHC	ILC	ATLAS-HL-LHC	
				Outer	Inner
Required Time Res. [ns]	110	20 000	350	25	
Particle Rate [kHz/mm^2]	4	10	250	1000	10 000
Fluence [n_{eq}/cm^2]	> 10^{12}	>10^{13}	10^{12}	10^{15}	10^{16}
Ion. Dose [Mrad]	0.2	0.7	0.4	50	1000

Sensor technology

- TowerJazz 180nm CMOS imaging process
- High resistivity (> 1kΩ cm) p-type epitaxial layer (25 µm thick)
- Deep PWELL shielding NWELL allowing in-pixel PMOS

2-3 µm → small C!



$\frac{Q}{C} \nearrow$
- – better analog performance
- – lower power consumption

- Reverse bias to further reduce input capacitance and increase depletion volume (still difficult to deplete under deep PWELL)

Modified process

- Novel modified process developed in collaboration with the foundry
- Adding a planar n-type layer significantly improves depletion under deep PWELL
- Increased depletion volume → fast charge collection by drift

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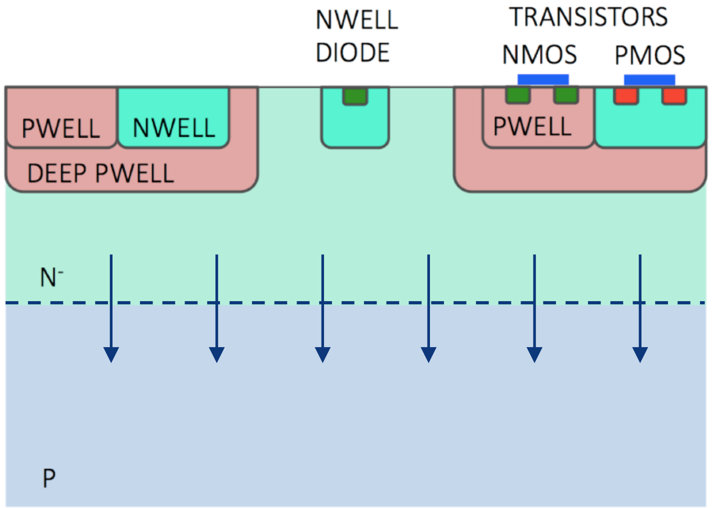
better time resolution
reduced probability of charge trapping
(radiation hardness)



W. Snoeys et al.
DOI 10.1016/j.nima.2017.07.046

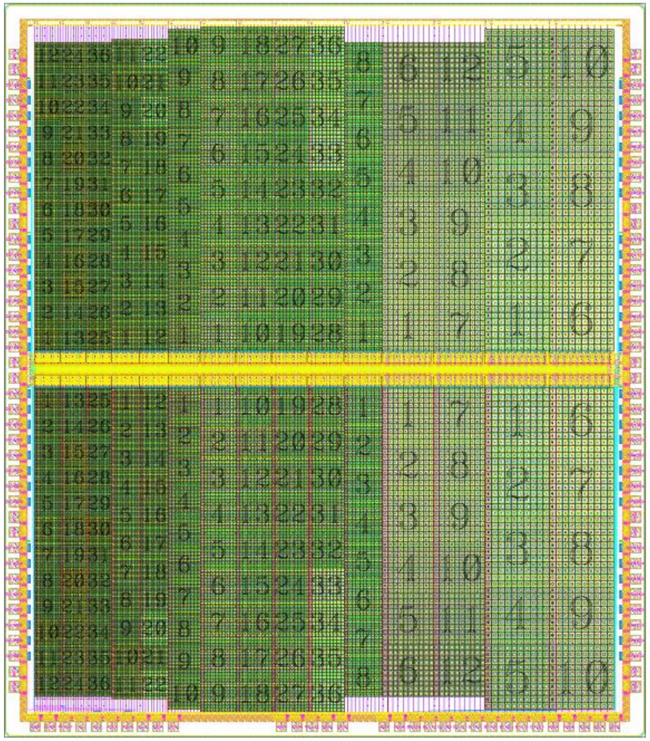
- Possibility to fully deplete sensing volume
- No significant circuit or layout changes required

The TowerJazz Investigator chip

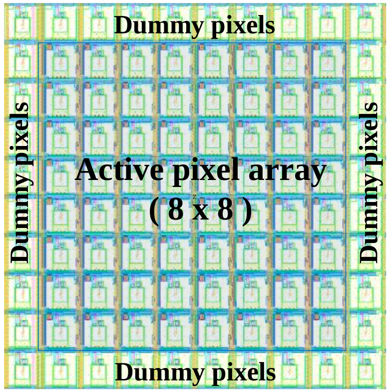
- Developed by ALICE as test chip for the ITS upgrade development
- 134 pixel sub-matrices of different designs (electrode size, PWELL spacing)
- Each sub-matrix contains 8x8 pixels surrounded by dummies
- Possibility of simultaneously measuring the analog signals on 64 pixels

Investigator-1 layout

5.0 mm x 5.7 mm

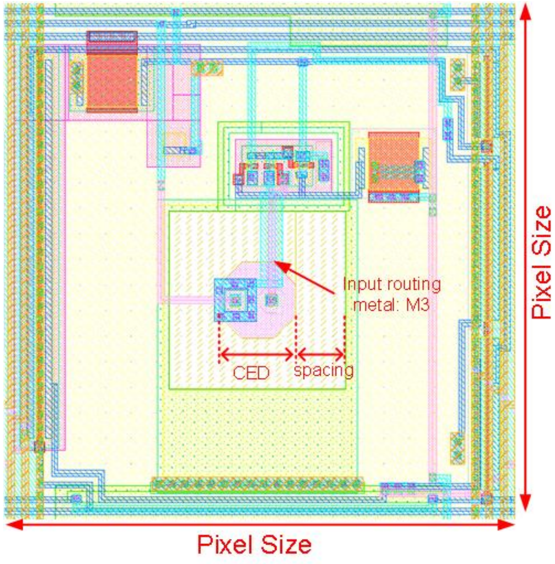


Mini-matrix



Mini-Matrix number	*Pixel size*
0 – 35	**20 by 20 um^2**
36 – 57	**22 by 22 um^2**
58 – 67	**25 by 25 um^2**
68 – 103	**28 by 28 um^2**
104 – 111	**30 by 30 um^2**
112 – 123	**40 by 40 um^2**
124 – 133	**50 by 50 um^2**

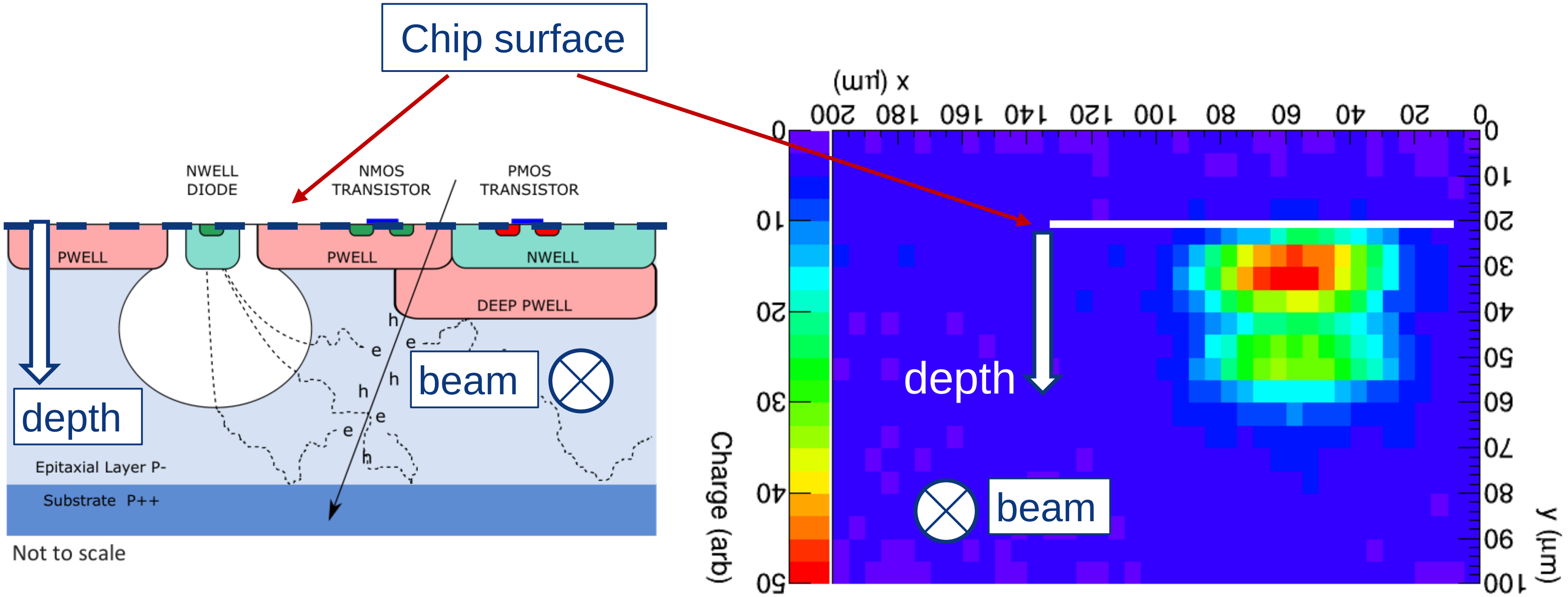
Pixel layout



C. Gao et al.
DOI 10.1016/j.nima.2016.03.074

Charge collection measurements

- Edge-TCT: used to study charge collection uniformity within the pixel



- Tests on Investigator chip done in IJS, Ljubljana on two structures:
  - 20x20 µm^2 pixel size
  - 50x50 µm^2 pixel size

Charge collection measurements

- e-TCT measurements show depletion of epi layer even after 10^{15} n_{eq}/cm^2 at -6V

- Signal collection after 10^{15} n_{eq}/cm^2 irradiation also directly under deep PWELL

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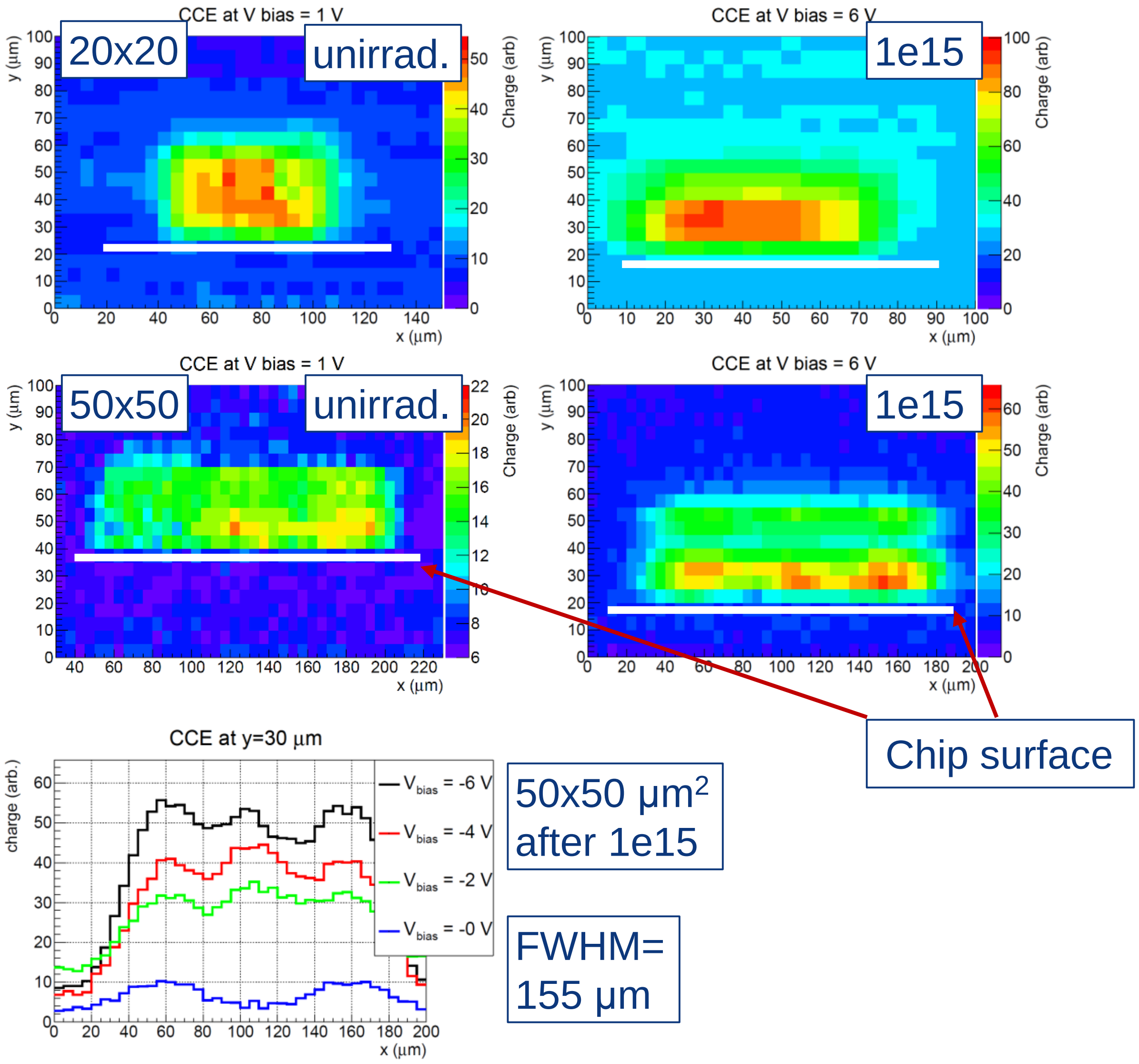
with process modification the full pixel is depleted!



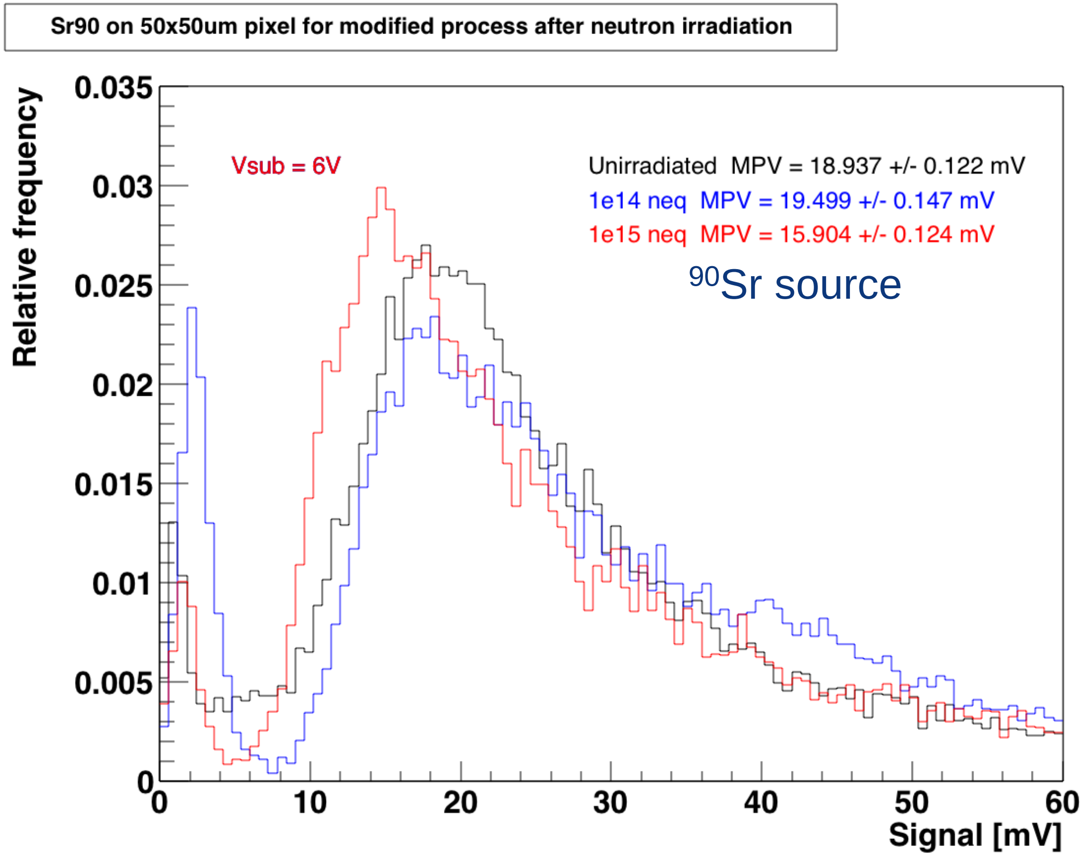
Chip surface

50x50 μm² after 1e15

FWHM= 155 μm

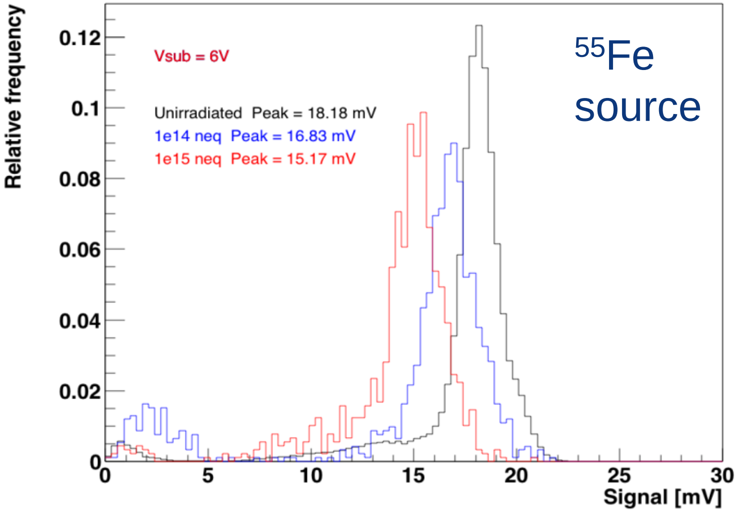
Irradiation results

- Investigator irradiated up to 10^{15} n_{eq}/cm^2 and 1 Mrad in several steps



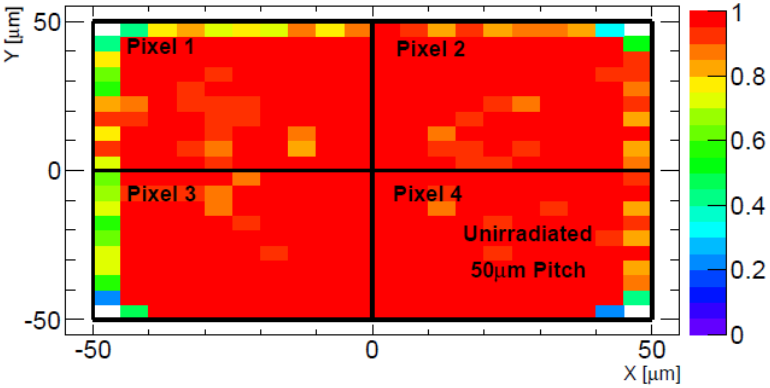
H. Pernegger et al., DOI 10.1088/1748-0221/12/06/P06008

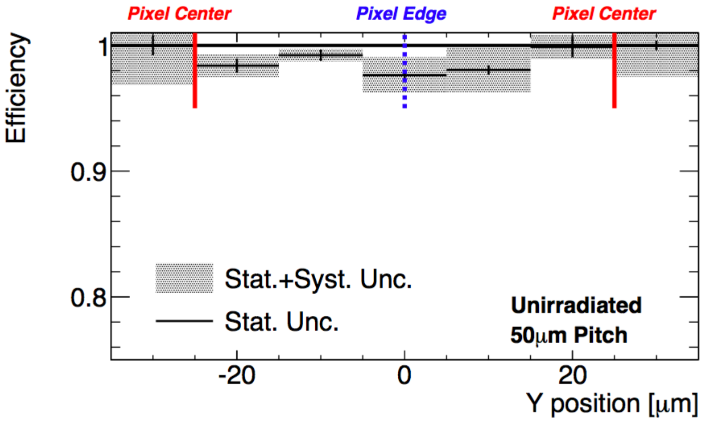
- Little change in signal after irradiation
- Signal well separated from noise



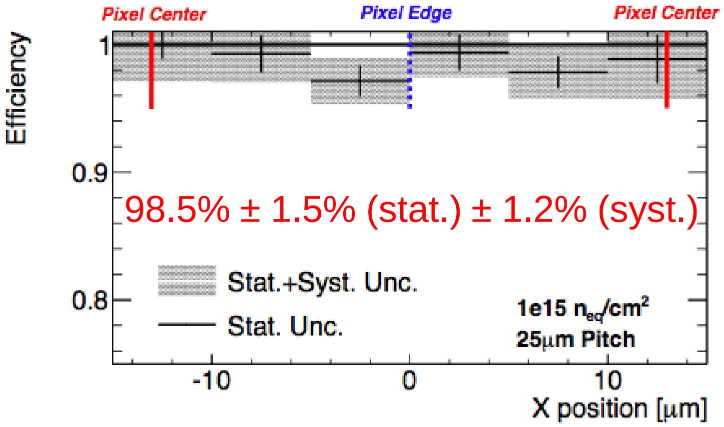
Beam test results

- Unirradiated sensor efficiency 98.5% ± 0.5% (stat.) ± 0.5% (sys.) (50x50 μm^2)

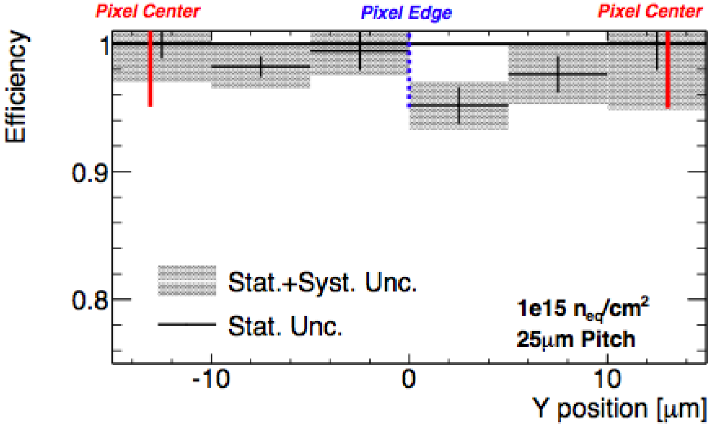




- Irradiated sensor also shows uniform efficiency across 25x25 μm^2 pixel



98.5% ± 1.5% (stat.) ± 1.2% (syst.)



Design of large-scale demonstrators

- Measurement results show improved radiation hardness for sensors manufactured using the modified process

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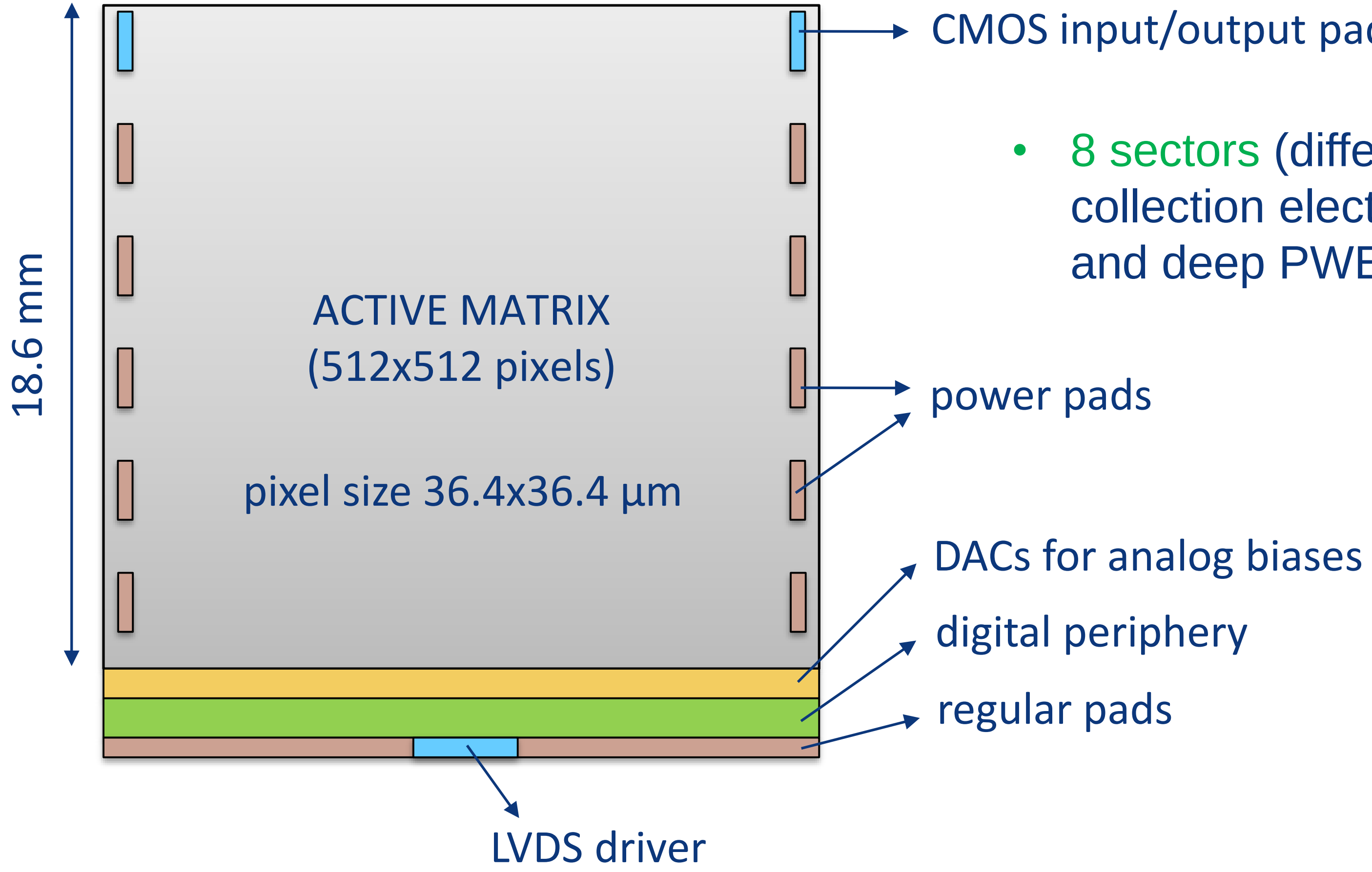
Design of two full-scale demonstrators to match ATLAS specifications for outer pixel layers

- The “MALTA” chip
  - Analog front-end based on a previous design for the ALICE experiment
  - Novel asynchronous readout architecture to reduce digital power consumption and increase hit rate capability in the matrix

- The “TJ-Monopix” chip
  - Front-end similar to the “MALTA” chip
  - Uses the well-established column drain readout architecture (experience from LF-Monopix design)

The “MALTA” chip

- “MALTA” (Monolithic from ALICE To ATLAS) chip under development at CERN

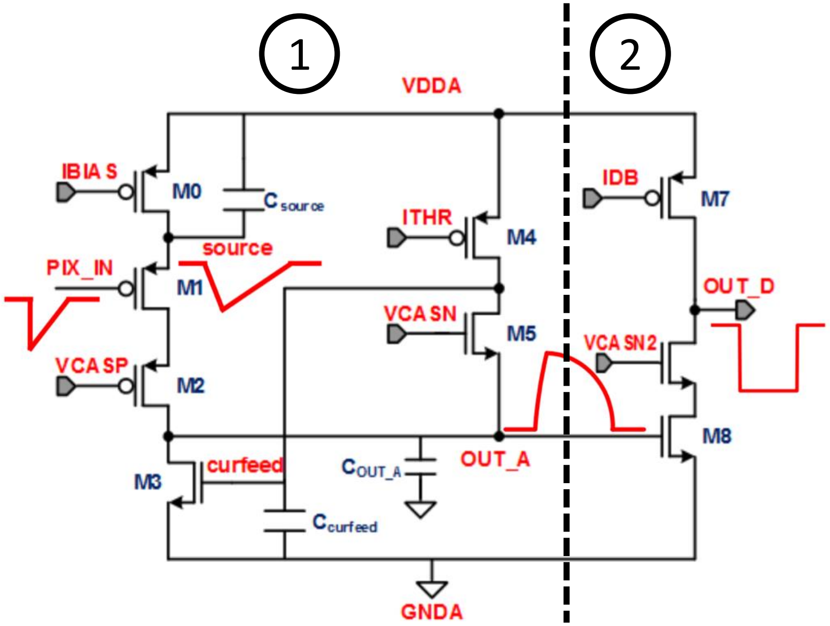


- 8 sectors (different collection electrode size and deep PWELL spacing)

Analog front-end

- Based on the front-end of the ALPIDE chip (previously developed for the upgrade of the ALICE experiment)

1 – amplification
2 – discrimination

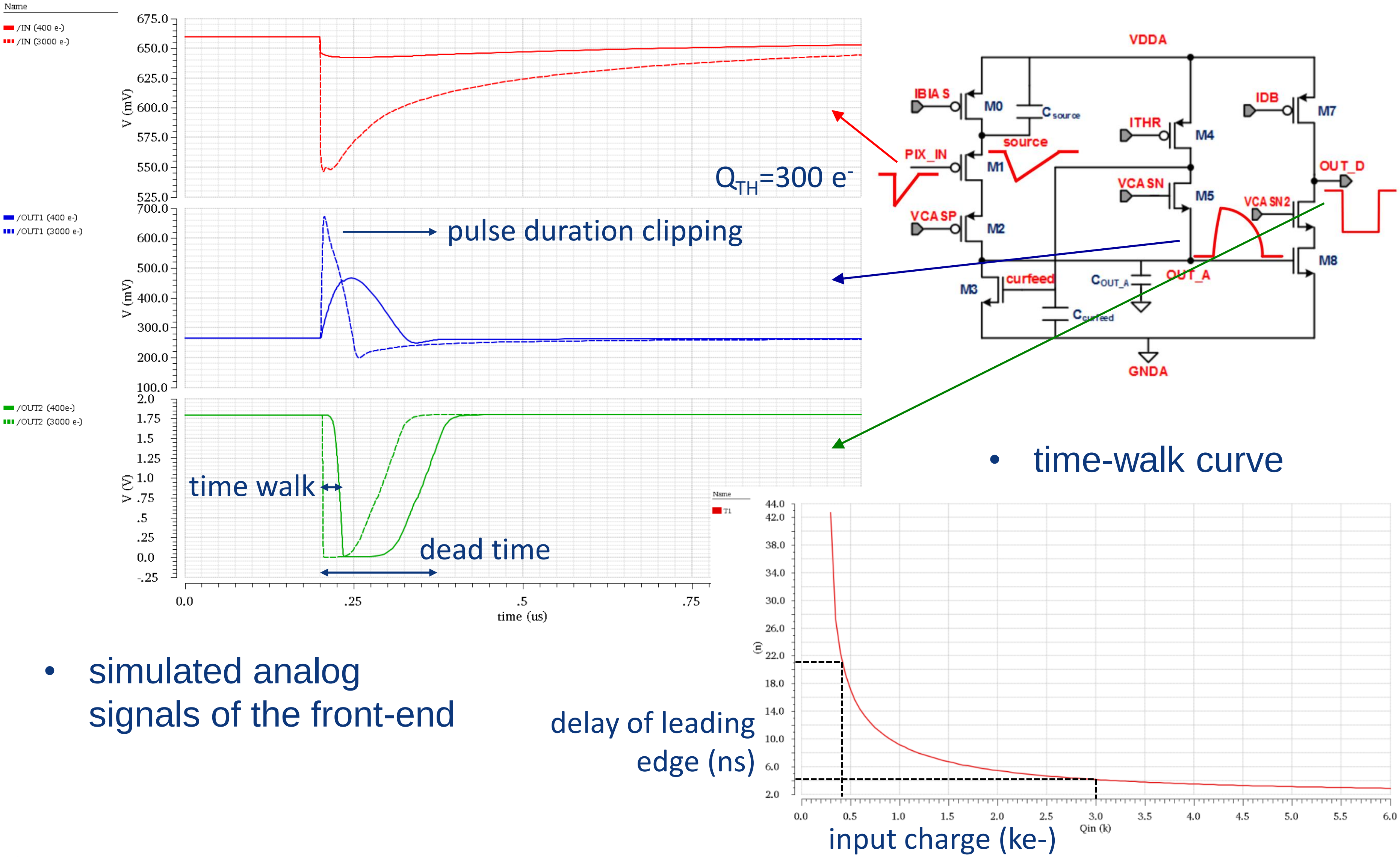


digital
architecture

D. Kim et al.
DOI 10.1088/1748-0221/11/02/C02042

- Improvement for fast timing (< 25 ns) and hit rate capability by increasing current consumption (250-500 nA/pixel, < 1 μW/pixel)

Front-end timing optimisation

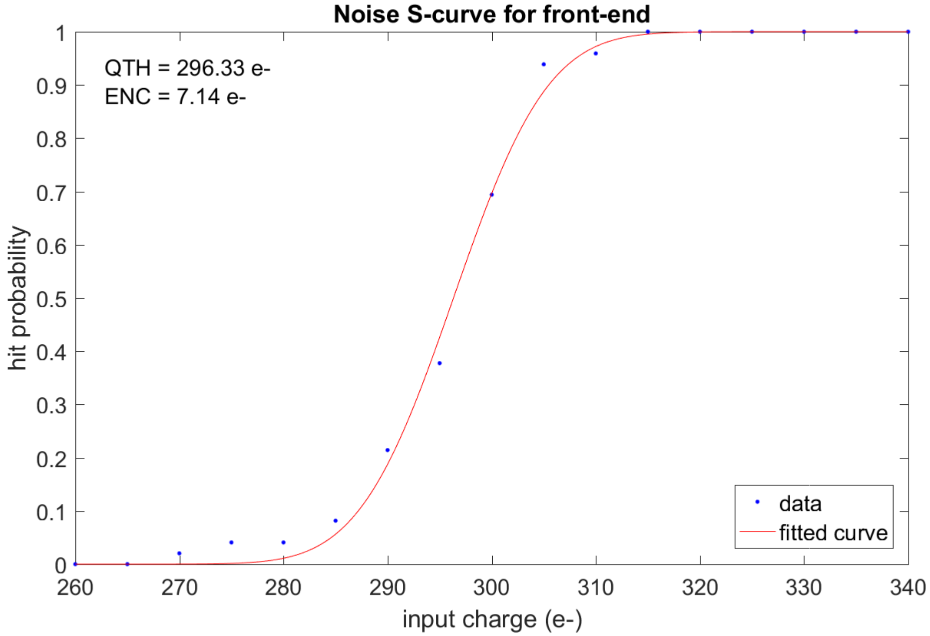


- time-walk curve

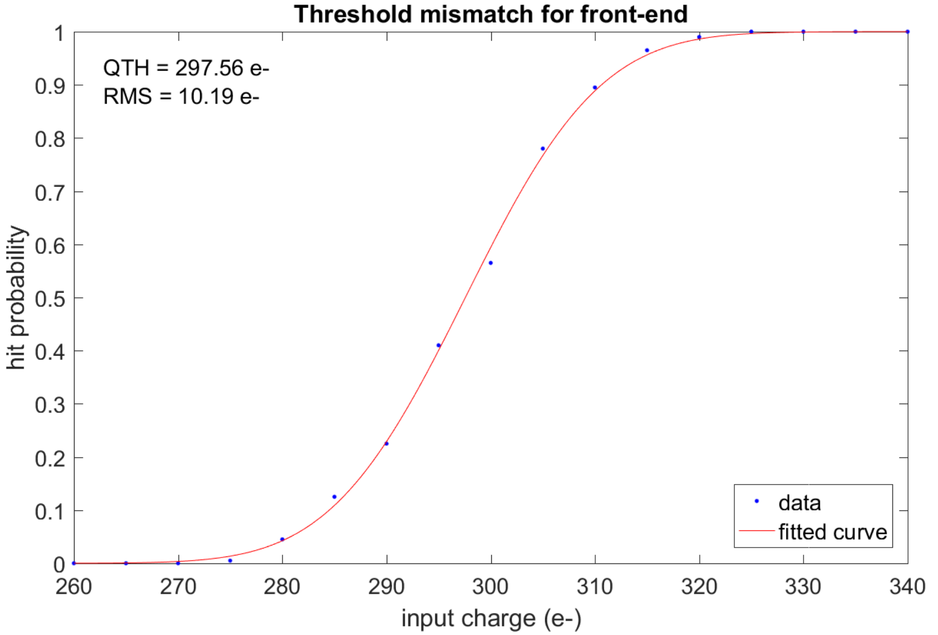
- simulated analog signals of the front-end

Noise and mismatch

- Noise and transistor mismatch cause a variation in the charge threshold of the front-end (S-curve)



threshold/noise > 10 ✓

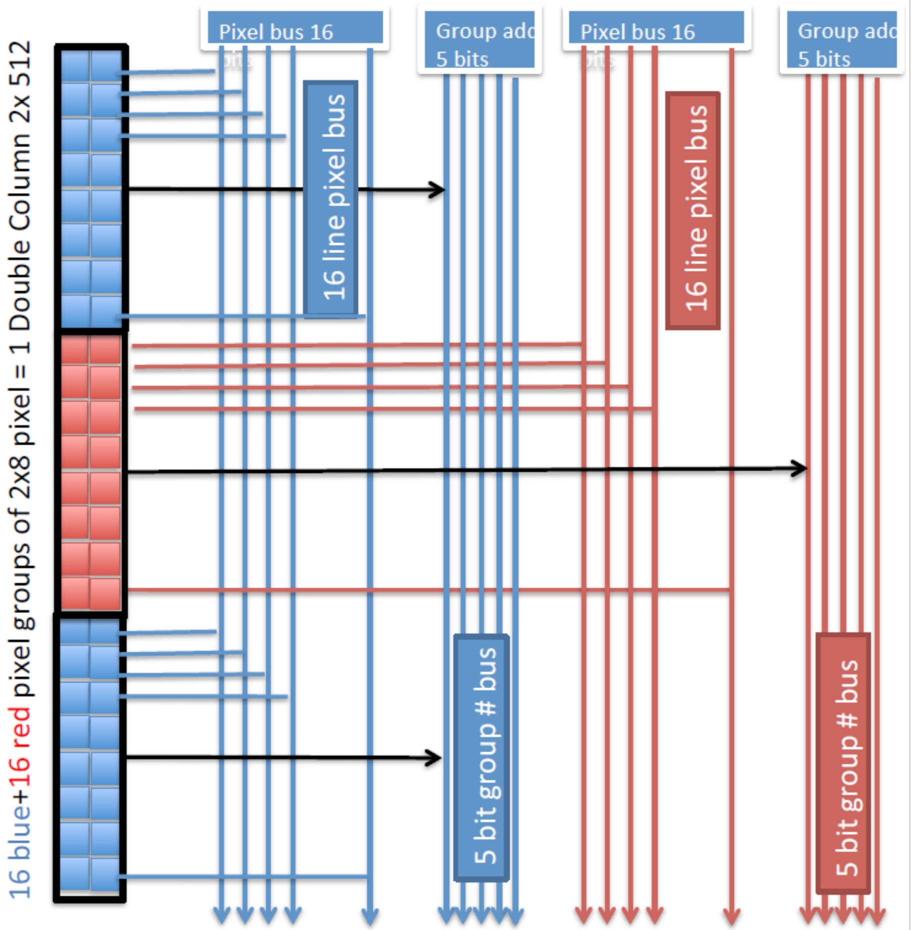


good threshold uniformity,
no need for in-pixel tuning

Digital readout architecture

- Front-end output injected into double-column digital readout logic
- Hits are stored using in-pixel flip-flops and transmitted asynchronously over high-speed buses to the end-of-column logic (digital periphery)
- No clock distribution over the active matrix – reduces power consumption!

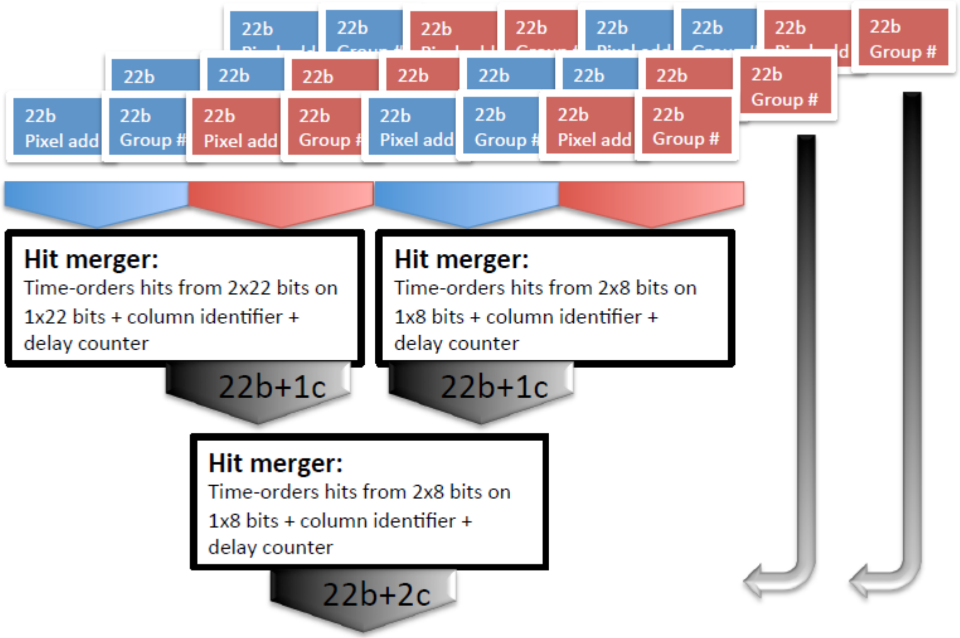
- Double-column divided into groups of 2x8 pixels (“red” and “blue”)
- Buses shared by all groups of the same colour in the double-column
- Group number encoded on 5-bit group address bus



Digital end-of-column logic

- At the periphery, signals of red and blue groups are merged together
- Simultaneous signals on two buses require additional arbitration logic (blue signal is given priority, red is delayed)
- Merging is repeated for all the double-columns and then continued until all outputs are merged into one parallel bus

x256 double-columns



Hit merger: Time-orders hits from 2x22 bits on 1x22 bits + column identifier + delay counter

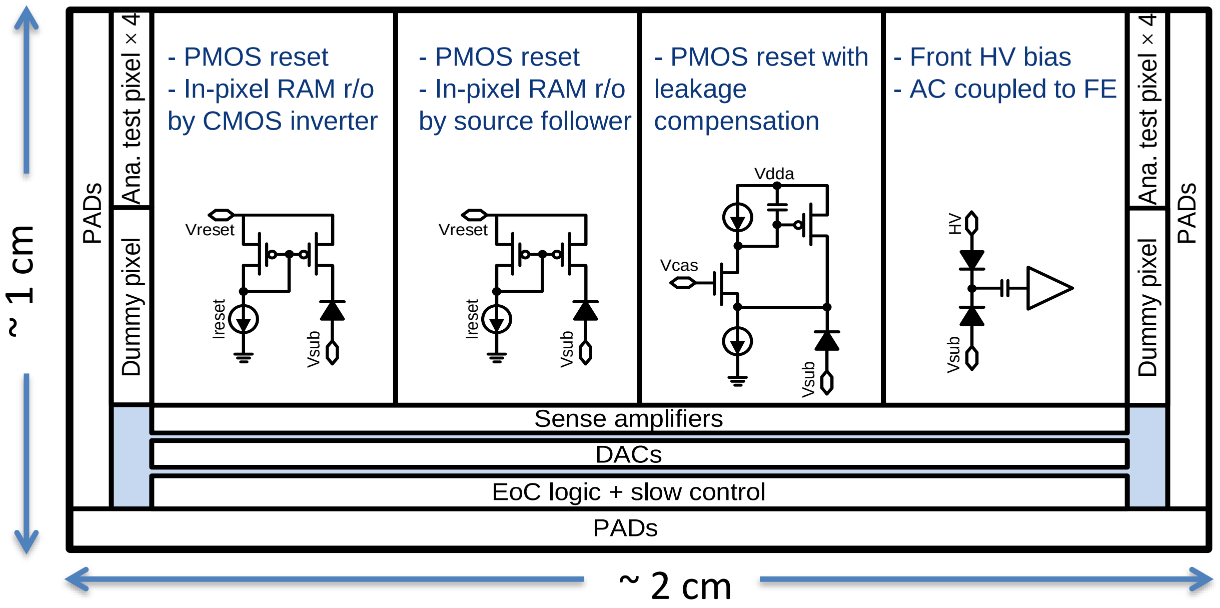
Hit merger: Time-orders hits from 2x8 bits on 1x8 bits + column identifier + delay counter

Hit merger: Time-orders hits from 2x8 bits on 1x8 bits + column identifier + delay counter

x10 levels of merging for full matrix

The "TJ-Monopix" chip

- Produced on the same reticle as the "MALTA" chip
- "MALTA" front-end modified to provide ToT information
- Well established column-drain architecture:
  - Time stamp distributed in pixel array
  - Hit information stored in the pixel
  - Hit read out following a priority scan


- PMOS reset
- In-pixel RAM r/o by CMOS inverter

- PMOS reset
- In-pixel RAM r/o by source follower

- PMOS reset with leakage compensation

- Front HV bias
- AC coupled to FE

T. Wang et al.
iWoRiD 2017

Summary

- The possibility of using a monolithic pixel sensor for the outer layers of the ATLAS experiment was investigated using the TowerJazz Investigator test chip
- Measurement results of sensors produced using a novel modified process, which combines high Q/C with radiation tolerance, show good performance and high efficiency even after irradiation
- This has opened the way for the design of two large-scale demonstrators with different readout architectures