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Monolithic Pixel Development in TowerJazz 180~nm CMOS for the outer pixel layers in the ATLAS experiment

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The upgrade of the ATLAS [1] tracking detector for the High-Luminosity Large Hadron Collider at CERN requires the development of novel radiation hard silicon sensor technologies. Latest developments in CMOS sensor processing offer the possibility of combining high-resitivity substrates with on-chip high-voltage biasing to achieve large depleted active sensor volume. We characterized depleted monolithic active pixel sensors (DMAPS), which were produced in a novel modified imaging process implemented in the TowerJazz 180nm CMOS process\footnote{manufactured by Tower Semiconductor Ltd, Israel} in the framework of the monolithic sensor development for the ALICE experiment [2]. The novel process modification [3] implemented in this technology allows full depletion of the epi layer even after substantial irradiation as expected for the ATLAS High-Luminosity LHC upgrade tracker "ITk". The required tolerance to non-ionizing energy loss (NIEL) in the outer ATLAS ITk pixel layers is 1.5×10^{15}1 MeV n_{eq}/cm^2, two orders of magnitude higher than the ALICE ITS.

The designed sensor aims to minimise the capacitive load on the amplifier and enable fast signal collection, in time for the LHC 25ns bunch spacing. Separating the collection well from digital area allows to decouple analog and digital electronics to further minimize capacitance and prevent cross-talk. The radiation hardness of the charge collection to Non Ionizing Energy Loss (NIEL) has been characterized for the different pixel sensor cell designs. The talk focuses on the charge collection properties measured in the laboratory using radioactive sources, focused X-ray beam tests and in test beams. The talk summarises results on charge collection efficiency and charge collection time measured in the lab and beam tests, local efficiency distribution in the pixel as determined in beam tests with comparisons before and after irradiation.

These results showed the significantly improved radiation hardness obtained for sensors manufactured through the modified process. Achieving these results opened the way to the design of two large scale demonstrators for the ATLAS ITk outermost pixel layers, where the expected hit rate is 0.4 to 2 MHz/mm^2. The "MALTA" chip contains a 512×512 pixel matrix of 36.4 μm pitch featuring a 1 μW frontend with in-pixel discrimination based on ALPIDE [5] with a time response $<$ 20ns. The full asynchronous readout without clock distribution over the matrix reduces digital power. The "TJ-Monopix" chip implements the same front-end as MALTA combining it with the well-established column drain architecture [6].

[1] The ATLAS Collaboration, JINST 3 (2008) S08003.

[2] G. Aglieri et al., JINST 8 (2013) C12041.

[3] W. Snoeys et al., submitted to NIMA.

[4] J. Willem van Hoorne et al., IEEE NSS/MIC 2016.

[5] D. Kim et al., JINST 12 (2016) C02042.

[6] I.Peric et al. NIMA 565 (2006) 178.

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