Characterisation of capacitively coupled HV/HR-CMOS sensor chips for the CLIC vertex detector

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Position Sensitive Detectors 11

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This work was carried out in the framework of the CLICdp collaboration

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Overview

- The CLIC vertex detector requirements
- Introduction to capacitively coupled pixel detectors
- The CLICpix Capacitively Coupled Pixel Detector (C3PD)
  - Overview of the C3PD chip
  - Submission with higher resistivity wafers
- Measurements with bare C3PD chips
- Measurements with C3PD in a capacitively coupled assembly
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  - Test pulse injection
  - Calibration using test pulses
- Outlook
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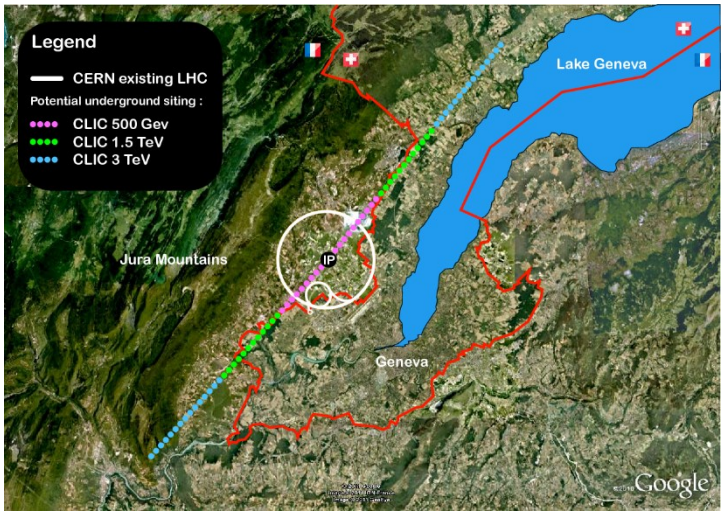
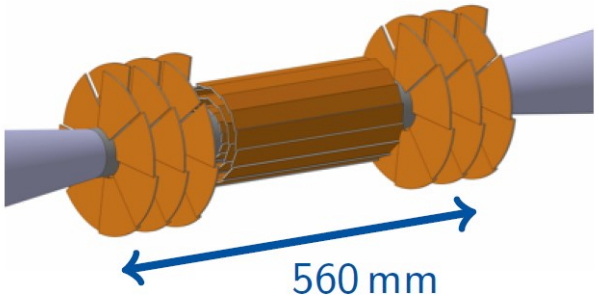
The CLIC vertex detector requirements

- The Compact Linear Collider (CLIC) is a proposed future high-energy linear e^+e^- collider

- The CLIC beam structure consists of bunch trains at a repetition rate of $50\ Hz$
  - Each bunch train consists of 312 bunch crossings separated by 0.5 ns
  - Thanks to the low duty cycle of the CLIC beam ($156\ ns/20\ ms$), a power pulsing scheme can be introduced in order to power down the main driving nodes of the front-end between subsequent bunch trains. The average power consumption over the $50\ Hz$ cycle can therefore be minimised



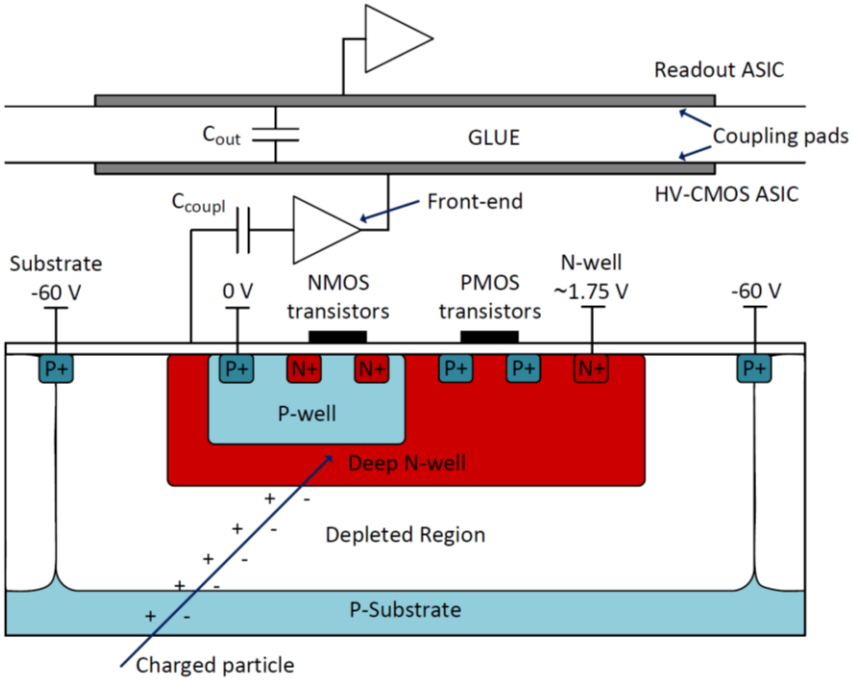
- Requirements for the CLIC vertex detector:
  - Single point resolution: $3\ \mu m$
  - Material budget: $< 0.2\%\ X_0$ per detection layer (corresponding to $100\ \mu m$ for silicon sensor and readout chip)
  - Power consumption: $< 50\ mW/cm^2$ (after power pulsing)
  - Time-stamping resolution: $10\ ns$



- The capacitive coupling between an active HV-CMOS sensor and a readout ASIC has been considered in the framework of the CLIC vertex detector study

Introduction to capacitively coupled pixel detectors

- High-Voltage (HV) CMOS sensors:
  - In a HV-CMOS device, all electronics are placed in a deep N-well, which is also the collecting electrode
  - Due to the reverse applied high-voltage bias, a depletion region with a depth of $\sim 10\ \mu m$ is created under the collection electrode, which leads to fast signal collection through drift



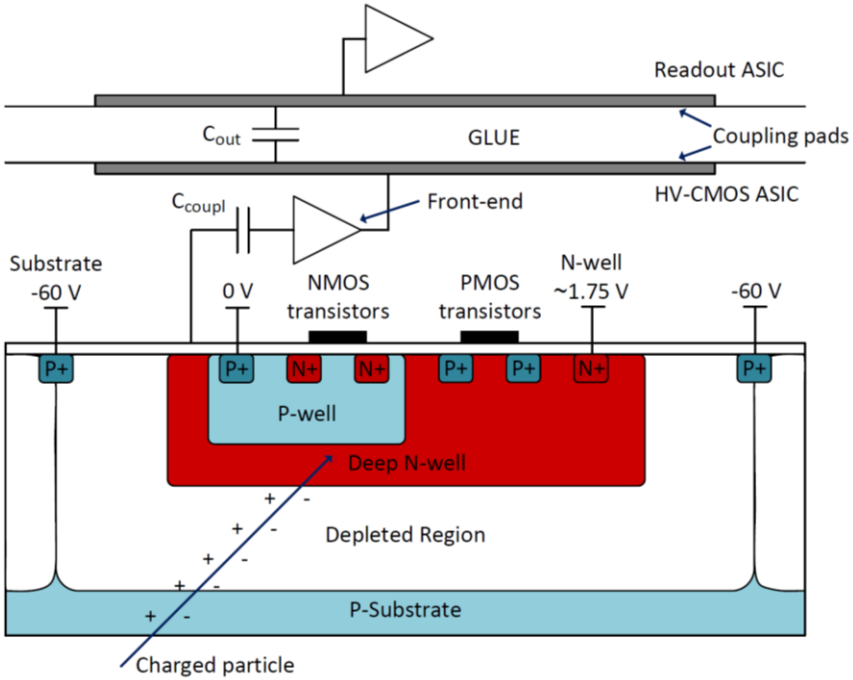
- Capacitively coupled pixel detectors:
  - A thin layer of glue is applied between the sensor and the readout chip
  - The charge collected in the HV-CMOS pixel is amplified by an on-pixel Charge Sensitive Amplifier (CSA) and then transferred to the readout chip for further processing

- Two chips have been designed in the framework of the CLIC vertex detector studies
  - The C3PD HV-CMOS sensor chip *[1]*, produced in a 180 nm HV-CMOS process, and
  - The CLICpix2 readout chip *[2]*, produced in a 65 nm CMOS process
  - Both chips are the successors of a 1st generation of chips that have been tested in capacitively coupled assemblies *[3]*
  - The matrix of each chip features 128×128 square pixels with $25\ \mu m$ pitch
  - Assemblies consisting of the C3PD HV-CMOS sensor chip and the CLICpix2 readout chip have been built in order to study the concept of capacitive coupling

Introduction to capacitively coupled pixel detectors

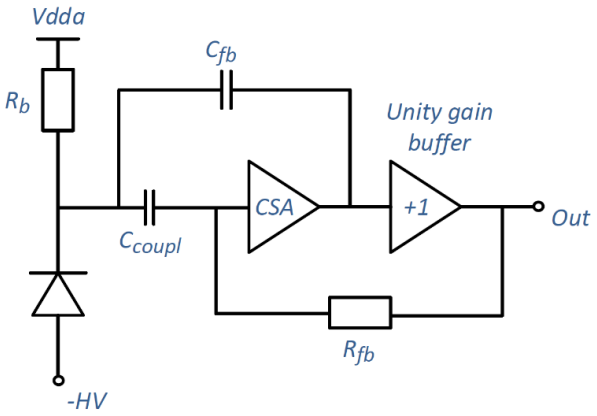
- The concept of capacitive coupling offers advantages
  - The difficulties and cost of bump-bonding the sensor to the readout chip are overcome by gluing the two chips together
  - The readout ASIC and the sensor can be separately optimised
  - The CLICpix2 has been (so far) produced with an MPW, therefore only bare dies have been received
  - Since bump-bonding bare dies at a 25 µm pitch is challenging, the option of using a capacitively coupled active sensor was conducive to test the readout chip with particles

- On the other hand, there are some drawbacks
  - The main limitation by design is that every P+ diffusion is capacitively coupled to the sensor
    - The use of PMOS transistors needs to be minimised in order to reduce unwanted signal injection
  - Complications are added at system level
    - Such assemblies require a readout system which simultaneously controls both chips
    - Complex powering/readout connections need to be introduced in order to operate the chips

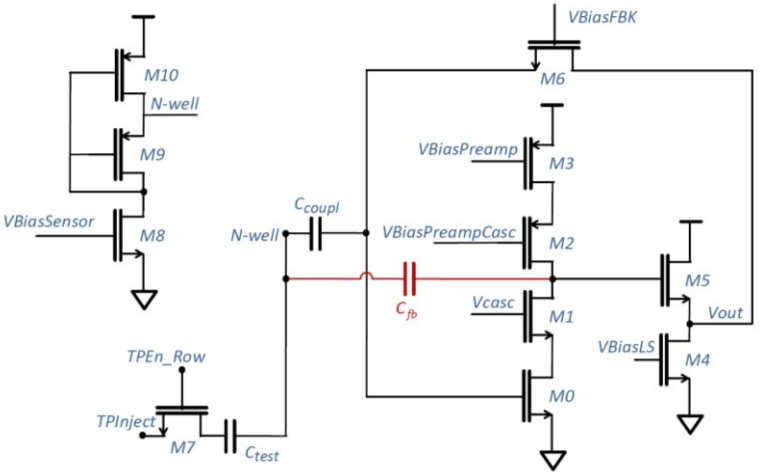


The CLICpix Capacitively Coupled Pixel Detector (C3PD)

- Active HV-CMOS sensor to be used in capacitively coupled assemblies with the CLICpix2 readout chip
  - Produced in a commercial 180 nm HV-CMOS process
  - Requirements:
    - 128×128 square pixels with $25\ \mu m$ pitch
    - Rise time: $\sim 20\ ns$
    - Charge gain: $> 120\ mV/ke^-$
    - Power consumption: $< 50\ mW/cm^2$ (both for sensor and readout chip, after power pulsing)
  - The analog front-end is based on a charge sensitive amplifier (CSA), followed by a unity gain buffer



Block diagram of the C3PD pixel



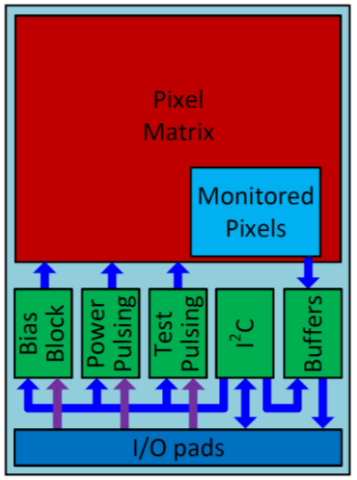
Schematic of the C3PD pixel

The CLICpix Capacitively Coupled Pixel Detector (C3PD)

- The pixel matrix is organised in double columns
  - Apart from the regular pixel, two different flavours have been implemented in the two rightmost double columns
  - One of the testing columns features a pixel with a metal-to-metal coupling capacitance (C_{coupl} in schematic) instead of CMOS gate capacitance
  - The second testing column features a pixel with a simplified scheme for biasing the sensor

- The C3PD chip interface
  - In the digital part, a standard I^2C interface is used for configuration *[4]*
  - A 3×3 cluster of pixels with their outputs multiplexed and buffered to the IOs is used in order to monitor the front-end output
  - One of the monitored pixels is used to directly monitor the injected test pulse

- Submission with higher resistivity wafers
  - C3PD sensor chips will be available on wafers with $\sim 20, 80, 200, 1000\ \Omega\text{cm}$ resistivity for the substrate
  - A layout modification took place in order to achieve a higher breakdown voltage. A higher reverse bias can then be applied to the sensor
  - The higher substrate resistivity, along with the higher applied bias are expected to be beneficial for the charge collection thanks to the larger depleted volume *[5]*
  - The expected benefits will be studied in beam tests, once the chips are available and capacitively coupled assemblies are produced



Block diagram of the C3PD chip

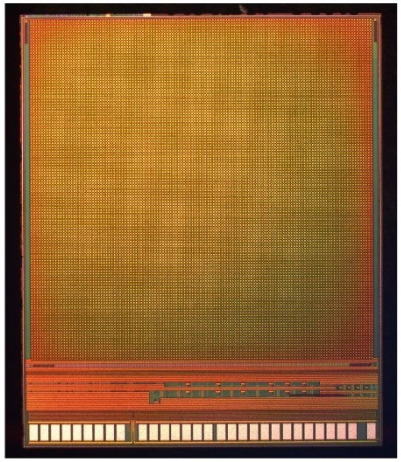


Photo: J. Alozy

Measurements with bare C3PD chips

- Before receiving assemblies with the readout chip, a standalone characterisation was performed using bare C3PD chips, as reported in *[1]*
- The chip has been tested using the internal test pulse injection, as well as with a ^{55}Fe source
- The results of the standalone test for bare chips have shown:
  - Average charge gain: $190\ mV/ke^-$
  - RMS noise: $40\ e^-$
  - Rise time: $20\ ns$
  - Power consumption: $\sim 5\mu W$ per pixel (before power pulsing)
  - After power pulsing, the average power consumption over the $50\ Hz$ cycle was estimated to be $\sim 16\ mW/cm^2$
  - These results are close to the ones expected from simulations, and are within the detector requirements
- Samples thinned down to $50\ \mu m$ have been tested, apart from the standard thickness ($250\ \mu m$)
  - No impact on the chip performance has been observed for the thinned-down samples

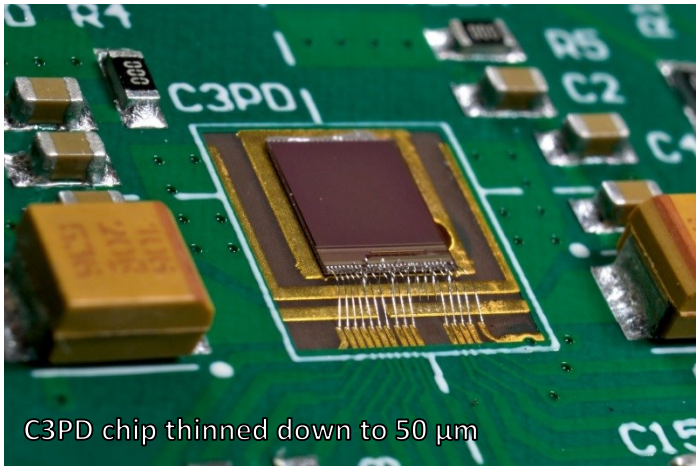
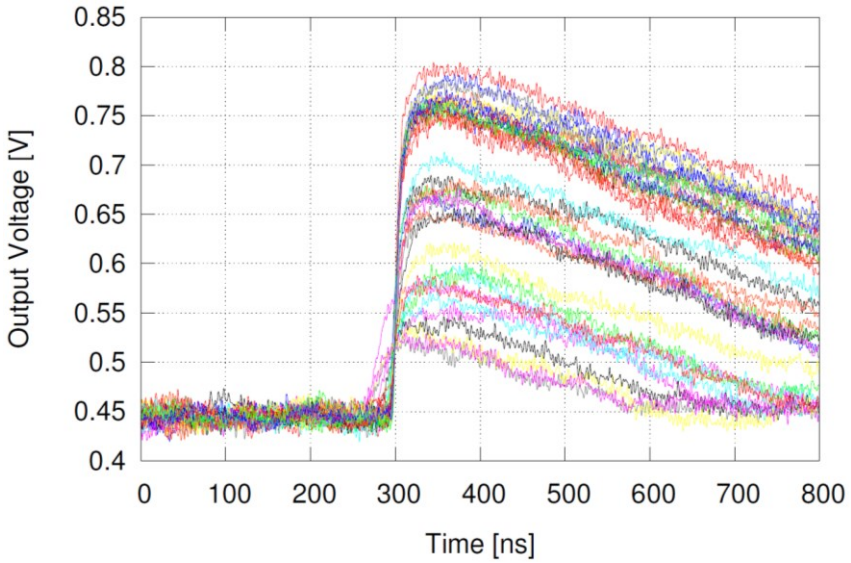
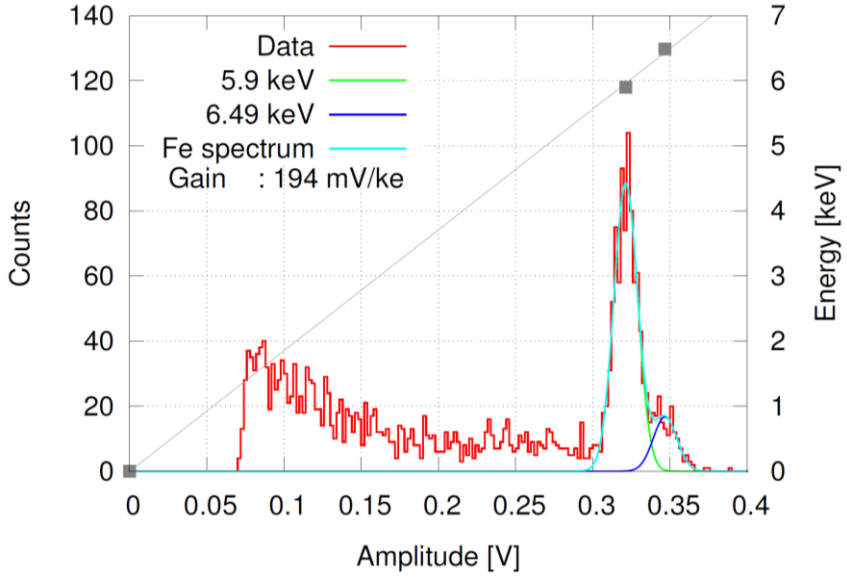


Photo: S. Kulis

Measurements with bare C3PD chips

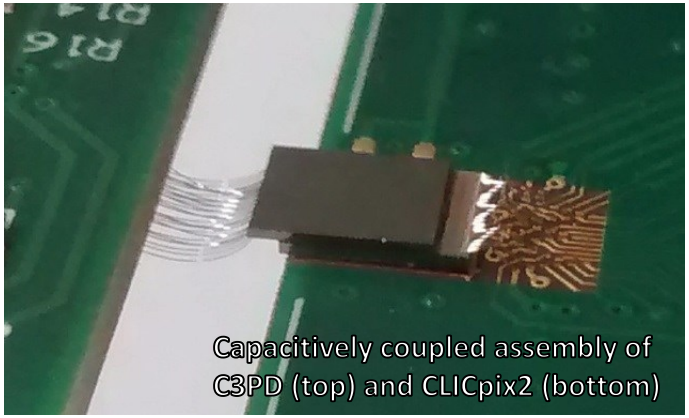
- Measurements with a ^{55}Fe source for one of the monitored pixels
  - Sample pulses (left) and
  - Resulting amplitude spectrum (right)





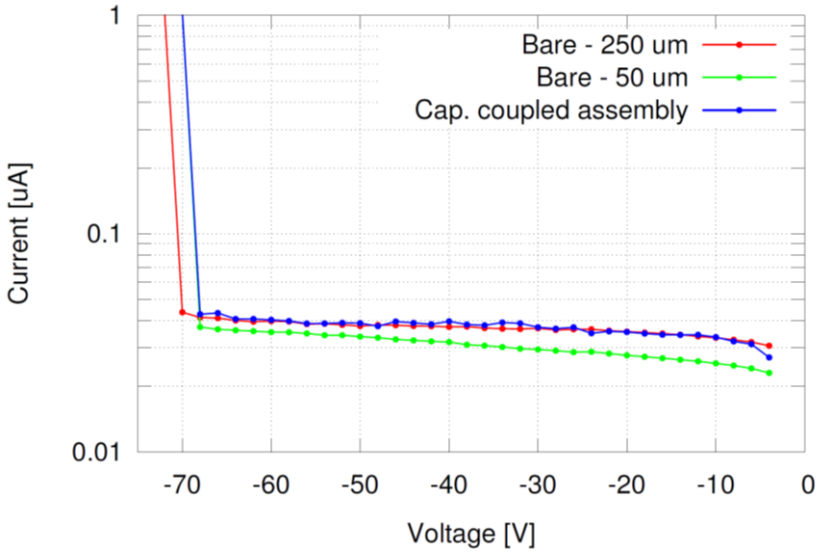
CLICpix2 and C3PD assembly

- Assemblies with the C3PD HV-CMOS sensor capacitively coupled to the CLICpix2 readout chip have been produced
- The chips are mounted and wire-bonded on a custom designed PCB, which is then connected to the CaRIBOu data acquisition system *[6]*
- Measurements on C3PD where performed with both the sensor and the readout chip operating in continuous power mode
- It was challenging to illuminate the C3PD pixels using the ^{55}Fe source, as the X-rays from the ^{55}Fe source do not have enough energy to penetrate through the backside of the sensor into the depleted region
  - Charge injection tests were therefore performed using the C3PD internal test pulse injection

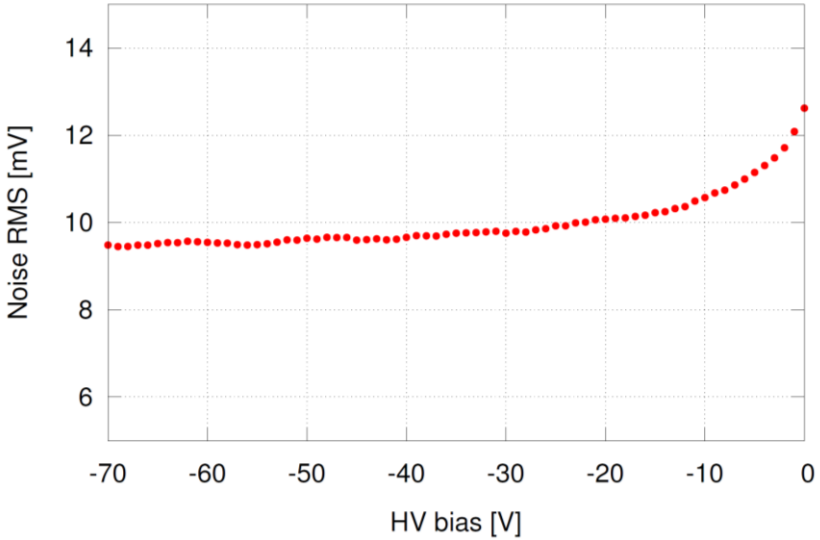

Capacitively coupled assembly of C3PD (top) and CLICpix2 (bottom)

I-V characteristic

- The sensor leakage current was measured as a function of the applied HV bias
  - Both the sensor and the readout ASICs were powered on during this measurement
  - At nominal bias of $-60\ V$: $I_{leak} \cong 40\ nA$ (measured for the full chip, at room temperature)
  - Breakdown voltage: $-70\ V$
- The noise at the output of one of the monitored pixels was also measured as a function of the HV bias
  - Noise is minimised for a bias $< -40\ V$



Leakage current as a function of the HV bias

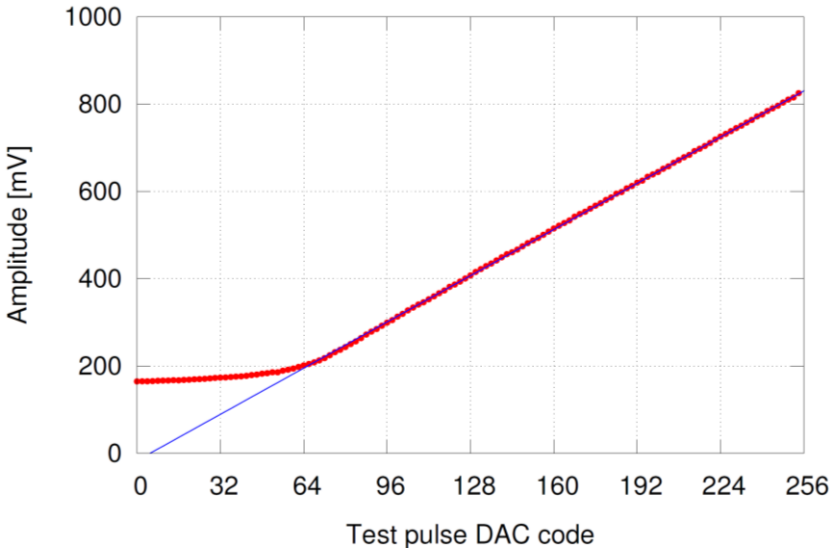


Noise at the amplifier output as a function of the HV bias

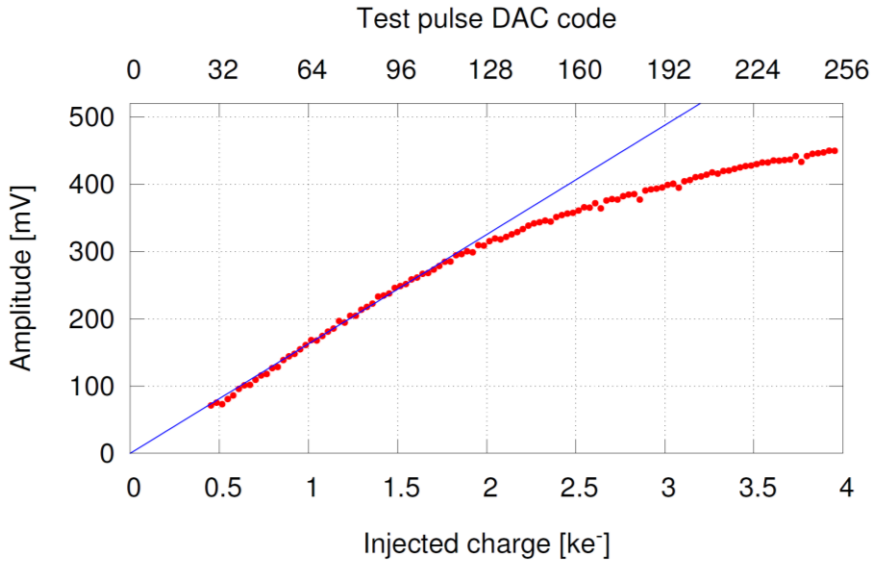
Internal test pulse injection

- The injected test pulse voltage was measured as a function of the DAC code, using the C3PD pixel with direct monitoring of the test pulse (left)

- The output amplitude was measured as a function of the injected test pulse DAC code (right)
  - The injected charge was calculated using the design value ($0.8\ fF$) for the test pulse injection capacitance (C_{test})
  - The amplifier is linear for injected charges up to $\sim 1.7\ ke^-$ (a linearity for injected charges up to $2\ ke^-$ was expected from simulations)



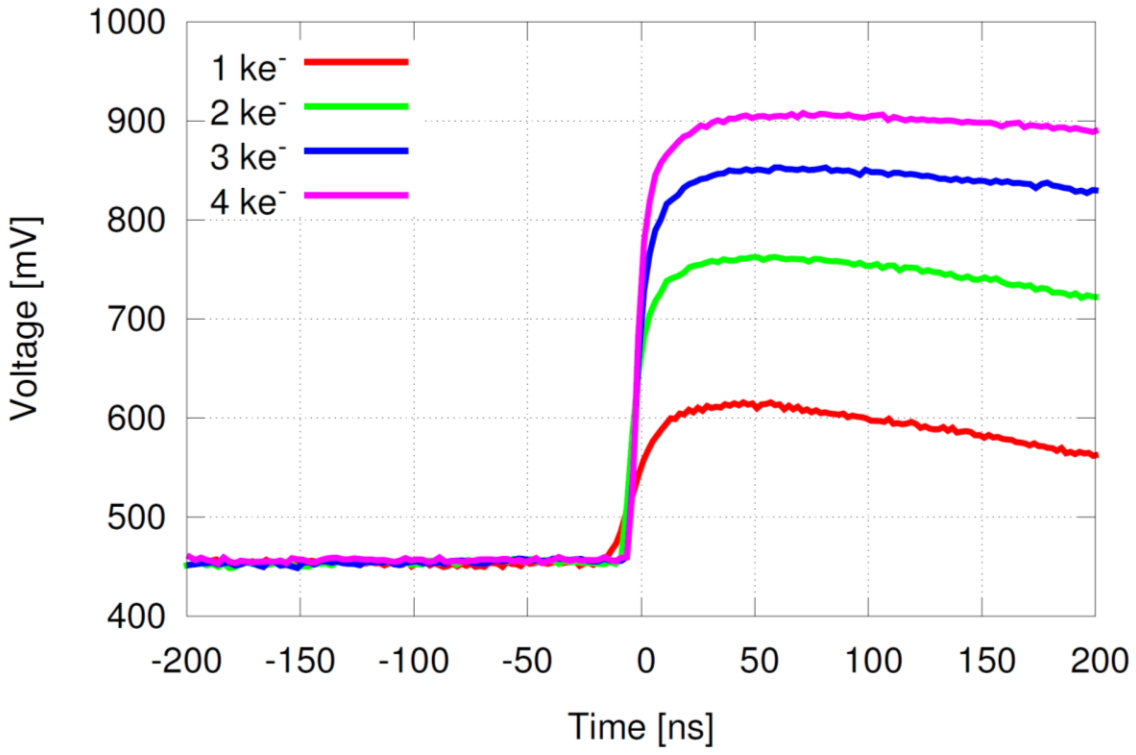
Measured amplitude of the injected test pulse as a function of the test pulse DAC code



Measured amplitude at the amplifier output as a function of the injected test pulse

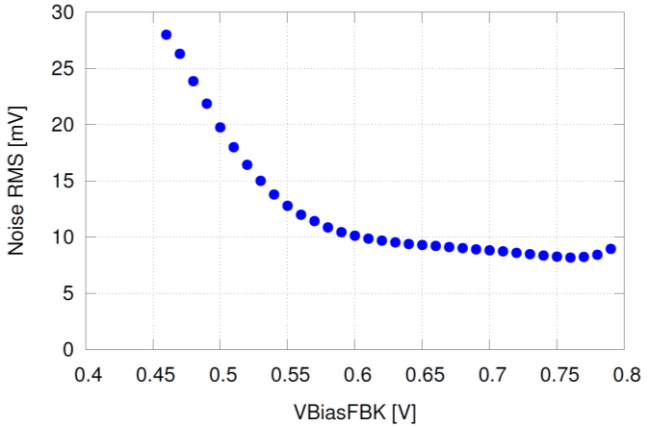
Internal test pulse injection

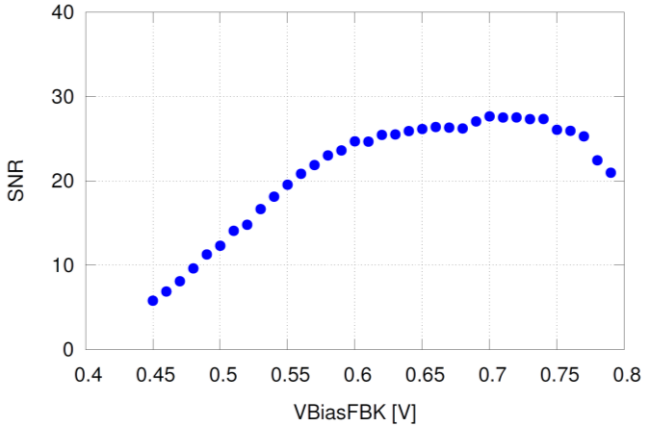
- Output pulse of the C3PD amplifier for different charges injected using the internal test pulse:
  - Rise time $\sim 20\ ns$
  - Slow return to baseline



Calibration using test pulses

- Key parameters of the C3PD front-end were measured as a function of the biasing of different nodes
  - These scans were used in order to optimise the operating point of C3PD for the capacitively coupled assembly
  - As an example, plots of the measured RMS noise (left) and SNR (right) as a function of the feedback biasing (transistor M6 in slide 5 schematic) are presented
  - The SNR was measured with an injected charge of $\sim 1.63 ke^-$ (using internal test pulse)

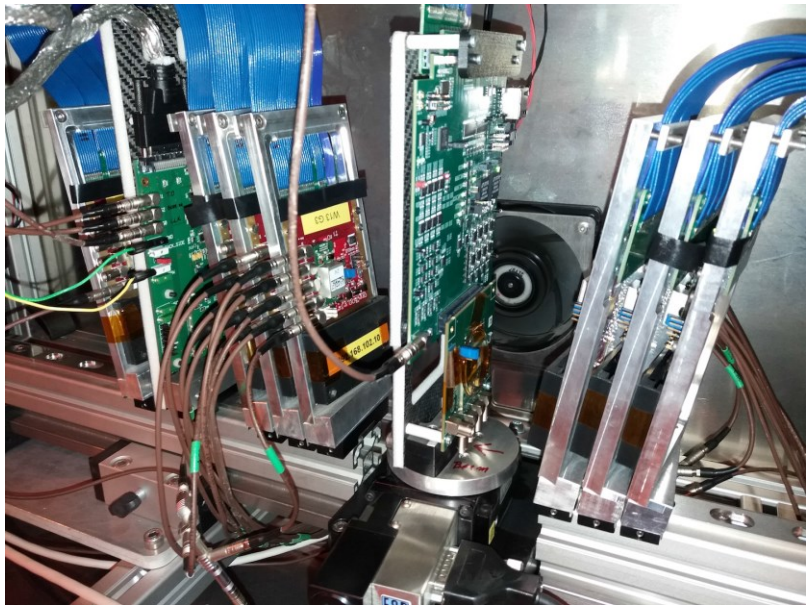




- The operating point was selected such that the maximum Signal-to-Noise Ratio is achieved, while keeping a fast rise time ($\sim 20\ ns$)
  - For the selected operating point the average output amplitude was measured to be $278\ mV$, the RMS noise $7\ mV$ and the rise time $17.6\ ns$
  - Power consumption: $\sim 5\ \mu W$ per pixel during 'power-on', and $\sim 95\ nW$ per pixel during 'power-off'
  - The average power consumption over the $50\ Hz$ cycle of the CLIC beam was estimated to be $\sim 16\ mW/cm^2$ (assuming a $30\ \mu s/20\ ms$ duty cycle)

Outlook

- The functionality of both the HV-CMOS sensor and the readout chip has been tested in standalone mode
  - Testing both chips in capacitively coupled assemblies is in progress
- Further testing to be performed using capacitively coupled assemblies
  - Using the readout chip testing of C3PD will not be restricted to a limited number of monitored pixels
  - Pixel-to-pixel mismatch, top-down effects and homogeneity across the pixel matrix will be studied
  - C3PD samples with higher resistivity wafers ($\sim 20, 80, 200$ & $1000\ \Omega\mathrm{cm}$) are expected to be available soon
  - Testing of the higher resistivity sensor chips will be performed using future capacitively coupled assemblies



Test beam setup (Photo: A. Nurnberg)

Summary and conclusions

- The CLICpix Capacitively Coupled Pixel Detector (C3PD) is a HV-CMOS sensor designed to be used in capacitively coupled assemblies with the CLICpix2 readout chip in the context of the CLIC vertex detector R&D
- Bare C3PD chips, as well as chips in capacitively coupled assemblies have been tested in standalone mode. The observed performance is close to the one expected from simulations and matches the detector requirements
- The average power consumption of $16\ mW/cm^2$ gives enough margin for the readout chip, in view of the $50\ mW/cm^2$ required for the capacitively coupled assemblies
- Samples thinned down to $50\ \mu m$ have been tested, without any observed impact on the sensor performance
- A version of C3PD with higher resistivity wafers ($\sim 20, 80, 200\ \&\ 1000\ \Omega\mathrm{cm}$) has been submitted and samples are expected to be available soon
- Capacitively coupled assemblies with the readout chip will be characterised over laboratory measurements and beam tests

References

[1] *I. Kremastiotis et al: Design and standalone characterisation of a capacitively coupled HV-CMOS sensor for the CLIC vertex detector (2017),* *https://arxiv.org/pdf/1706.04470.pdf*

[2] *E. Santin, P. Valerio and A. Fiergolski: CLICpix2 User's Manual (2016)*

[3] *N. Alipour Tehrani et al., Capacitively coupled hybrid pixel assemblies for the CLIC vertex detector (2016)* *https://doi.org/10.1016/j.nima.2016.03.072*

[4] *S. Kulis and A. Fiergolski: C3PD-sc – A slow control interface for C3PD chip (2016)*

[5] *M. Buckland: TCAD simulations of High-Voltage-CMOS Pixel structures for the CLIC vertex detector (2016),* *https://cds.cern.ch/record/2159671/*

[6] *A. Fiergolski: A multi-chip data acquisition system based on a heterogeneous system-on-chip platform (2017),* *https://cds.cern.ch/record/2272077/*