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Characterisation of capacitively coupled HV/HR-CMOS sensor chips for the CLIC vertex detector

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The capacitive coupling between an active sensor and a readout ASIC has been considered in the framework of the CLIC vertex detector study. The CLICpix Capacitively Coupled Pixel Detector (C3PD) is a High-Voltage CMOS sensor chip produced in a commercial 180 nm HV-CMOS process for this purpose. The sensor was designed to be connected to the CLICpix2 readout chip. It therefore matches the dimensions of the readout chip, featuring a matrix of 128×128 square pixels with $25 \mu\text{m}$ pitch. The sensor chip has been produced with the standard value for the substrate resistivity (of $\sim 20 \Omega\text{cm}$) and characterised in standalone testing mode, before receiving and testing capacitively coupled assemblies. The standalone measurement results show a rise time of $\sim 20 \text{ ns}$ for a power consumption of $2.7 \mu\text{A}/\text{pixel}$.

Following the successful characterisation of the C3PD ASICs produced with the standard substrate resistivity a second submission took place, with higher substrate resistivity wafers ($\sim 20, 80, 200,$ and $1000 \Omega\text{cm}$). The higher resistivity, along with a layout modification done in order to achieve a higher breakdown voltage, are expected to have beneficial results on the sensor performance. A comparison of the performance of the sensor with different substrate resistivities will be presented.

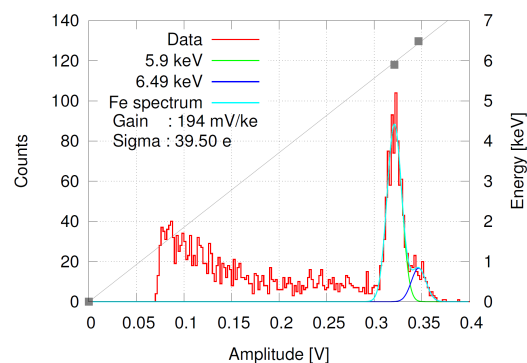
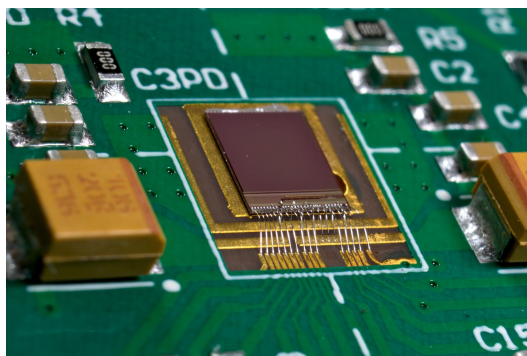


Figure 1: C3PD ASIC and measured ^{55}Fe spectrum.

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