

ILC SiW-ECAL開発 現状

Taikan Suehara (Kyushu University)

※ すみません。ほぼ既存のスライドをかき集めただけです

ILD 測定器





- 崩壊点検出器 (VTX)
 CMOS, FPCCD, ...
- シリコン飛跡検出器
 - SIT, SET
- 中央飛跡検出器 (TPC)
- 電磁カロリメータ (Si/Sc)
- ハドロンカロリメータ
- ・ ミューオン検出器
- 前方検出器

シリコン電磁カロリメータ (ILD)









20-30層 内径1.4-1.8m

4 x 9 x 5 x 30 x 8 x 5 = 216000 (max.)

Sensor studies



To avoid ring events from guard rings, we tested several guard-ring structures using 3x3 or 4x4 pixels baby sensors and infrared laser

(Floating) guard ring structures

Sensor w/ 5.5 x 5.5 mm² cells No GR 1 GR Split GR (2/4 GR)





Ring crosstalk seen only with GR 0 GR big sensor produced, will be tested Taikan Suehara, 19 Mar. 2017 page 4

Leakage current 0 GR

センサー: これまでのstudy

- (floating)ガードリングの効果
- ・ガードリングなしのセンサーの特性
- 放射線耐性
- PSDサンプル



Ring crosstalk with laser seen only with GR

I/V curve at the edge pixels



Cut size B is preferred; 500 μ m is OK with cut size B

Compared with lower R sensor



Slightly lower leakage current seen in new sensor (breakdown voltage lower, but this has sample dependence)

I/V curve at the center pixels



500 μm have ~3 times higher current, no difference on B/C

Statistics

Dark current comparison at 120V



Neutron irradiation tests



Irradiation of neutrons on baby sensor Increase on dark current is acceptable considering ILC-1 TeV 10 year radiation dose estimation



Gamma irradiation: Setup

- Facility & source
 - Gamma from 60Co, 82.3 TBq, Kyushu University
- Sensor: 500 μ m, 4 GR, 3 x 3 baby
- Irradiation (too big for ILC detectors)
 - 1.1 kGy, no voltage applied during irradiation
 - 10.2 kGy, no voltage
 - 10.2 kGy, 100 V applied during irradiation (4 hours)







Dark current



Current during irradiation (including current from gamma energy deposit)



Dark current after irradiation

- No big difference on voltage
- Damage not proportional? (maybe sample dependence)
- 10 kGy damage almost consistent with displacement

C/V characteristics



No big difference in capacitance Strange shape seen \sim 10 V after irradiation

Detector module



SKIROC2



Diagram of analog part of SKIROC2

SKIROC2



64 ch / chip 15 analog memories / ch with 12 bit BX counting by BX clock 12 bit ADC (G1 and G10) Internal trigger (1BX shift seen) Power pulsing TDC (large noise) within one BX External trigger (not working)

ADC test

12 bit-ADC Ramp

Diagram of analog part of SKIROC2

SKIROC2/2A testboard

Analog probe

HHHH

()

/OMEGA/KYUSYU-U/HANO CALLIER/T.SUEHARA/T.KUWANA



With soldered SKIROC2A (Thanks to OMEGA)

Connector for detector connection



BGA400 socket SKIROC2/2A

186

VI1 VI2 VI4 WI5 WI8 R173 R175 R175 R174 R175 R175 R185 R174 R187 R190

Test pulse in

GND 😡

DIF interface Taikan Suehara, 19 Mar. 2017 page 17

lacksquare

R149 R150 R151 R152 R153 R154 R155 R156 R157 R158 R159 R160 R161 R162 R163 R164 R165 R166 Slow clock in

Control PP/TDC etc.

USB readout

Readout and DAQ

| ixed Test: S-Curve (Threshold) all Ch. Ana | logue Test: DAC | Analogue Test: DC | External ADC | Internal ADC calib | Hold scan | w. DAQ | Digital ASIC Debug / DAQ | |
|---|--|--|---|--|--|---|--|--|
| tup Slow Control 1 Slow Control 2 | Probe, SCA Read | FPGA Configuration | Info SKIROC2 | Info pcb1011 I/O | Info pcb1011 | Test Mix | ed Test: S-Curve (Threshold) | |
| tup Slow Control 1 Slow Control 2 Probe, SCA Read FPGA Co Transmit Slow Control Save Slow Control -> File Reset Slow Control File -> Load Slow Control Slow Control Register Correlation Test Chip Global Configuration Feedback Capacitance Compensation Capacitance 6.0pF ⊂ 6pF (1pF-2pF+3pF) ⊂ Chip ID Fast Shaper (time) Trigger Delay | | FIGA Configuration | Info SKIROC2 Info External Communication Enable Select Digital Inputs Sel Trig Ext Trig Ixt Trig Ixt ASIC command Set Start_rampADC_ext ASIC command Set Start_rampADC_ext Set Start_rampADC_ext Set Start_rampADC_ext Set Start_rampADC_ext Set Start_randout Set Start_randout Start_ReadOut Start_ReadOut Silow Shaper Gain 1 Enable power on Fast Shaper Enable power on Fast Shaper Enable power on Fast DAC Information Start DAC | | fo pcb10111/0 Info pcb1011 Select Analogue Input[Sel: ADC Test ScA Select Digital Output[Sel: End, ReadOut] Power Mod Shaper Gain 10 nable power on ap nable power on ap able power on ap ble power on ble power on ble power on ap ble power on ble power | | Test Mixed Test: S-Curve (Threshold) Enable Open Collector Digital Outputs EN: OC Trig_Out EN: OC ChipSat OransmitOn1 EN: OC Dout1 OransmitOn1 EN: OC Dout1 EN: OC TransmitOn2 EN: OC Dout2 TransmitOn2b Dout2b EN: OC TransmitOn2 EN: OC Dout2 TransmitOn2b Dout2b EN: OC TransmitOn2 EN: OC Dout2 Enter Substance Fain 10 Power pulsing (A) Power pulsing (A) Free Bandgap Pulsing (A) Power pulsing (AC) 10-bit dual DAC | |
| DACO: Trigger DACI: Gain Select SCA sel | ection SCA bias as annel A 0 GS ed am | Trigger (Sain Sele Enal Gain Sele Enal SCA @ Enal Output (@ Enal | biscri Discri Discri di power on di power | belay Trigger Enable power on MC Discri Enable power on MC Camp Enable power on Sackup SCA Enable power on Probe OTA Enable power on Probe OTA | Trigger Dis Power Gain Selec Power TDC Ramp Power SCA Power Output OT Power | scri pulsing (A) t Discri pulsing (ADC) pulsing (ADC) pulsing (DAC) Aq pulsing (ADC) | Power pulsing (APC) Power pulsing (APC) ADC Discri Power pulsing (ADC) ADC Ramp Power pulsing (ADC) Backup SCA Power pulsing (DAC) Probe 0TA Power pulsing (ADC) | |

C++ DAQ (original)

- Based on labview DAQ • (snip of source diagram)
- **DIF-compatible output** • (raw2root process-able)

| Procedure | | reg. | bit |
|--------------------|----|-------|-----|
| ASIC reset | WC | 1 | 2 |
| Start acq. | W | 2 | 0 |
| (200 ms wait) | | | |
| Stop acq. | С | 2 | 0 |
| Start readout | WC | 2 | 2 |
| Wait readout | R | 4 | 3 |
| (wait till bit on) | | | |
| Obtain # bytes | R | 13,14 | |
| Obtain data | Rn | 15 | |

(ported to Linux)

- Initialization ۲
- Slow control ٠
- Analog probe •

Taikan Suehara, 21 Mar. 2017 page 18

Out_SS1

Out SS10

Out FSB

Threshold

Power pulsing in testboard





One of power lines can be controlled from outside (this time Analog is tested)

Slow clock will be provided Problem: readout also depends on the clock: slow down due to inactive 99.5% of time

Start of slow clock delayed several ms from power_on_a



~ 3 ms delay is needed to ensure typical gain in PP

Next BX is affected (triggered & negative shift)



Fast shaper & triggering @SKIROC2,2A



Fast shaper@SKIROC2,2A

Soldered version (SKIROC2A)

All 64ch s-curve @SKIROC2A

| channel | Gain | width @ 1MIP | S/N |
|---------|-------|-----------------|-------|
| 10 | 86.12 | 5.46 | 15.76 |
| 39 | 87.58 | 5.29 | 16.58 |
| 63 | 86.79 | 5.64 | 15.38 |



Individual trigger threshold is checked: dynamic range of 13 DAC

feedback capacitance: 1.2 pF compensation capacitance: 6 pF

Slightly better than socket version (result should be confirmed)

SKIROC2A ch10&ch39&ch63 threshold





Time measurement with TDC on SKIROC2A



Packaging & PCB



In the second tech. prototype, we used BGA400 for package • Smaller footprint • Availability of

thinner package is better

Another form: Chip On Board



Non-packaged chips with direct wire-bonding to PCBs Much thinner than packaged PCB More fragile / sensitive to outside noise





S-Curve with 5 MIP charge injection

Better flatness needed to glue sensors Taikan Suehara, 19 Mar. 2017 page 26

Assembly

Gluing robot was developed for room-temperature conductive glue between sensors and PCBs (to avoid bending by heat)



Assembly procedure of the slabs is prepared





Readout Electronics



Si DIFs

HDMI GDCC/LDA — Si CCC



ethernet

Clock Acquisition cycle

Busy

PC (calicoes)

Start/stop acquisition Run number

Second Tech. Prototype

- 2 x 2 sensor / unit, 16 BGA ASICs
- Assembled from 2015
- New version of readout hardware (GDCC) and software (new CALICOES)



Going to test beam...

Test beam at CERN SPS 2015

Si

Three layers of second tech. prototype was on CERN SPS and tested with 10-150 GeV electrons, pions, and muons Temporary connection

between sensor PCB and adapter to DAQ

DIF 1



Signal-to-noise ratio



Higher gain with 1.2 pF feedback cap. (nominal: 6.0pF)

S/N 15-20 obtained on most of channels

OK for 0.5 MIP threshold with practically no noise

Analysis is still ongoing, more to come...

Test beams

12 D1

1st test beam of 2nd tech. proto. Nov. 2015





Retrigger and pedestal shift seen in 1st TB



Square event seen in 1st TB

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Position Sensitive Detector





Multiple electrodes in one cell to obtain particle position Popular technique in laser optics

First PSDs arrived Measurement will be done with testboard readout within FY2016

- Linearity / Stability (laser)
- Position resolution (cosmic?)



First PSD sample in Kyushu meshed (left) and unmeshed 8 mm one side, 1 mm electrodes

PSD赤外線レーザ測定



1064 nm パルスYAGレーザ



PSD保持具 preampにつなぐ レーザ入射用の十字切り欠きあり

Two types of PSD



レーザによる位置ゆがみ測定

§.05



メッシュありの結果

電極を工夫して歪みを減らす 必要がある ダイナミックレンジが課題 本質的には、ノイズで制約 → avalancheに期待



recx:recy



メッシュなしの結果 Taikan Suehara, 19 Mar. 2017 page 35



- Sensor study
 - 大量試験
 - コストダウン
 - 8インチ化?
- Electronics
 - ASIC/PCBの問題解決
 - 国内生産・改良
 - フルレイヤ(20~30層)ビーム試験
- PSD
 - アバランシェゲイン付きセンサーのテスト