CE Installation and QC

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representing the CE team

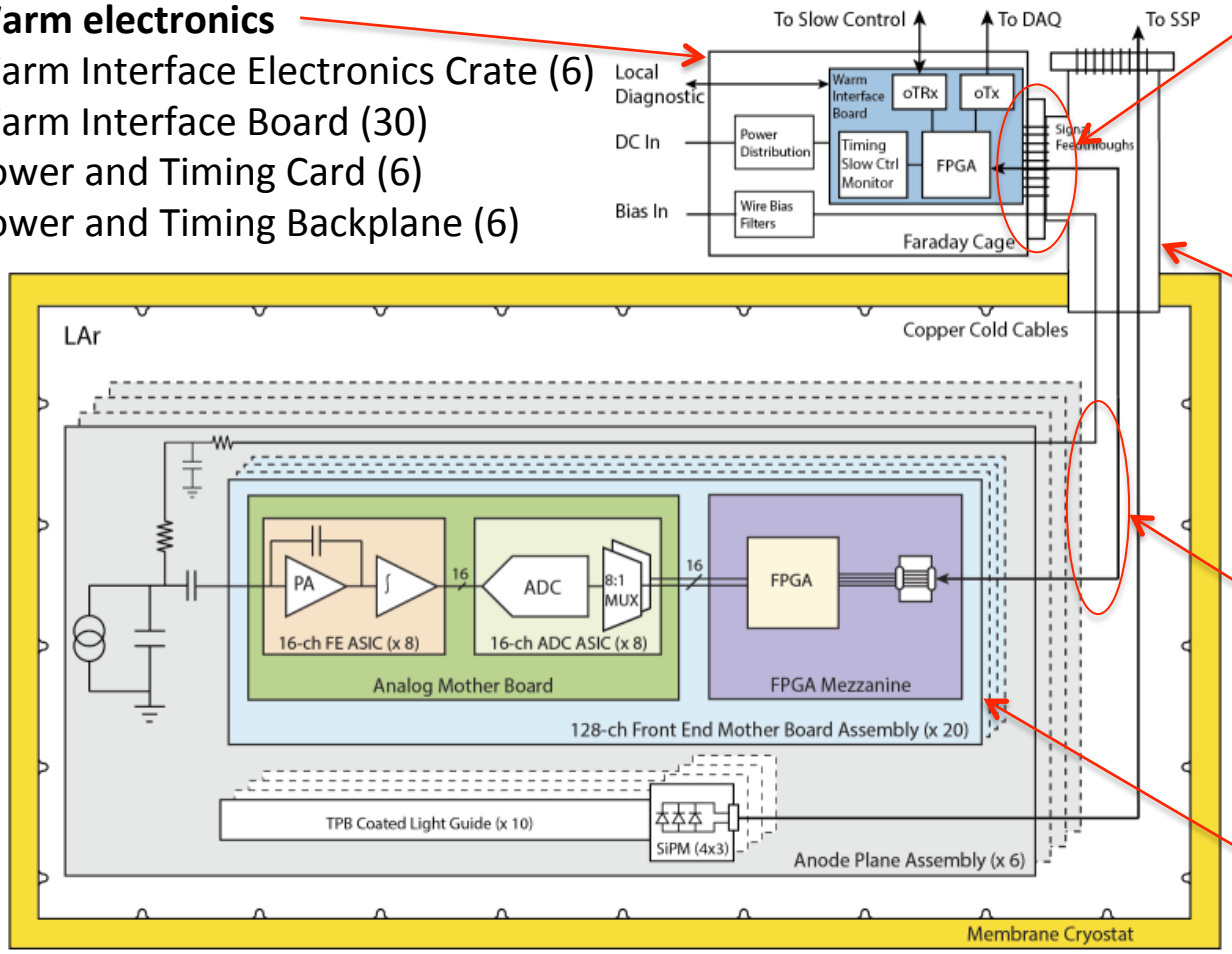
ProtoDUNE Single Phase Installation Workshop
April 20, 2017

Outline

- CE overview and current status
- Milestones and schedule
- Installation and QC on APAs
- Signal feed-through installation
- Installation and QC inside the cryostat
- CE installation team
- Summary

ProtoDUNE-SP Cold Electronics

Warm electronics
Warm Interface Electronics Crate (6)
Warm Interface Board (30)
Power and Timing Card (6)
Power and Timing Backplane (6)



CE flange
Flange assembly with cable strain relief and flange PCB for cable/WIB connection (6)

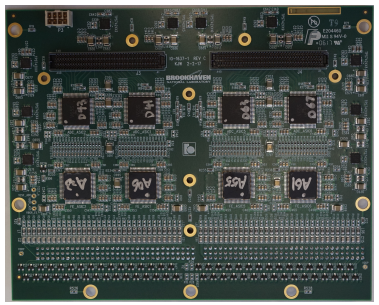
Signal feed-through
Tee pipe with 14” Conflat flanges and crossing tube cable (CTC) support (6)

Cold cable to FEMB
LV and data cable (120+120) and APA wire-bias SHV cable (48)

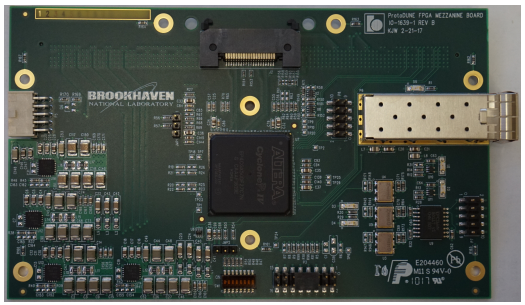
Front End Motherboard
(FEMB) 128 channels of digitized wire readout enclosed in CE Box (120)

FEMB and Cold Cable Status

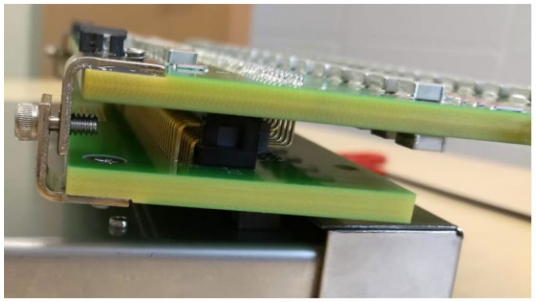
- 3 P2 FEMB (with P2 FE/P1 ADC) have been delivered to BNL
  - Test results on BNL 40% APA teststand being finalized for CE electricals PRR on May 3rd
- 280 P2 FE and 400 P1 ADC ASICs from January MPW submission expected in early May for APA1 FEMB
- Production mask set of at least 3000 each of P2 FE and P1 ADC ASIC expected in early June
- First 50 cold data bundles by end of May (150 cold LV bundles in April)
  - Fabrication for all remaining cold data cable has been ordered
- 3 final prototype CE Boxes available by end of April
  - 1 prototype CE box tested for cable strain relief in LN2 and mechanical assembly with PSL adapter and CR board
  - Fabrication of all CE Boxes will be ordered in early May with 4 week lead time



P2 analog motherboard



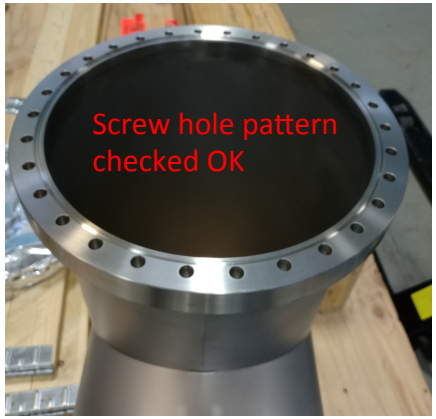
P2 FPGA mezzanine

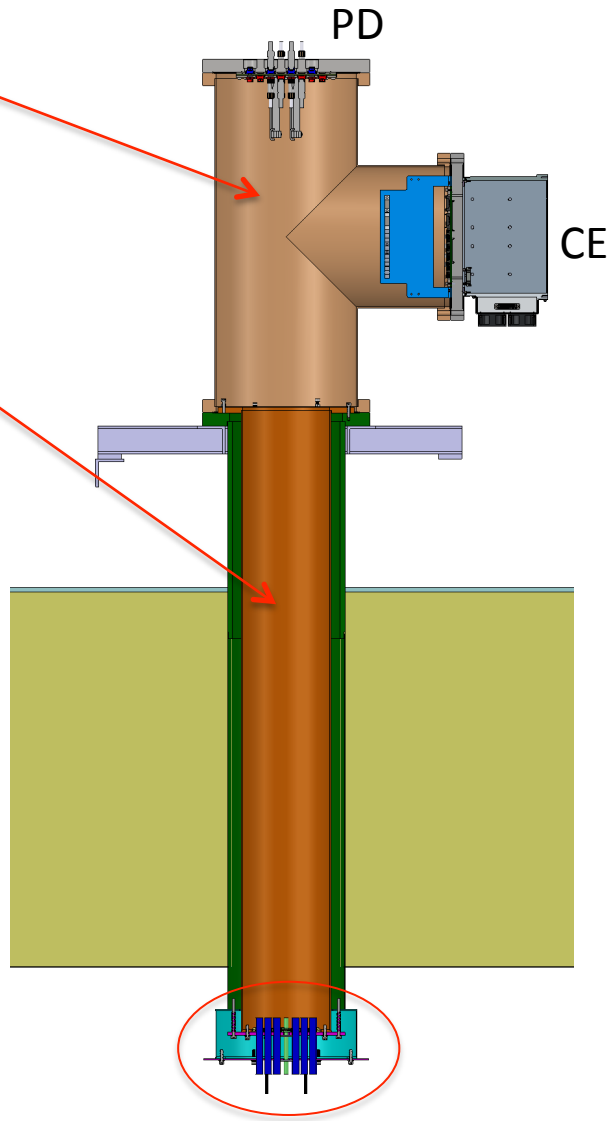


Top to bottom: CR board, PSL adapter, CE Box

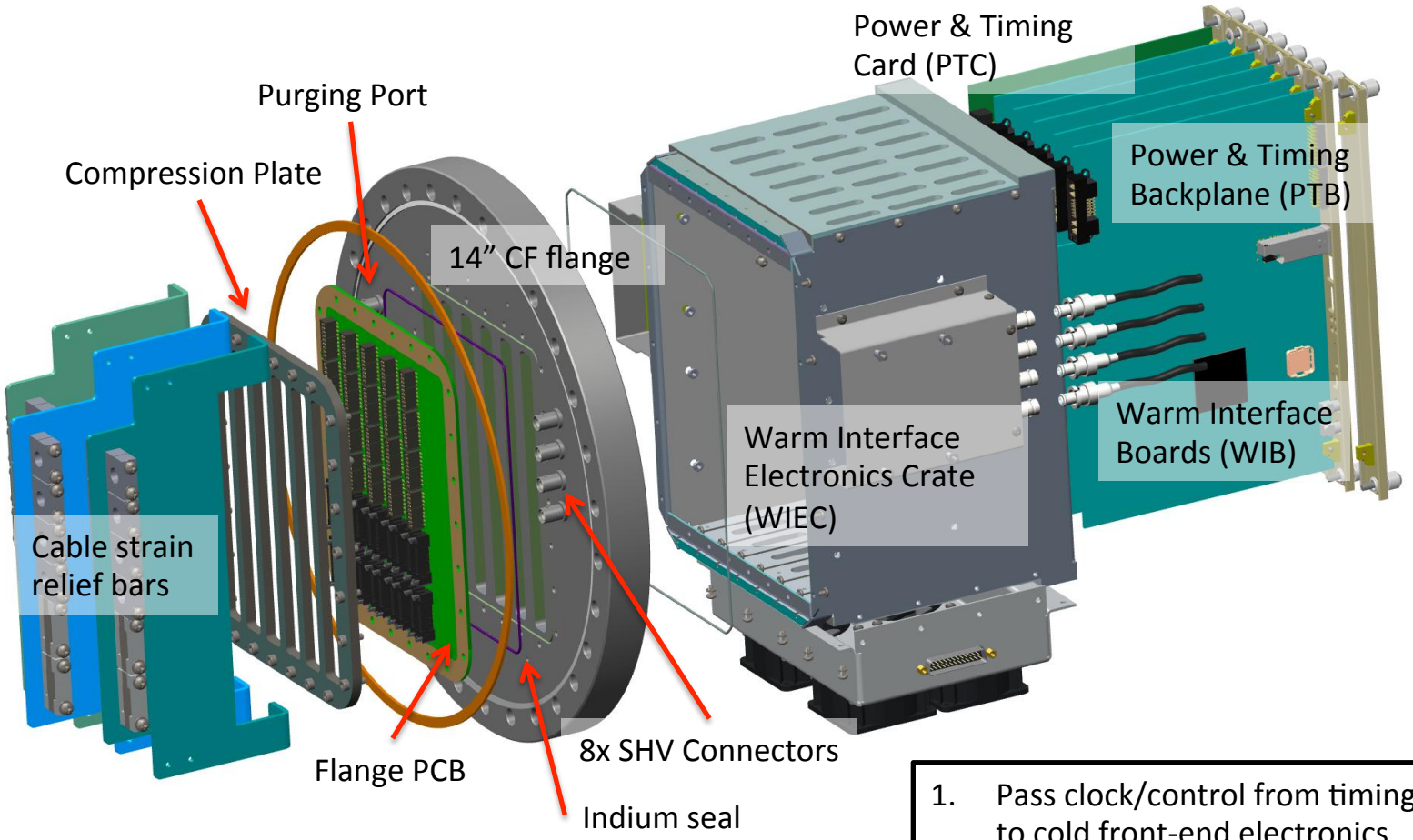
Signal Feed-through Status

- Tee pipe fabrication (10 pipes) ordered
  - Delivery expected mid-June
  - 1 prototype available at BNL: checked against mechanical drawings
- Crossing Tube Cable (CTC) support prototypes ordered
  - Submit final order 5/26 with 4 weeks lead time
  - Not needed for cold box test
- QC at BNL in June/July
  - See CE mechanicals QA/QC Plan DocDB 1809
  - Ship to CERN in shipping containers designed and built at BNL





CE Warm Components

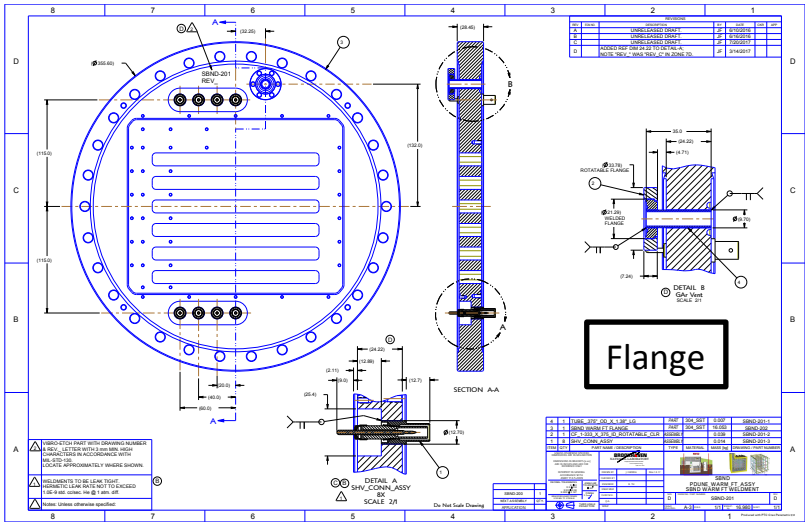


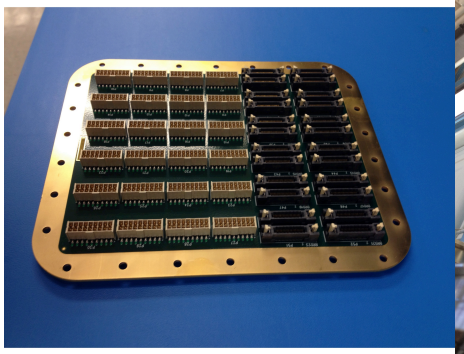
1. Pass clock/control from timing system to cold front-end electronics
2. Deliver high-speed TPC wire data from cryostat to DAQ

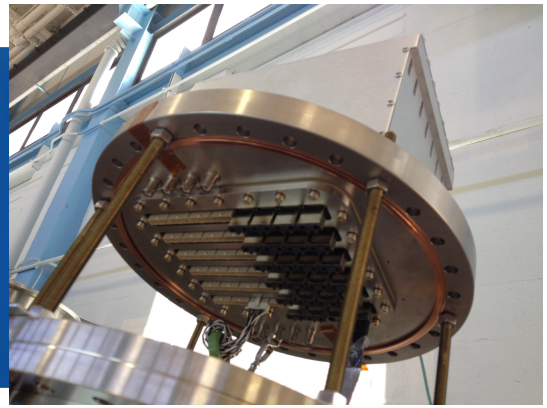
3. Connection to detector ground at CE flange
4. Pass wire-bias and FC HV to cryostat

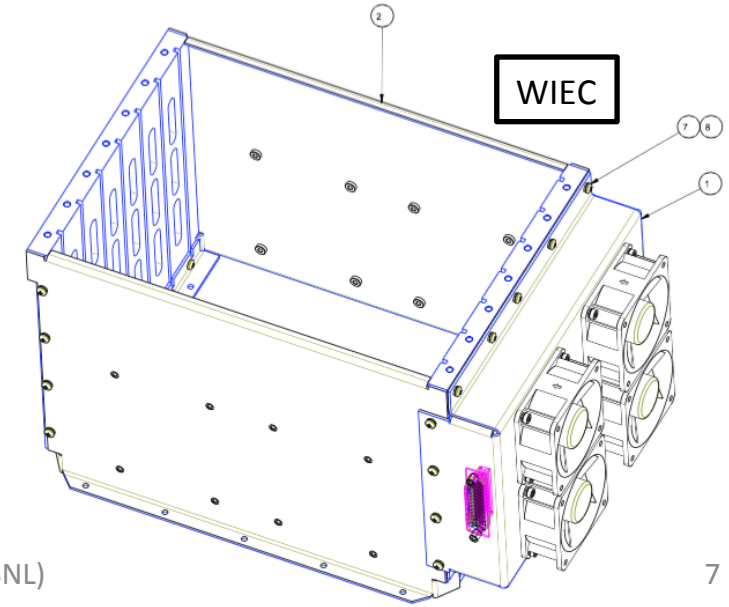
CE Flange and WIEC Status

- Final CE flange prototypes ordered
  - Submit final order mid-May with 6 week lead time
- Final WIEC prototypes ordered
  - Submit final order mid-May with 4 week lead time
- Flange PCB ordered
  - 3 prototypes being assembled
- QC at BNL in July/August
  - See CE mechanicals QA/QC Plan [DocDB 1809]
  - Ship to CERN in shipping containers designed and built at BNL

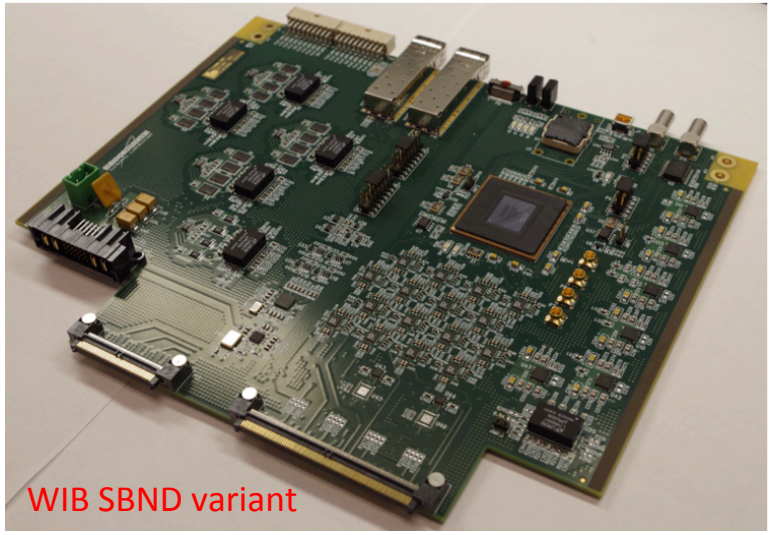


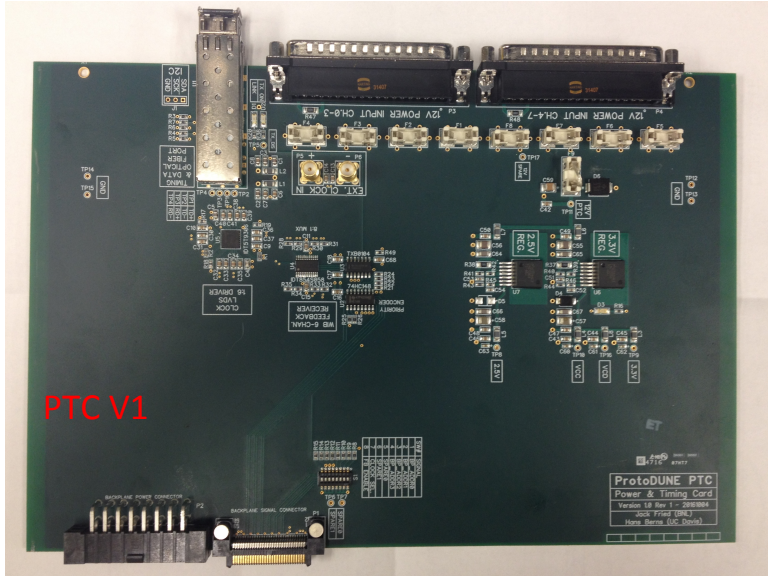






WIB/PTC Status


WIB SBND variant



PTC V1

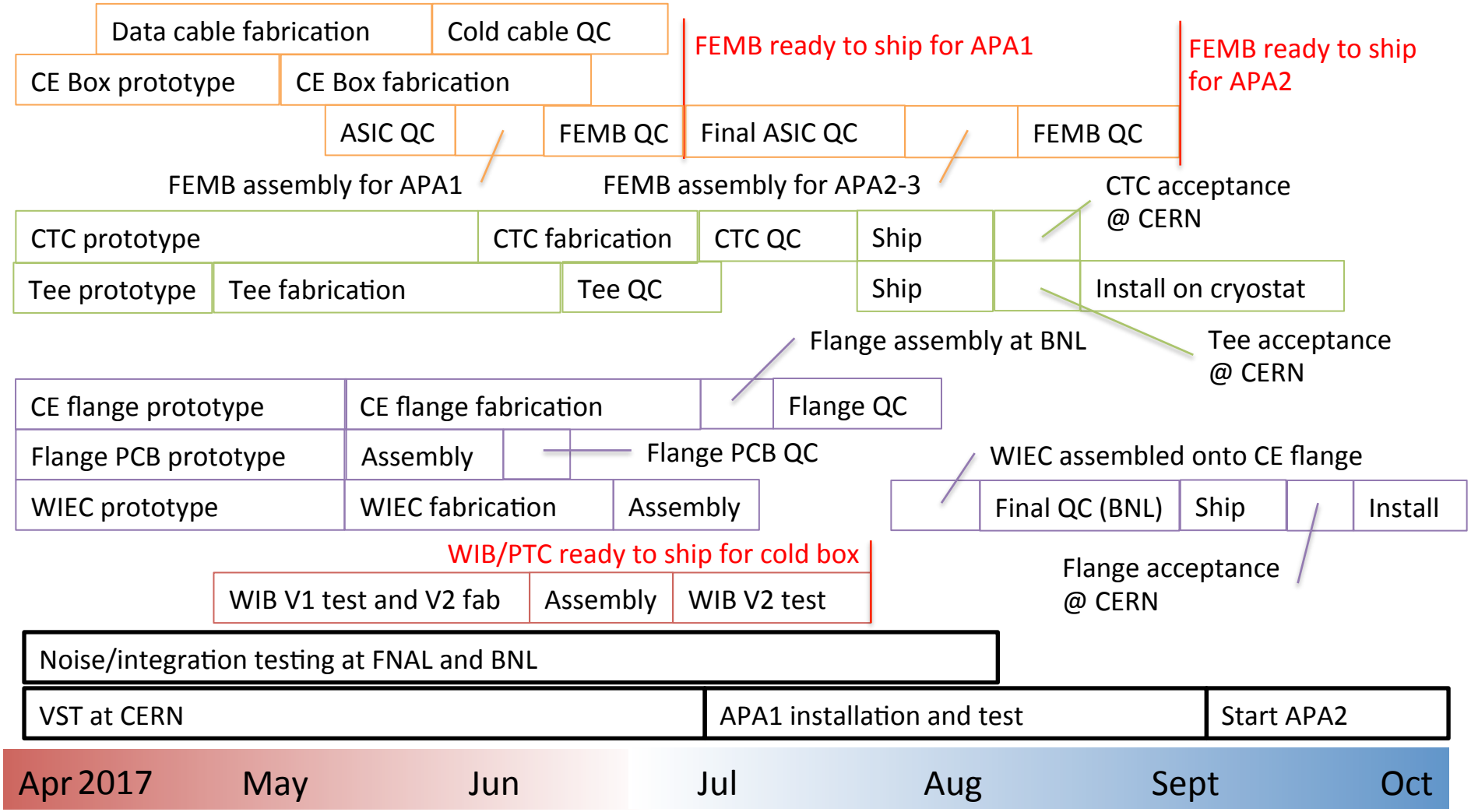
- Integration/noise measurements ongoing with SBND WIB at Fermilab and BNL
- ProtoDUNE V1 WIB out for assembly
  - Arria V GT variant FPGA (10 Gbps links)
  - ProtoDUNE clock/data separator
  - Receive at BNL next week and perform hardware functionality test
- Deliver WIB to Boston in early May
  - Development of firmware for FEMB-WIB and WIB-RCE communication ongoing with SBND prototype
  - Preliminary firmware with timing endpoint ported to Altera
- Assemble 4-5 more V1 WIBs by end of May
- Minor modifications will be made for V2 WIB
  - Fabrication and assembly done by late June
  - V2 WIBs available for full crate test at BNL in early July
- V2 version PTC layout complete (UC Davis)
  - 2 variants for 2 options for 48/12V DC converters
    - V2-A: with Vicor "Cool Power" Pi3546
    - V2-B: with Linear Tech. LTM8064
  - V2 prototype order will be placed next week

Milestones

- APA/Cryostat
  - Deliver V1 WIB/PTC for vertical slice in early June
  - 25 FEMB for APA1 ship to CERN in late June
  - Tee pipe + CTC units install on cryostat in late August
  - 50 FEMB for APA2-3 ship to CERN in early September
  - CE flange + WIEC assembly install on Tees in late September
  - Production WIB/PTC install in WIEC in early October
  - 75 FEMB for APA4-6 ship to CERN in mid-October
- Cold Box
  - Tee pipe ship to CERN in late June
  - Full prototype Flange + WIEC assembly install on cold box in July
  - Deliver V2 WIB/PTC for installation in WIEC in late July

Schedule

CE installation
(as of March)
- APA1: 6/28
- APA2: 9/8
- APA3: 10/26



Labeling

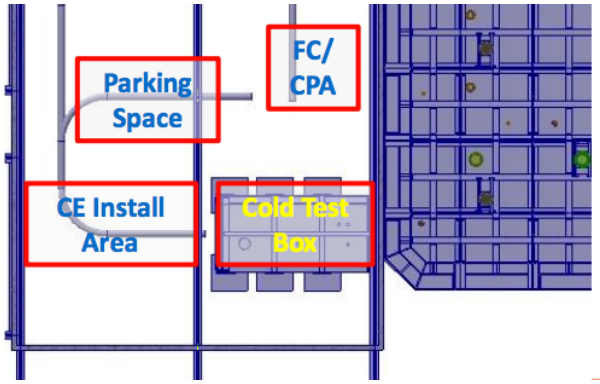
- Each major unit (FEMB, flange, signal FT) will have a primary label for identification at CERN
  - FEMB: have vendor etch ID onto CE Box
    - ASICs and FEMB will have individual IDs for QC testing at BNL
    - Once installed in CE Box, box ID becomes the final label for QC tests and tracking
    - QC database will allow for reporting test results from box ID back to each individual ASIC
  - Flange: have vendor etch ID onto stainless steel flange
    - Flange PCB and WIEC will be QC tested on flange and follow flange ID
  - Signal FT: have vendor etch ID onto Tee pipe
    - CTC support will follow Tee pipe ID
- All major units will all be tracked by a hardcopy traveller
  - Receiving and assembly history
  - Sign off on QC results
- Cables will be labeled at each end after FEMB pass final QC tests
  - Once FEMB are installed on APA and cable routed, label at box end will be removed

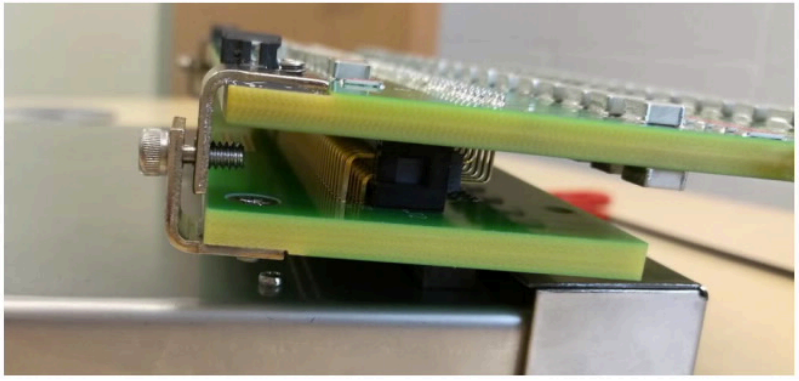
Shipping to CERN

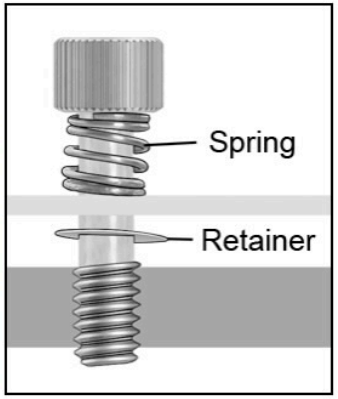
- Handled by Interfreight, an experienced broker, to CERN directly
  - Done for ATLAS LAr Calorimeter electronics for 10+ years
  - BNL rep will interact directly with Interfreight
- Custom packaging for all items will be designed and built by BNL team that installed MicroBooNE
  - FEMB/CE Box/PSL adapter will ship as unit
  - CE flange/WIEC unit will ship as unit
- Electronics protection
  - Cables will be detached from FEMB prior to shipping
  - All electronics shipped in anti-static bags
  - All electronics packed/unpacked using ESD straps

Installation on APA (1)

- CE installation area adjacent to cold box
- APA frame will be temporarily grounded to cold box (detector ground)
- FEMB will be brought into clean room in shipping containers
  - FEMB will be removed from container in anti-static bag
  - FEMB and corresponding data + LV cable will be taken on scissor lift to top of APA frame
  - Installer will wear ESD strap attached to APA frame, remove FEMB from bag, and install on APA
    - Two spring screws with retainers will mate FEMB unit to CR board







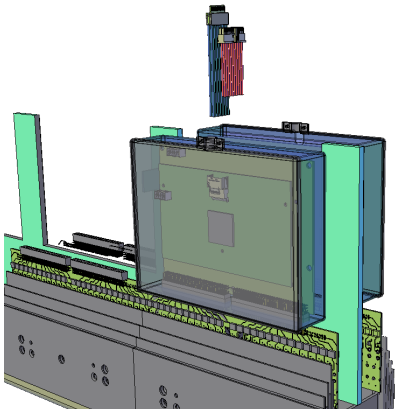
Electronics Mobile Teststand

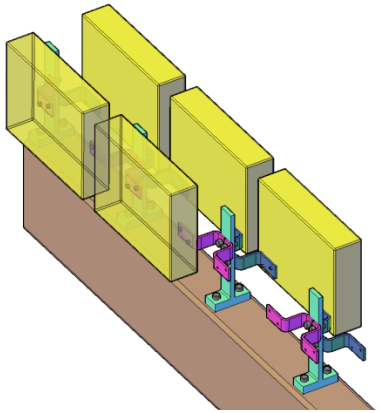
- Electronics Mobile Teststand (EMT) on cart
  - Laptop DAQ (simple set of Python scripts and ROOT for analysis)
  - WIB + cable adapter connected to DAQ via gig-E
  - LV power supply capable of 12V/4A

- Can be positioned at the bottom of APA where FEMB are being installed at the top
- Full checkout of FEMB
  - LV power over 7m LV cable bundle
  - I/O from WIB and high-speed data to WIB over 7m data cable bundle

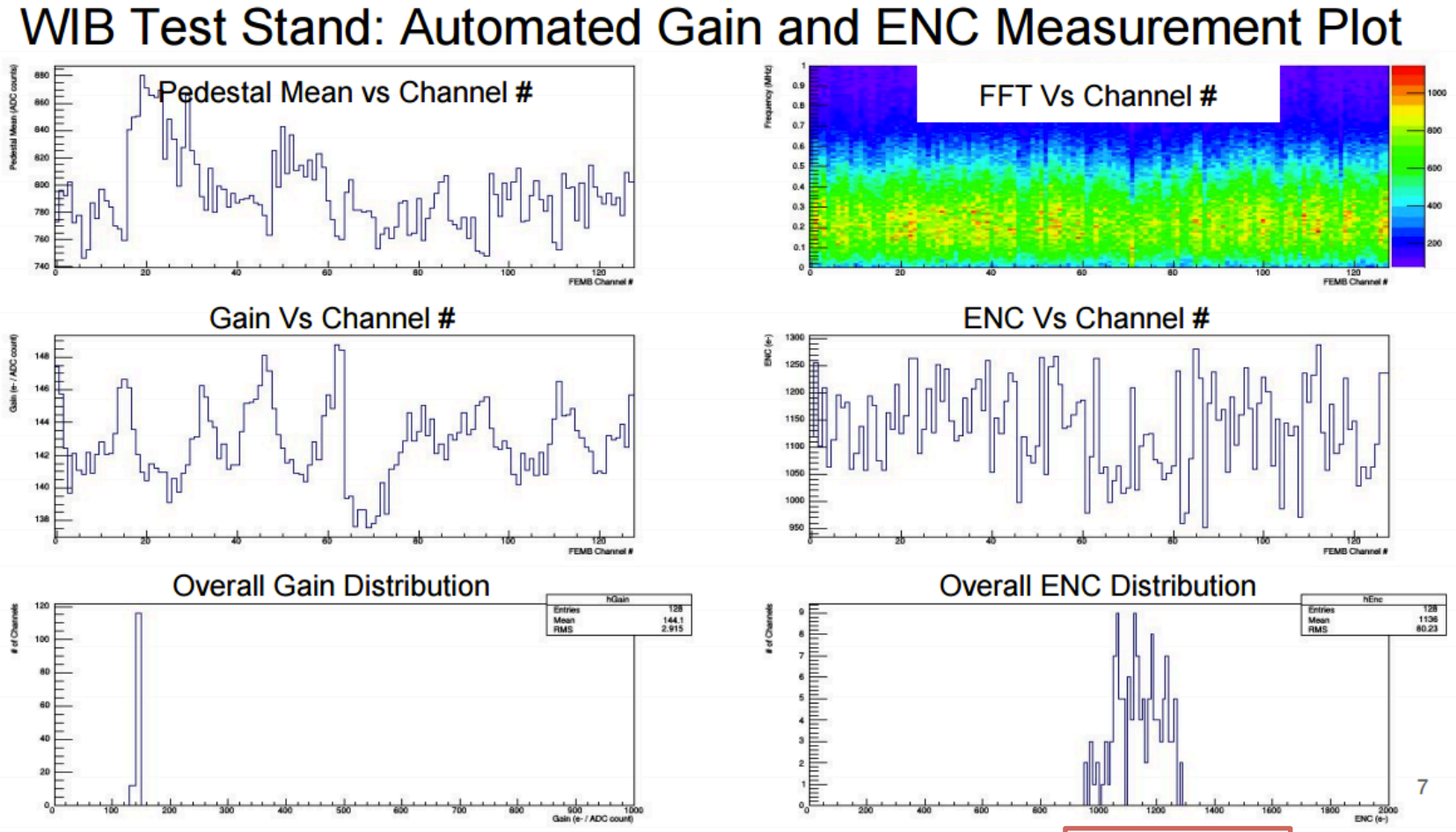
Installation on APA (2)

- Once FEMB is attached to CR board, CE box will be attached to mounting brackets
  - Copper ground braid will be attached to CE box and APA frame
    - Ensure low impedance connection between FEMB and APA
    - FEMB is now connected to detector ground
- LV cable lowered to EMT operator and plugged into FEMB
  - EMT operator also wearing ESD strap to detector ground
  - LV cable then plugged into WIB adapter board
- Data cable then lowered to EMT operator and plugged into FEMB
- CE box closed and FEMB warm checkout done





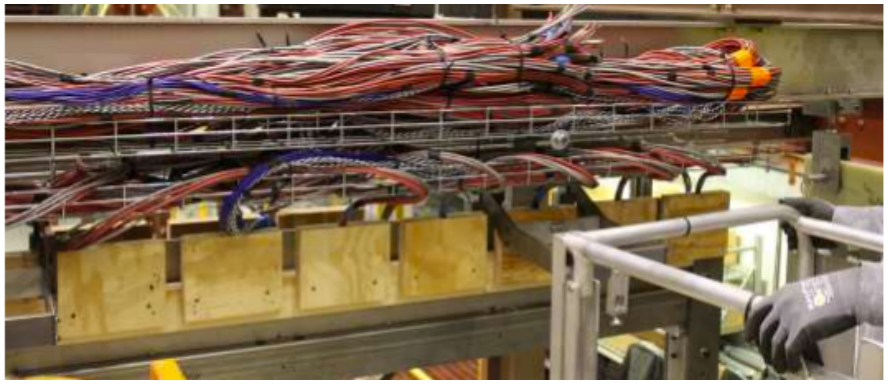
EMT Example Data



From B. Kirby

FEMB Acceptance Criteria

- All FEMB functionality must be successful via WIB interface
  - See CE electricals QA/QC Plan DocDB 1809
- No new dead channels relative to QC testing at BNL
- If FEMB passes acceptance criteria
  - Cables unplugged from WIB, lifted back up to top of APA, and routed along the double layer cable tray

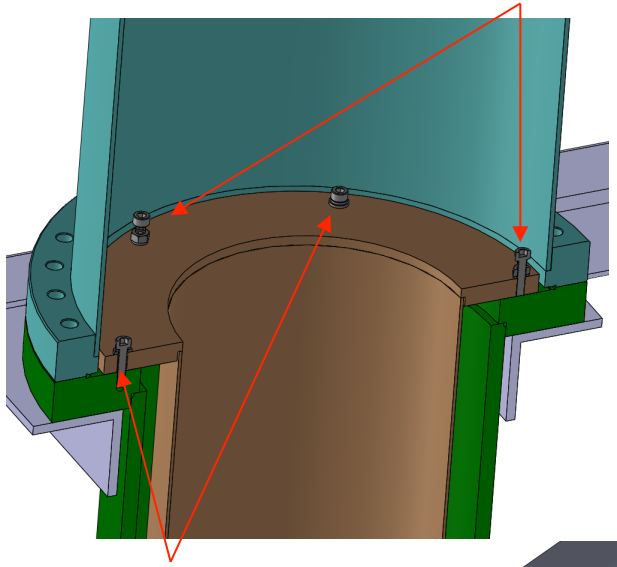


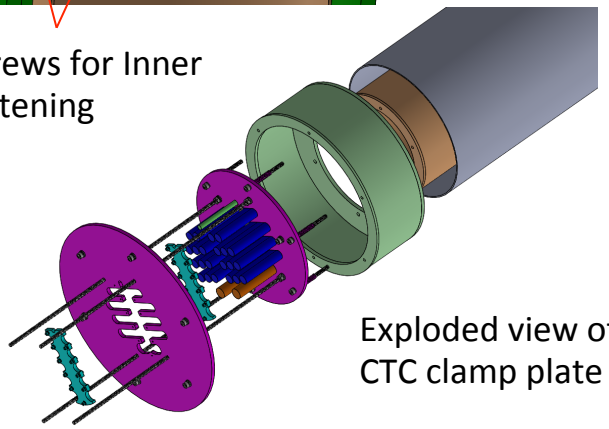
4.1 Functionality

To validate the functionality requires testing the following features of the FEMB both at room temperature and under multiple thermal cycles in LN2:

- successful loading of the FPGA programming from the onboard EEPROM;
- ability to program the FPGA and EEPROM over the backup JTAG links in the cold data cable bundle;
- ability to set the control registers on the FPGA via the I^2C control IO links;
- confirmation that the backup onboard oscillators can generate the clock for the FPGA state machine in case the clock from the system is lost;
- confirmation that the FPGA can configure all 16 ASICs on the analog motherboard via SPI interface and synchronize the data from all serial links from the ADCs (either 16:1 or 8:1 multiplexing on each ADC ASIC);
- verify that in the state with all ASICs configured, the current drawn by the CLR for all LV power inputs are nominal, indicating the FPGA is programmed and ASICs operational;
- confirmation that all channels observe both the FPGA internal pulser and an external pulser with the FE test capacitor enabled;
- confirmation that all channels observe the FE ASCI internal pulser;
- successful transmission of all digitized waveform data over all 4 ~1.2 Gbps links at sufficiently low Bit Error Rate (BER).

Signal Feed-through Installation

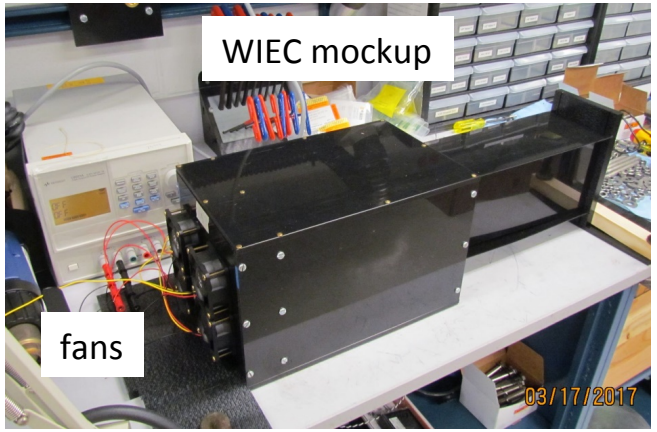


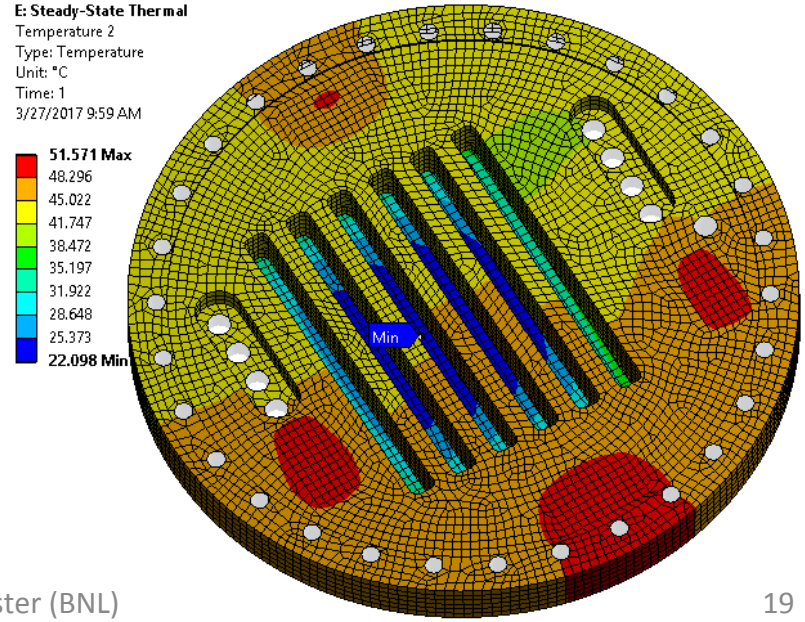


- CTC assembled and lowered down through crossing tube
  - Positioned with alignment screws
- Tee pipe attached to 14” flange on top of cryostat
  - Hardware to attach Tee to cryostat flange provided by BNL
- CE flange/WIEC unit will be held off Tee port by a fixture allowing access to both sides of flange
  - Adjustable fixture being developed at BNL with prototype Tee and flange
    - After cables connected, flange can be slid mostly closed and temporarily sealed while final validation is done
  - Hardware to attach CE flange to Tee provided by BNL

WIEC Fans and Heaters

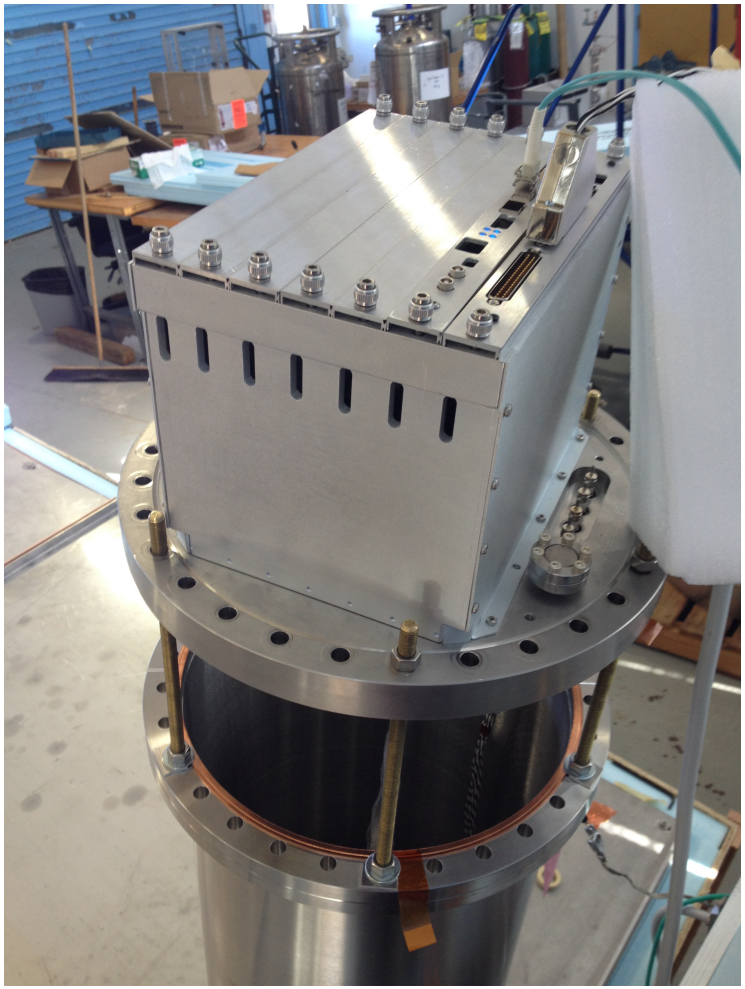
- 4 WIEC fans and 4 flange heaters will come installed on each flange and QC tested at BNL
  - Power and monitoring provided by the CERN DCS system
  - After each flange is attached to fixture, fans and heaters will be connected to CERN DCS racks
  - Full functionality test:
    - All 4 fans powered on and CERN DCS receives the RD monitoring signal
      - If RD signal indicates that a fan is non-operational, DCS interlock must engage and shut off LV power to WIEC electronics at the Wiener supply
    - All 4 heaters powered on and CERN DCS receives the RTD temperature sensor





Warm Electronics Installation

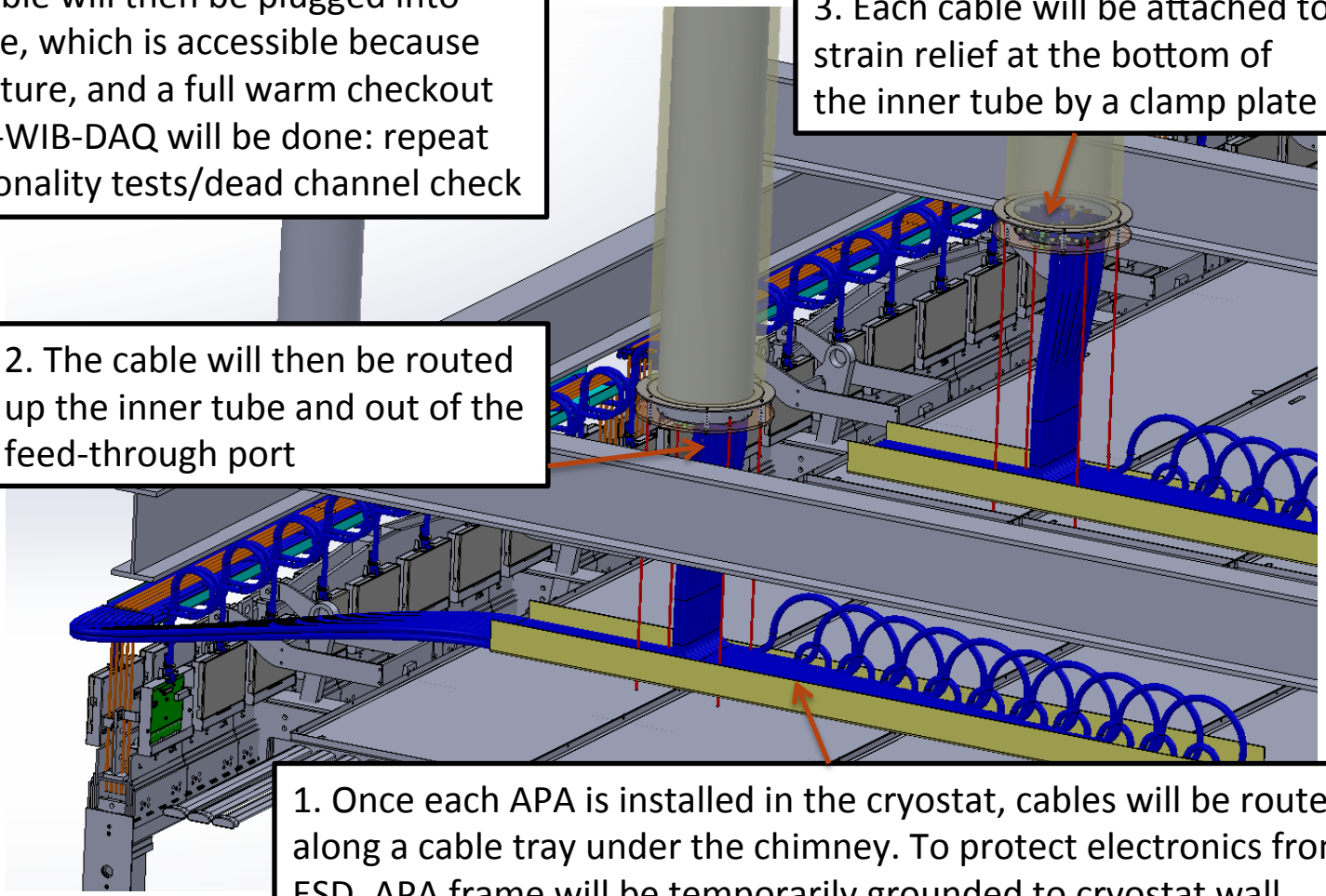
- As each WIB is installed in the WIEC it will be tested via GbE DAQ in test-data mode
  - Once WIB is validated, it will be connected to DAQ via optical fibers
- Full functionality test of full crate will be done with final DAQ after assembly
  - All high-speed links operational with test-data
  - All WIB receiving and sending back to timing system
- WIB and PTC are easily swappable with spare boards for testing and debugging



Installation Inside the Cryostat

4. The cable will then be plugged into the flange, which is accessible because of the fixture, and a full warm checkout of FEMB-WIB-DAQ will be done: repeat of functionality tests/dead channel check

3. Each cable will be attached to strain relief at the bottom of the inner tube by a clamp plate



2. The cable will then be routed up the inner tube and out of the feed-through port

1. Once each APA is installed in the cryostat, cables will be routed along a cable tray under the chimney. To protect electronics from ESD, APA frame will be temporarily grounded to cryostat wall

CE Installation Team

- BNL
  - Hucheng Chen, Bo Yu, Jack Fried, Ken Sexton, Augie Hoffman, Shanshan Gao, Brian Kirby, Elizabeth Worcester, Matt Worcester
  - 1 new post-doc is being hired and will arrive at CERN in November
- MSU
  - Dean Shooltz, Jake Calcutt, Kendall Mahn, and Carl Bromberg
- LSU
  - Justin Hugon and Martin Tzanov
- Fermilab
  - Terri Shaw and Linda Bagby (focus on grounding)
- Others for help as needed
  - Hans Berns (UC Davis), Eric Hazen and Dan Gastler (Boston)

Cold Commissioning

- Detector commissioning after filling: May-July 2018
  - However, MicroBooNE commissioning "took ~one year to understand and remove/reduce the excess noise effects, to be left with the remaining FE ASIC noise" (V. Radeka)
  - 35-ton commissioning was hampered by lack of real-time local diagnostics once the cryostat was filled
    - Current design includes option to read out in real-time either analog waveforms or digitized waveforms at the WIB
- Cold electronics tests to be performed:
  - Baseline uniformity and RMS noise on all channels
    - Identify any channel with loss of performance after LAr filling
    - Both MicroBooNE and 35-ton lost channels at or immediately after cooldown
      - Current version of ASICs do not have the "cold start up" issue
  - Gain calibration with onboard FE ASIC pulser
    - Cross-check with injectable pulser from FPGA
  - ADC linearity measurement with FE ASIC pulser
    - Including stuck code analysis

Summary

- The APA+cold readout+Faraday Cage/Feedthrough with Warm Interface and Local Diagnostics should be treated as an integrated whole and installed as such
  - Coordinated TPC grounding and shielding between CE, PD, and APA teams
- QC plan for validation at BNL in place
  - Developing written plan for installation QC at CERN
- Shipping details being finalized at BNL
  - Using experienced vendor
  - Custom containers being designed at BNL
- Still lots of details to be worked out in this discussion…