

Software for operating the magnet protection systems

GSI - CERN workshop

Marc-Antoine Galilée
TE-MPE-MS



Overview

- ▶ Software stack & architecture
- ▶ Tools for operators and experts
- ▶ Collection of data
- ▶ Known shortcomings & planned evolutions

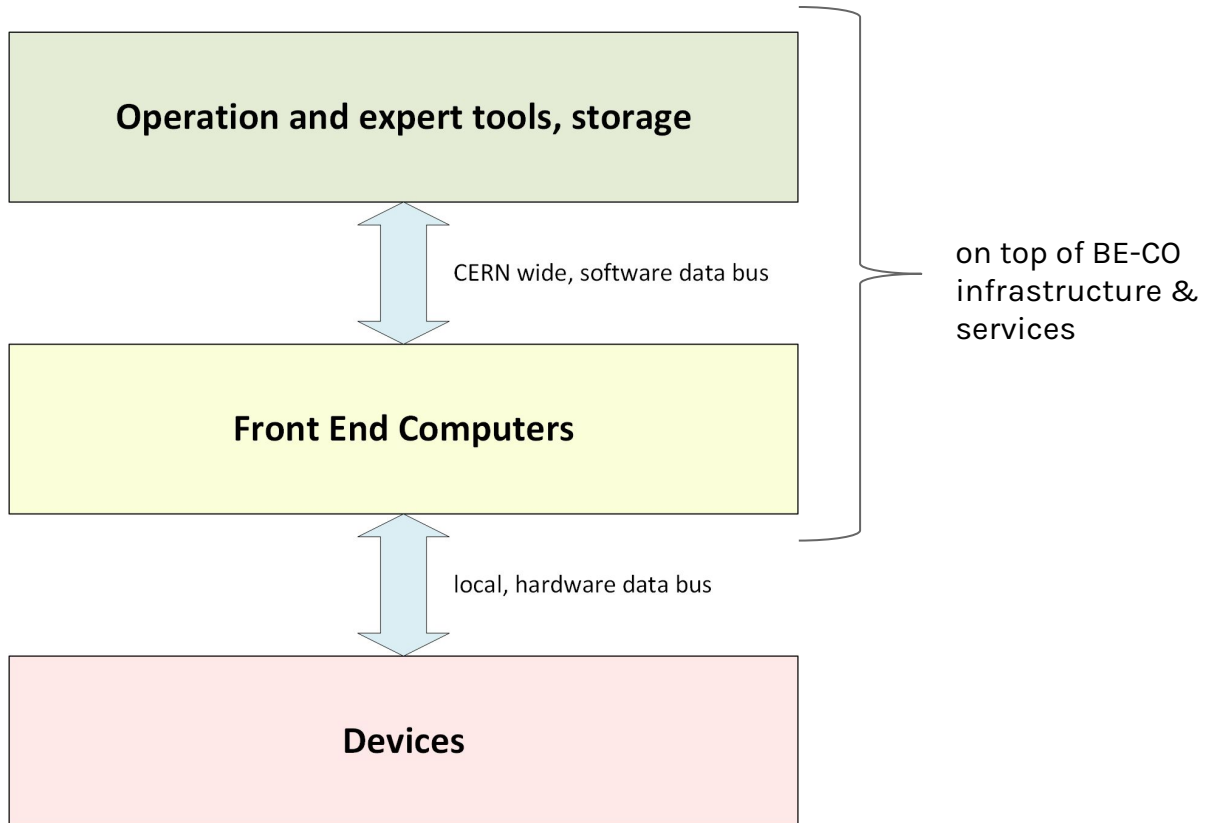


Overview

- ▶ **Software stack & architecture**
- ▶ Tools for operators and experts
- ▶ Collection of data
- ▶ Known shortcomings & planned evolutions

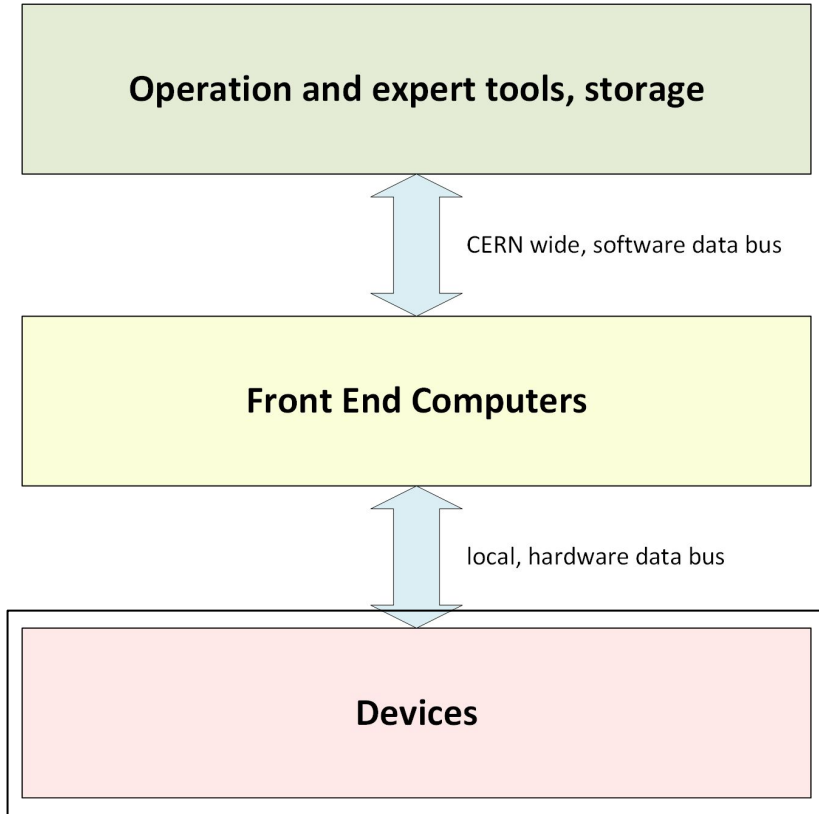


Software stack





Software stack - Devices

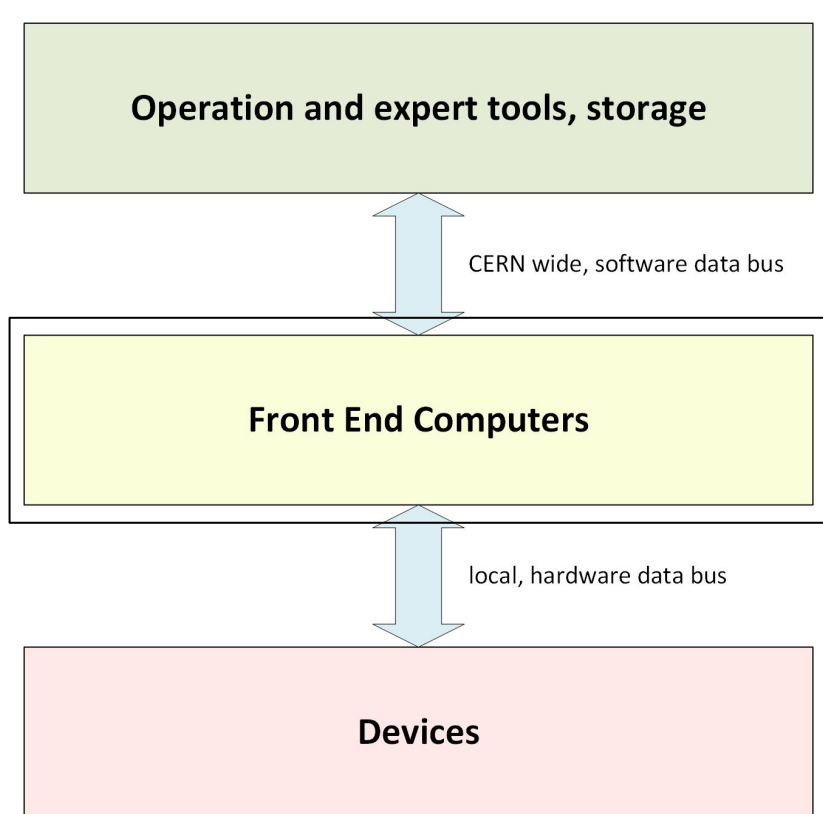


Software

- **firmware & drivers (VHDL, C, ...)**
- hardware development and validation tools



Software stack - Front End Computers (FECs)



Software

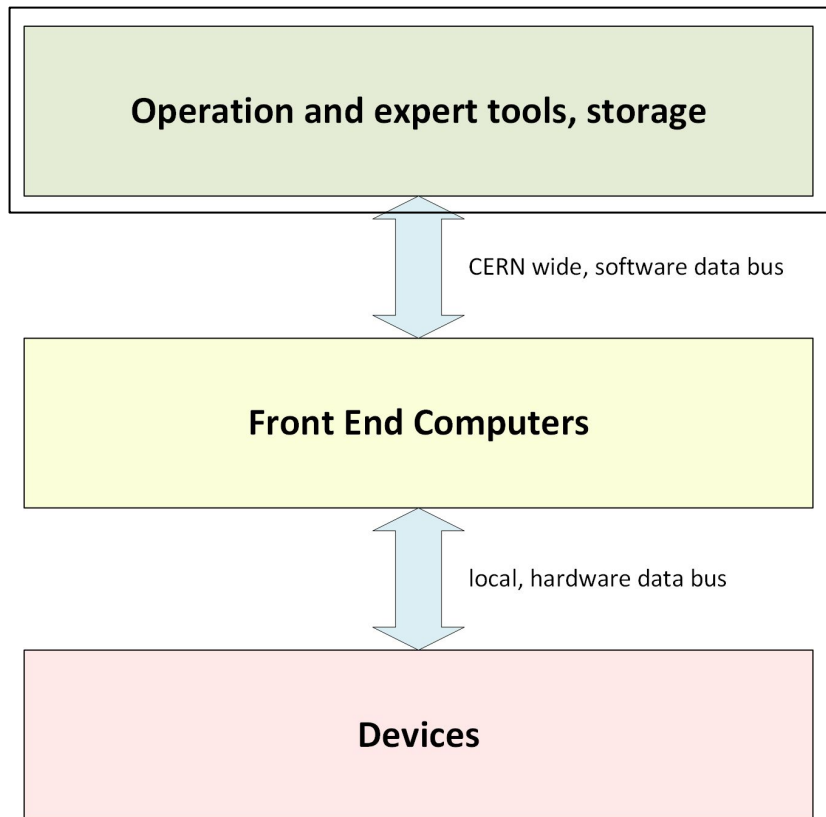
- **C++**
- **Real Time**
- 'Thin' layer to abstract over the device(s)

The 'FESA' (Front End Software Architecture) framework

- CERN standard
- authentication
- deployment
- configuration
- software data bus



Software stack - Tools & storage



Software

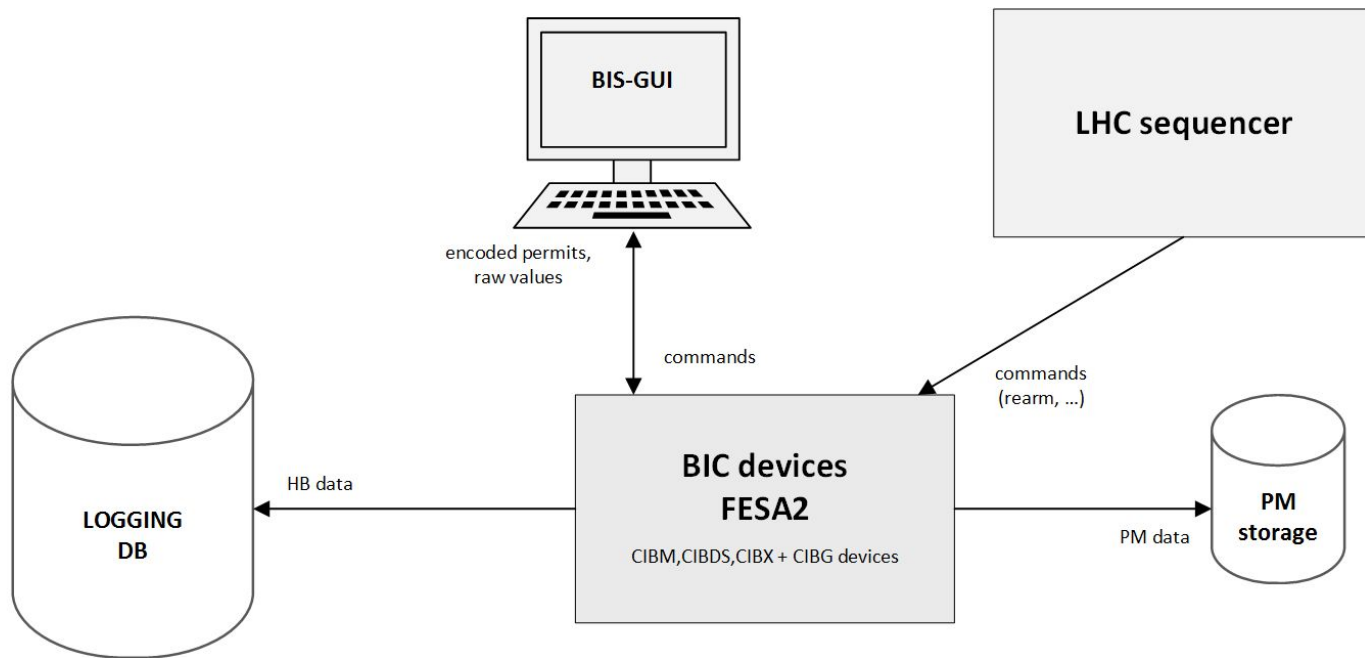
- **Java**
- **Labview**
- **WinCC OA**
- and more
- various DBs and storages

Usages

- Operation
- Analysis
- Commissioning
- Development
- Diagnostics



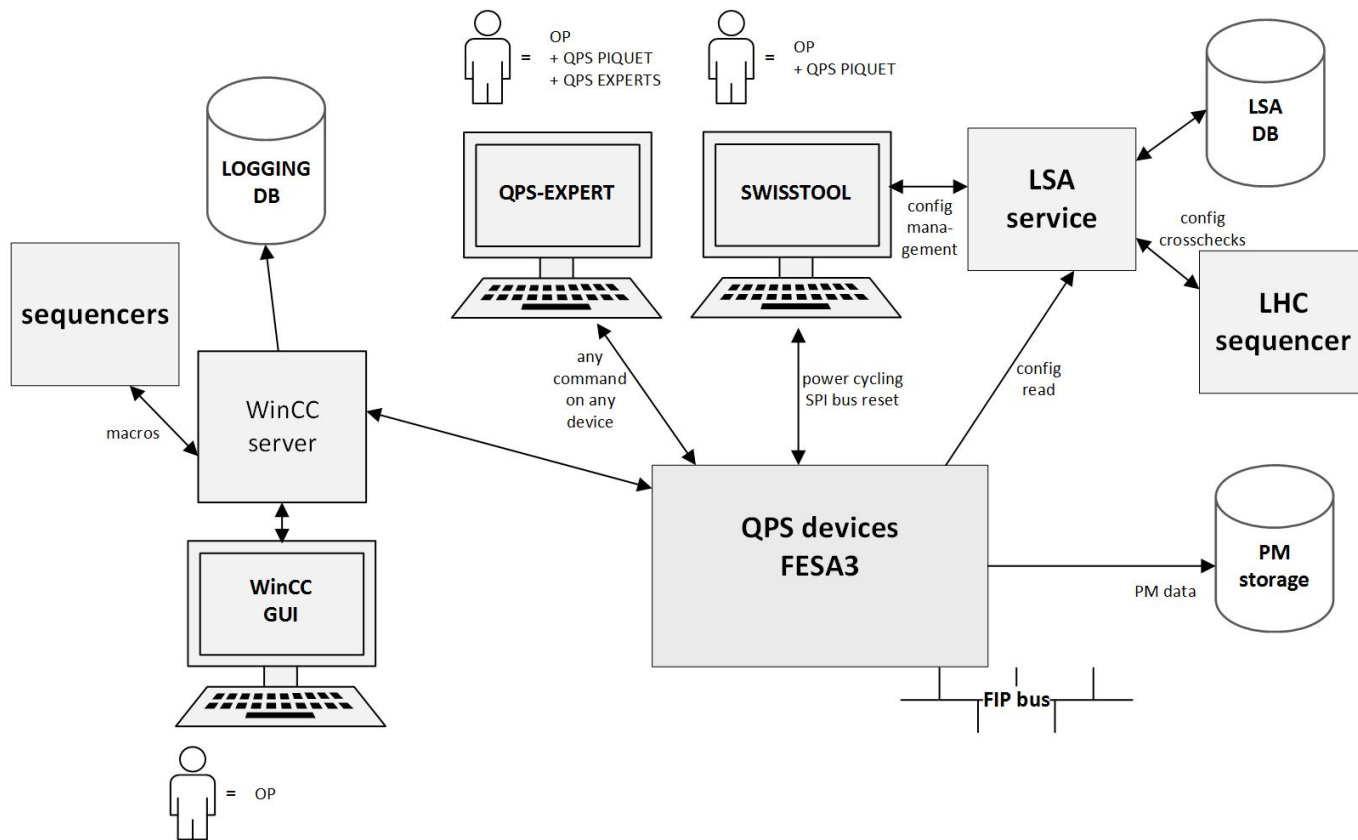
Example: Beam Interlock System architecture



(not a magnet protection system per se, provided here as an example of a lower complexity system following a very similar architecture)



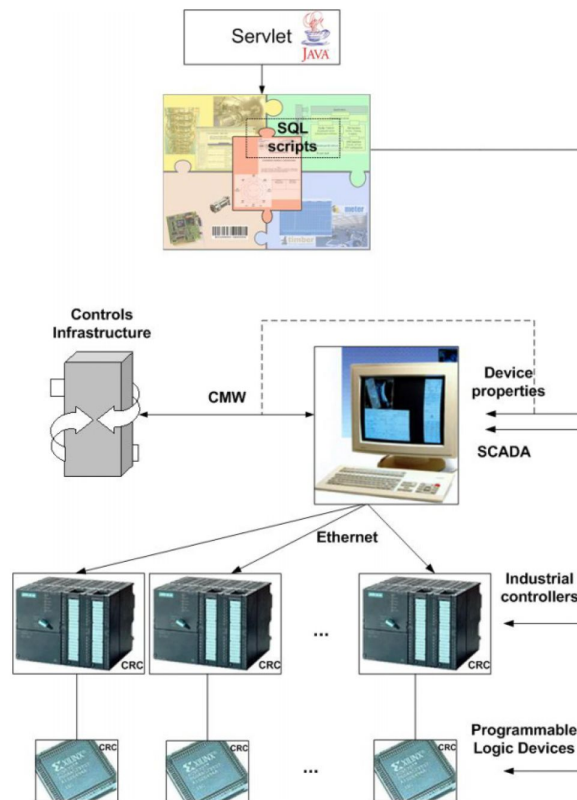
Example: QPS architecture





Example: Powering Interlock System architecture

- ▶ Example of another flavour of software architecture & technologies
- ▶ PLC based system, managing all (boolean) interlock conditions between QDS, converter, cryogenics, ancillaries, ... to assure safe operation of magnet powering system
- ▶ 36 individual systems around the circumference, using Profibus to connect remote I/Os
- ▶ Synchronised via NTP

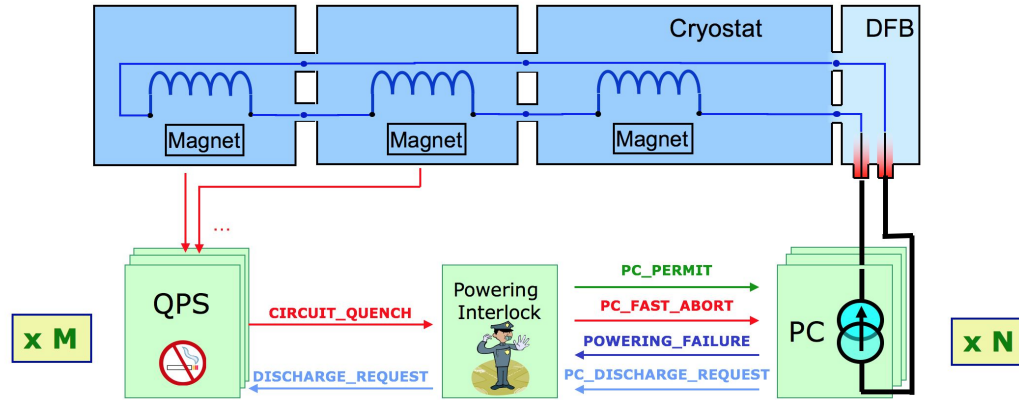




Tools for operators and experts

- ▶ Software stack & architecture
- ▶ **Tools for operators and experts**
- ▶ Collection of data
- ▶ Known shortcomings & planned evolutions

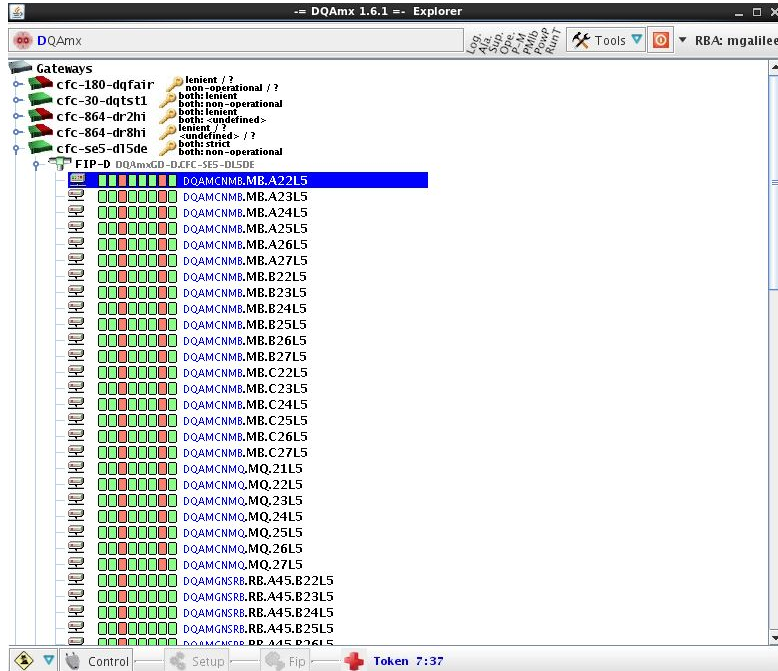
Tools for operators and experts



- ▶ Magnet protection system (for the LHC) relies on interaction of quench detection system, power converter and powering interlock system (+ ancillaries such as CRYO, emergency stops, UPS, access, ...)
- ▶ Systems use (very) different architectures and technologies
- ▶ Expert tools (system by system) are important for initial commissioning, development, maintenance, ...
- ▶ Operational tools focus on global system view (and provide limited functionality)
- ▶ For the LHC a set of rather heterogeneous tools is used for operation of the magnet powering system



Tools: QPS Expert, overview



- ▶ Expert tool, providing overview of all devices and allowing necessary (expert) interactions with devices
- ▶ One level of granularity: a single protection device
- ▶ Typically such applications provide little operational context or interactions with connected equipment systems



Tools: QPS Expert, device GUIs

The screenshot displays the DQAmx 1.6.1 GUI interface, which is used for testing and debugging hardware components. The main window shows the 'Logical States' section, which includes a table of bit states and a list of logical state names.

Logical States Table:

Bit_0	Bit_1	Bit_2	Bit_3	Bit_4	Bit_5	Bit_6	Bit_7
DQAMC PWR_PERM	DOAMC ACOSLOW	DQAMC BUS	DQAMC TIMING	DQCSU PWR_ISO_A	DQCSU PWR_ISO_B	DQCSU PWR_GEN_A	DQCSU PWR_GEN_B
MB MAGNET_OK	MB PWR_PERM	DQDDL PWR_PERM	DQDDL COHER	MB NQD0	DQDDL PWR	DQDDL LOOP_CLO	DQHSU HDS_FUSE_OI

Dump WorldFip Agent Table:

VAR	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
DATA 0	38	08	3F	00	58	C9	55	04	00	6E	FD	FD	08	03	08	01
DATA 1	38	08	40	01	00	00	00	00	00	2C	00	29	00	30	00	31
DATA 2	19	0F	FD	02	58	48	60	DB	01	56	F4	A8	08	0F	07	F6
DATA 3	19	0F	FD	03	58	48	60	DB	01	58	F4	A8	08	0F	07	F6
CMD	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00	00
TIME	58	C9	55	04	11	E1	A3	00								
Option	9A	01	00	44	09	03	00	00	00	00	00	00	00	00	00	00

Logical States Table (Bottom):

	Scale A	Offset B	Aqn Y Ax + B	S I	Occ/Max
U_1	0.10068	-206.2	000.3	V	
U_2	0.10068	-206.2	000.1	V	
U_Q50	1.2207E-4	-0.25	0.0012201	V	
PARE_0	1.0	0.0		V	
PARE_1	1.0	0.0		V	
PARE_2	1.0	0.0		V	
HDS_1	0.01916605	0.0	0000.8	V	
HDS_2	0.01916605	0.0	0000.8	V	
HDS_3	0.01916605	0.0	0000.9	V	
HDS_4	0.01916605	0.0	0001.0	V	
HDS_1	0.0019074	0.0	0.082	A	
HDS_2	0.0019074	0.0	0.084	A	
HDS_3	0.0019074	0.0	0.086	A	
HDS_4	0.0019074	0.0	0.088	A	

Powerful, information heavy GUI
=> ~microscope equivalent => pure Expert tool



Tools: QPS Swisstool

Powercycle Settings SPI Bus

Actions

- Settings cross-check
- Crosscheck all devices
- Acquire settings for all the devices

Filters

- Text Filter
- Consistency check
- Device type
- Firmware revision
- Location
- Powercycling capability
- Circuit Type
- Powering subsector

Fesa device name	Consistency	Firmware
DQAMGNSRQF.RQF.A23.B26R2	✓	214
DQAMGNSRQF.RQF.A45.B33R4	✓	214
DQAMNS00.RR53.RQF.A45B2	✗	0
DQAMNS00.RR53.RQF.A45B1	✗	0
DQAMGNSRQF.RQF.A67.B18L7	✓	214
DQAMGNSRQF.RQF.A81.B17L1	✓	214
DQAMGNSRQF.RQF.A23.B13L3	✓	214
DQAMGNSRQF.RQF.A34.B10L4	✓	214
DQAMGNSRQF.RQF.A78.B15L8	✓	214
DQAMGNSRQF.RQF.A12.B16R1	✓	214
DQAMGNSRQF.RQF.A78.B28L6	✓	214
DQAMGNSRQF.RQF.A81.B17R8	✓	214
DQQLC_NEVEN.RQD.A56.EVEN	✗	0
DQAMGNSRQF.RQF.A34.B23L4	✗	214
DQQLC_NEVEN.RQF.A34.EVEN	✗	0
DQAMGNSRQF.RQF.A23.B26R2	✗	214
DQAMGNSRQF.RQF.A56.B30R5	✓	214
DQAMNS00.UJ33.RQS.A34B2	✗	0
DQAMGNSRQF.RQF.A45.B20R4	✗	214
DQAMNSRB_UA63.RB.A56	✗	0
DQAMGNSRQF.RQF.A67.B18R6	✗	214
DQAMGNSRQF.RQF.A56.B12R5	✗	0
DQAMNS00.UA47.RU.R4	✗	0
DQAMGNSRQF.RQF.A12.B21L2	✗	0
DQAMGNSRQF.RQF.A34.B18R3	✗	0
DQAMGNSRQF.RQF.A78.B33L8	✗	0
DQAMGNSRQF.RQF.A23.B31L3	✗	0
DQAMNSRB.RR77.RB.A78	✗	0
DQAMNS00.RR77.RSS.A78B2	✗	0
DQAMNS00.RR77.RSS.A78B1	✗	0
DQAMNSRQ_UA63.RQD.A56	✗	0
DQAMGNSRQF.RQF.A56.B30L6	✗	0
DQAMNS00.RR73.RQD.A67B2	✗	0
DQAMNS00.RR73.RQD.A67R1	✗	0
DQAMGNSRQF.RQF.A12.B34R1	✗	0
DQAMGNSRQF.RQF.A78.B8R7	✓	214
DQAMGNSRQF.RQF.A78.B15R7	✓	214
DQAMNS00.UA87.P0TD.A91...	✓	214
DQAMNS00.UA43.RCD.A34B2	✗	0
DQAMNS00.UA43.RCD.A34B1	✗	0
DQAMGNSRQF.RQF.A78.B28R7	✓	214
DQAMGNSRQF.RQF.A12.B21R1	✓	214
DQAMGNSRQF.RQF.A23.B13R2	✓	214
DQAMGNSRQF.RQF.A67.B23L7	✓	214

Selected device name: DQAMGNSRQF.RQF.A23.B26L3

Hardware configuration Parameters table

Hardware configuration

Last reading from hardware: 2017-03-09 11:54:57.800000000
 Last reading from FESA: 2017-03-15 15:02:43.800000000
 Time set in hardware: 2015-02-13 15:51:58.200000000
 Data dimension: 1024

Address	Value	Name	Description	Board name
0	170	LSA mode	LSA view 0: expert (total) view	DQAMGS
1	214	firmware_revision	Firmware version	DQAMGS
2	129	sub_number	Device subscriber number	DQAMGS
3	255	macro_cycle_length	WorldFipTM macro-cycle length [ms]	DQAMGS
4	127	flp_wait_sec_h	Field-bus communication time out (300) [s]_higher_byte	DQAMGS
5	255	flp_wait_sec_l	Field-bus communication time out (300) [s]_lower_byte	DQAMGS
6	127	start_time	Start-up time (no DAQ trigger), 200 [cycles]	DQAMGS
7	255	local_com_on	Local communication ON/OFF	DQAMGS
8	127	no_pm_trig	0: PM trig 1: no PM trig	DQAMGS
9	255	qps_ok_opt	QPS_OK calculation	DQAMGS
10	0	time_cor_val	Timing error correction	DQAMGS
11	2	t_error_max	Maximum timing error [ms]	DQAMGS
12	40	buffer_wait_sec	PM buffer filling time out [s]	DQAMGS

Powercycle Settings SPI Bus

Actions

- Naming settings
- Show db crate names

Filters

- Text Filter
- Location
- Circuit Type

Expert crate name	Circuit 1	Circuit 2	Circuit 3	Circuit 4
DQGPU.F=RR77	RQ6.R761	RQ6.R762	RQ13.R761	RQ13.R762
DQGPU.L=RR77	RQ12.R762	RQ11.R762	RQ13.R761	RQ12.R761
DQGPU.D=RR77	RQ110.R761	RQ110.R762	RQ15.R761	RQ15.R762
DQGPU.U=RR77	RSS.A1262	RSS.A1261	RQS.R161	RQS.A1262
DQGPU.L=RR53	RSS.A4562	RSS.A4561	RQS.A4561	RQS.L562
DQGPU.L=RR57	RQS.R561	RQS.A5662	RSS.A5661	RSS.A5662
DQGPU.B=RR77	ROD.A7862	ROF.A7862	ROF.A7861	ROD.A7861
DQGPU.L=RR17	ROD.A1261	ROF.A1261	ROF.A1262	ROD.A1262
DQGPU.H=RR53	RQ111.L562	RQ12.L562	RQ11.L561	RQ12.L561
DQGPU.H=RR57	RQ12.R562	RQ11.L562	RQ11.L561	RQ12.L561
DQGPU.L=RR77	RQS.A7862	RQS.A7861	RSS.A7862	RSS.A7861
DQGPU.H=RR17	RQ12.R162	RQ11.L162	RQ12.R161	RQ11.L161
DQGPU.G=RR53	ROD.A4562	ROF.A4562	ROF.A4561	ROD.A4561
DQGPU.U=RR57	ROF.A5662	ROD.A5662	ROF.A5661	ROD.A5661
DQGPU.L=RR17	RQ13.R161	RQ13.L162		
DQGPU.F=RR53	RQ13.L561	RQ13.L562		
DQGPU.F=RR57	RQ13.R561	RQ13.R562		

Beam Presence Flag

Override Beam Presence Flag: Beam Presence Flag is FALSE - Reset Enabled

Powercycling fesa device

Name: DQAMGNSR.RR57.UNIT.A
Bank: 3

Detector crate

Name: DQGPU.06RR57

Circuit Name	Communication	QPS_LOCC2 [IA]	PC_MEAS_1 [IA]	PC Status	PC Name
RQS.R561	Wait 10 sec...	0.44	0.00	FLT_OFF	RPMB.A.RR57.RQS.R561
RQS.A56B2	Wait 10 sec...	0.44	0.00	FLT_OFF	RPMB.A.RR57.RQS.A56B2
RSS.A56B1	Wait 10 sec...	0.44	0.00	FLT_OFF	RPMB.B.RR57.RSS.A56B1
RSS.A56B2	Wait 10 sec...	0.44	-0.00	FLT_OFF	RPMB.B.RR57.RSS.A56B2

Refresh data

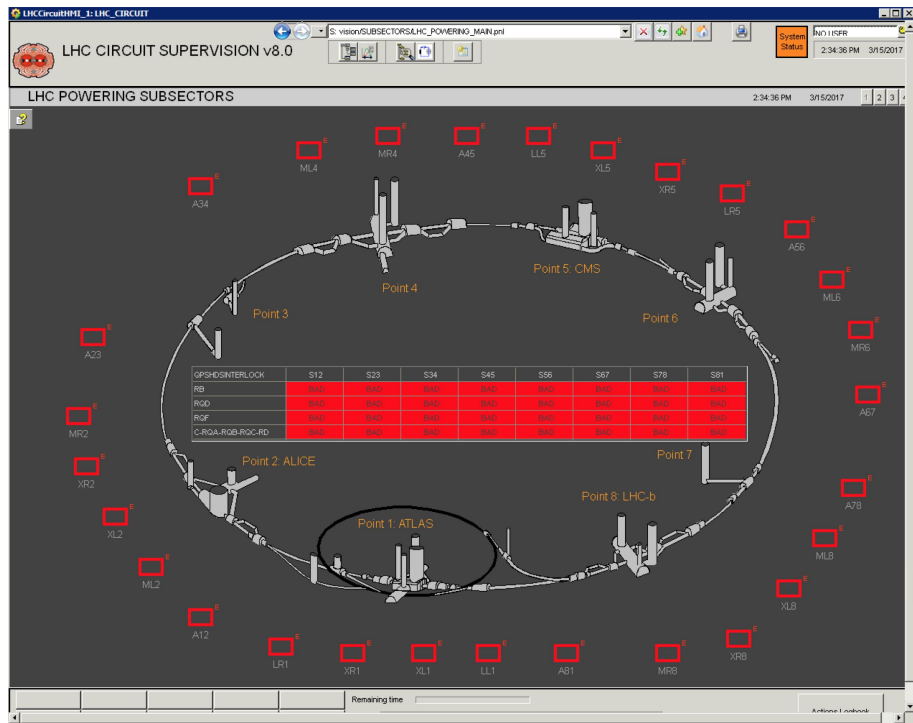
← Configuration cross checking
 Device registers definitions + values

----->
 Device status summary
 Operational commands
 Beam context

=> mixed Standby-service / OPERATOR tool
 for standard validation and recovery actions
 (Implementing several levels of protection)



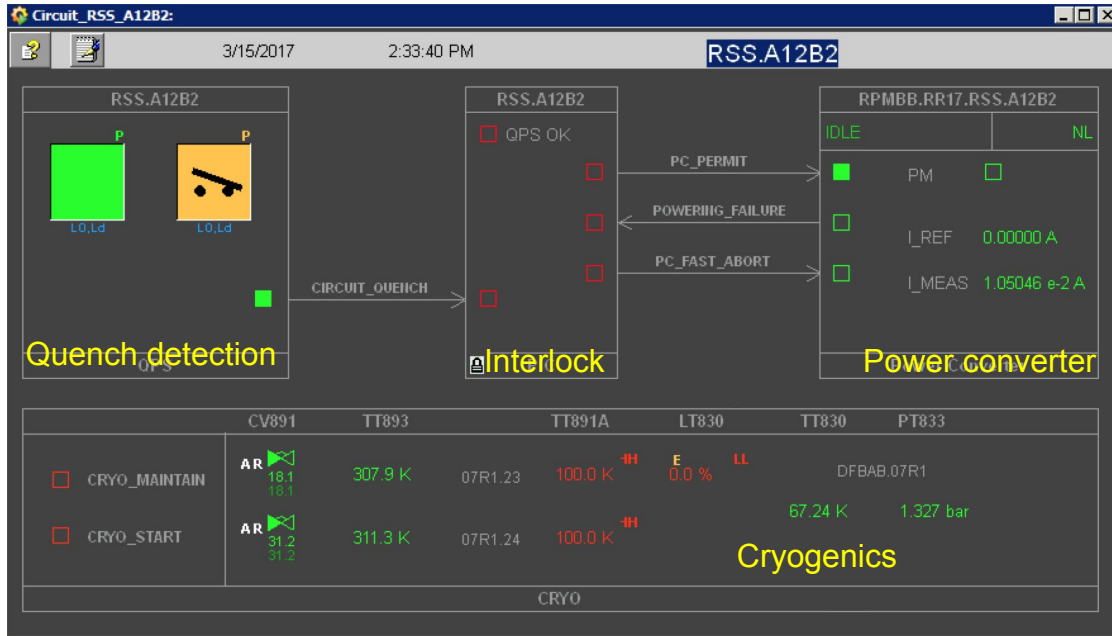
Tools: LHC circuit supervision



- ▶ Operational tool, intended to provide an LHC wide synthetic view for the >1600 magnet circuits
- ▶ Main aim is to quickly find and identify the root cause of events
- ▶ First level of granularity: sector (then circuits, powering/protection systems and finally individual electronic cards)



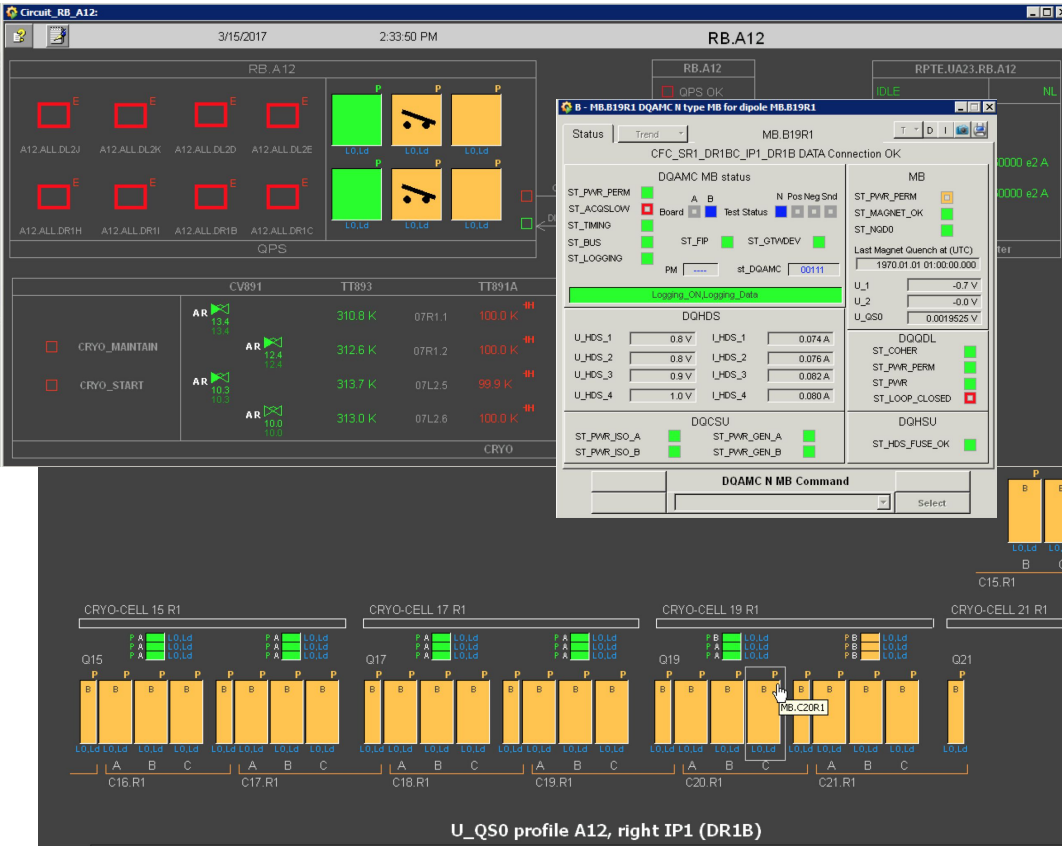
Tools: circuit supervision



- ▶ Second level of granularity: the magnet circuit
- ▶ Comprehensive circuit view, includes devices and ancillaries
- ▶ Allowing for easy identification of root cause



Tools: circuit supervision, into the device



- ▶ Third level of granularity: the protection device
- ▶ Detailed device status, operational commands
- ▶ Display and verify configuration parameters



Overview

- ▶ Software stack & architecture
- ▶ Tools for operators and experts
- ▶ **Collection of data**
- ▶ Known shortcomings & planned evolutions



Collection of data

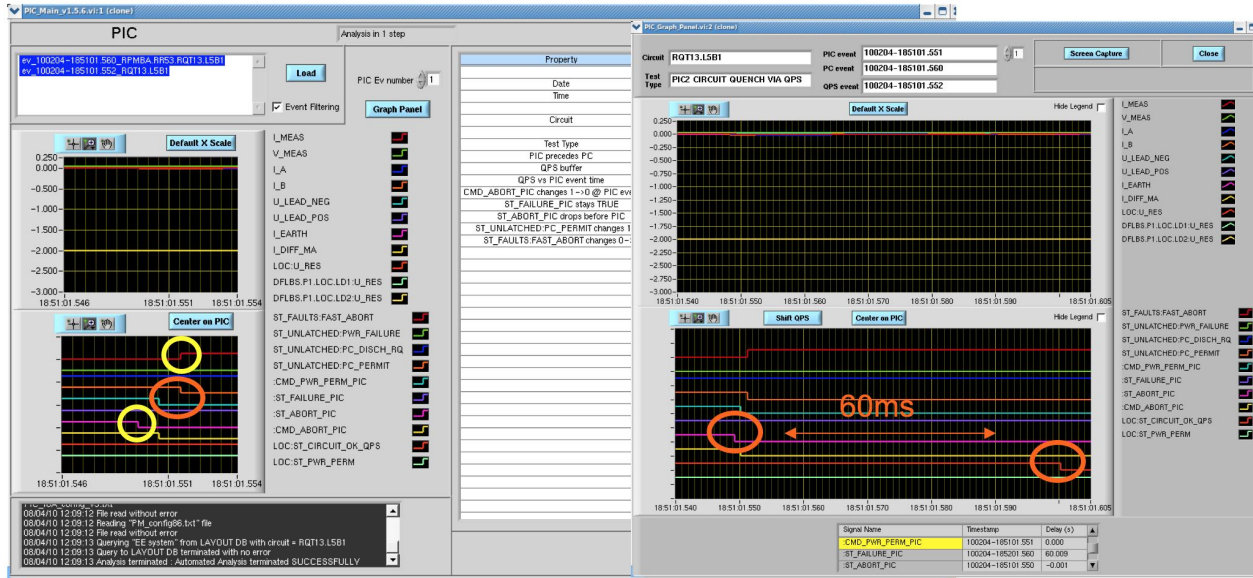
The screenshot displays the PIC SUPERVISION v5.6 interface for the LHC Powering Interlocks System. The main window shows a schematic with various interlock components (CIP-AR1 to CIP-AR6) and points (Point 4, Point 5, Point 6). A 'History Buffer' window is open, showing a list of events for item 'ROT13 R1B2'.

Local Time	Source	Type	Item	Description	Message	Status	Invalid
2010.07.27 01:23:36.842	Input	BI	ROT13 R1B2	Extended D. S. Tuning trim quad	ST_FALLURE_FIC	BAD	<input type="checkbox"/>
2010.07.27 01:23:36.843	Output	BO	ROT13 R1B2	Extended D. S. Tuning trim quad	CMD_ZWR_PERM_FIC	BAD	<input type="checkbox"/>
2010.07.27 01:23:36.851	Input	BI	ROT13 R1B2	Extended D. S. Tuning trim quad	ST_ABORT_FIC	BAD	<input type="checkbox"/>
2010.07.27 01:23:36.852	Output	BO	ROT13 R1B2	Extended D. S. Tuning trim quad	CMD_ABORT_FIC	BAD	<input type="checkbox"/>
2010.07.27 01:23:37.898	External Systems	CMW	ROT13 R1B2	Power Permit from OPS to start powering of circuit	ST_OPS_OK_BOOL	BAD	<input type="checkbox"/>
2010.07.27 01:23:58.504	External Systems	CMW	ROT13 R1B2	Power Permit from OPS to start powering of circuit	ST_OPS_OK_BOOL	OK	<input type="checkbox"/>
2010.07.27 01:43:24.810	Input	BI	ROT13 R1B2	Extended D. S. Tuning trim quad	ST_FALLURE_FIC	OK	<input type="checkbox"/>

- ▶ Interlock systems play a central role in event analysis as signals from many systems are connected (and logged) by such systems
- ▶ Accurate interlock history buffers are in the LHC the sole key to reliably resolve the event sequence for powering events
- ▶ Timing accuracy of <1ms required



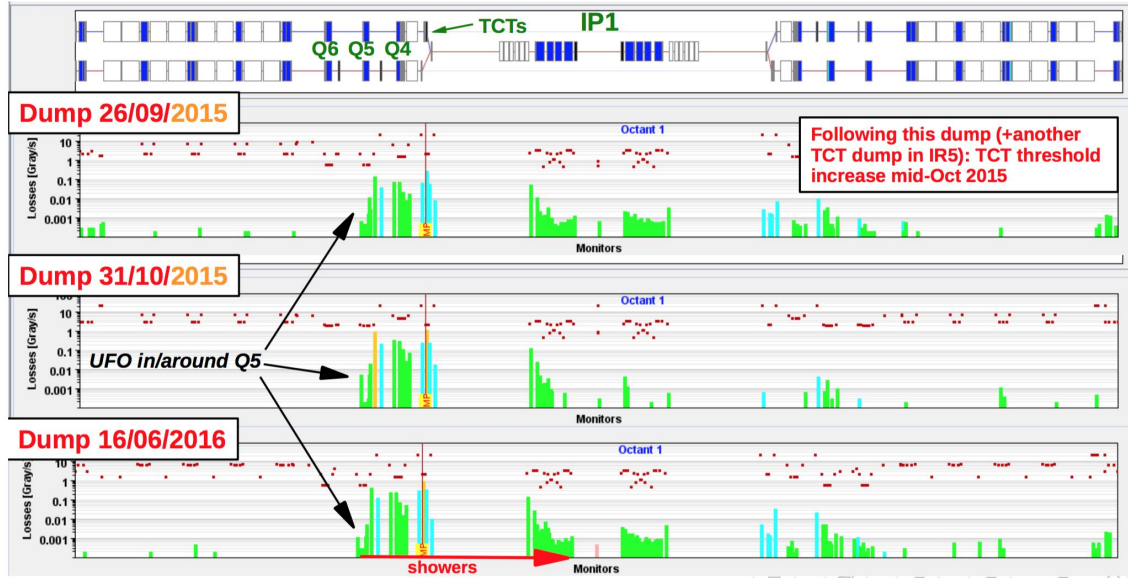
Collection of data



- ▶ Due to differences in timestamping source and mechanisms (local vs remote/gateway timestamping, central timing vs NTP...), identical signals can get timestamped with insufficient accuracy



Collection of data



- ▶ Typical LHC example: Losses from (dust) objects interacting with beam - did the beam losses trigger the quench or did the quench trigger the beam losses?
For a deeper look, see presentation by Zinur later this morning



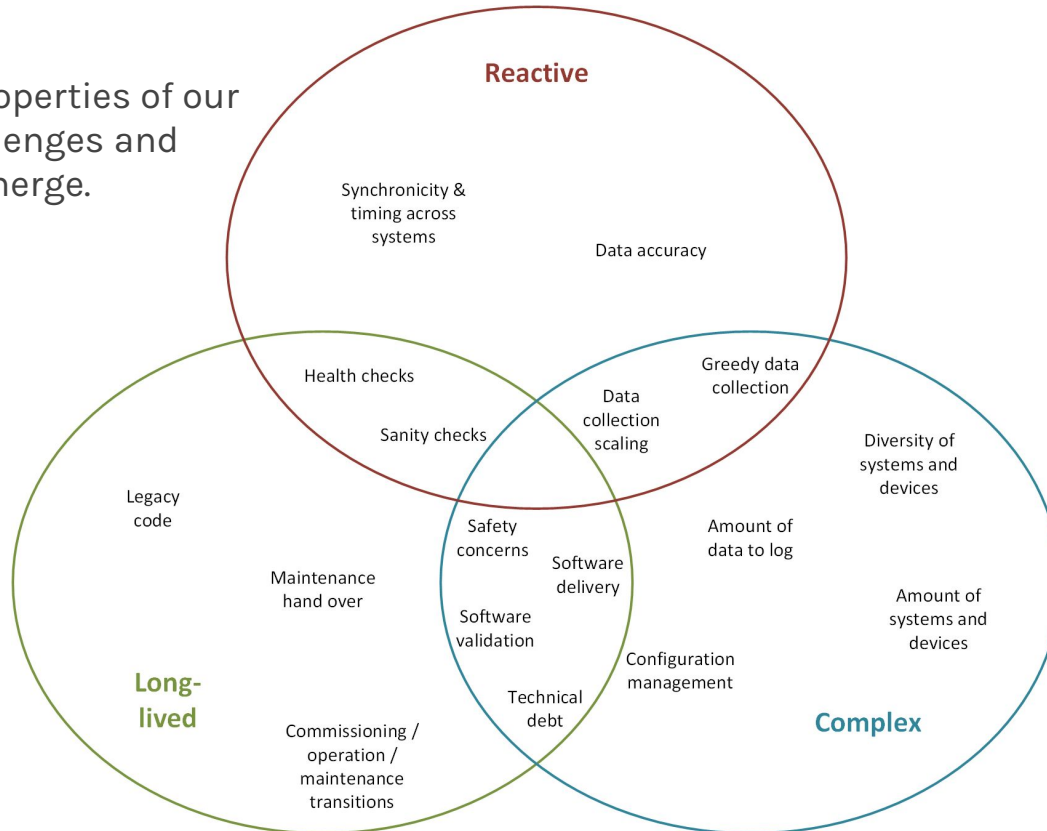
Overview

- ▶ Software stack & architecture
- ▶ Tools for operators and experts
- ▶ Collection of data
- ▶ Known shortcomings & planned evolutions



Shortcomings & challenges

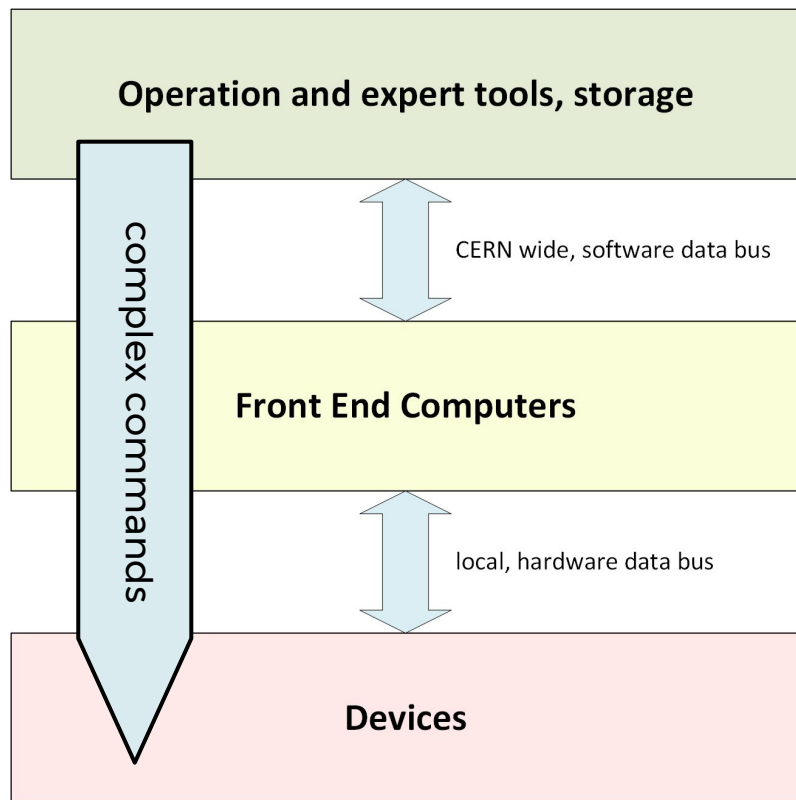
From 3 inherent properties of our system, many challenges and potential issues emerge.



Note: non exhaustive, non quantitative representation



Example - Commissioning / Operation transition

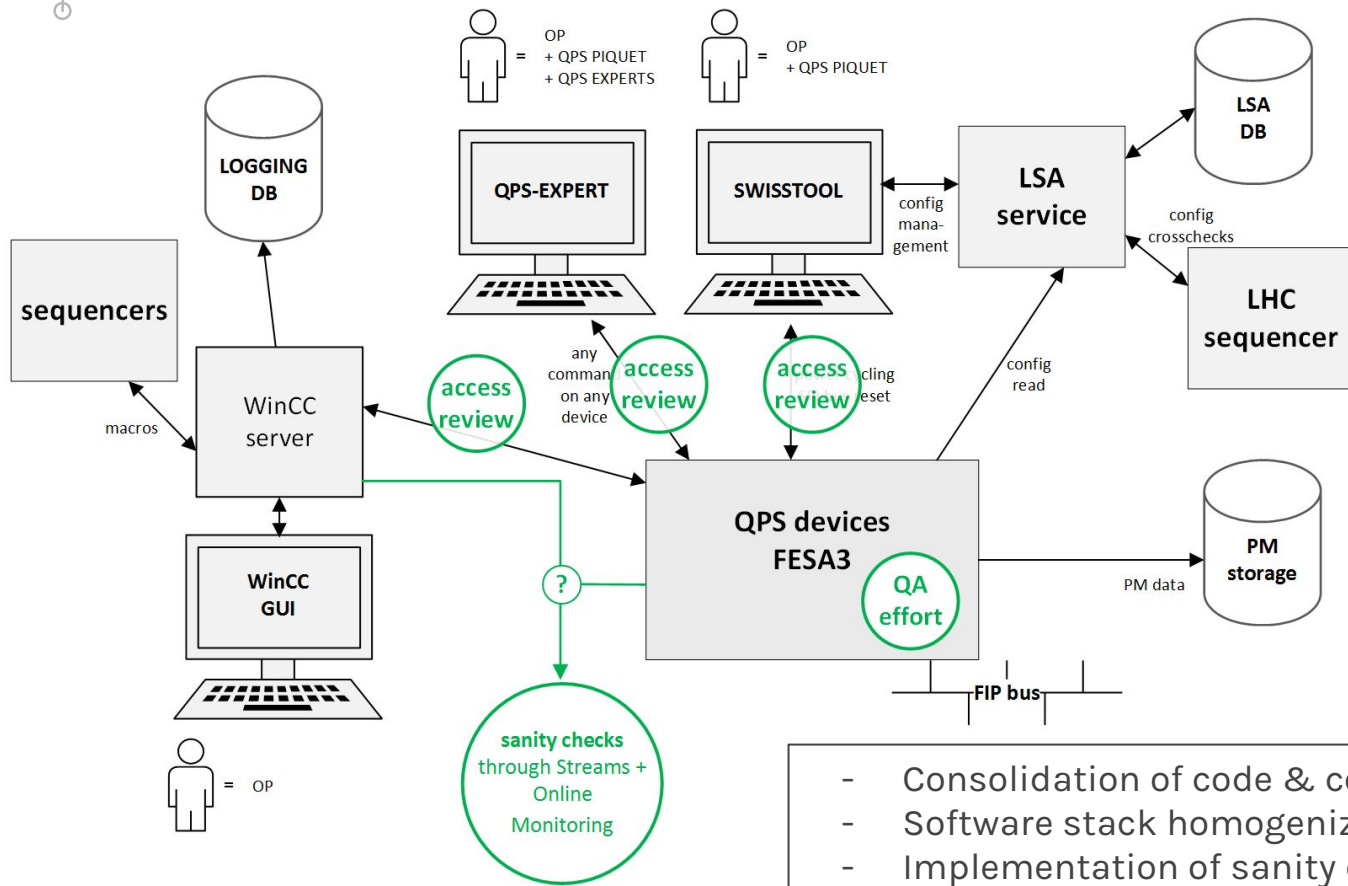


Low-level control,
from **high-level** applications

- Crosses all abstraction layers
- *Desirable* during commissioning
- *Risky* during operation
- Requires cautious handling when developing, configuring and delivering software
- Difficult to get around once in place



Example: QPS planned evolutions





Thank you

Questions?