Proposta per uso di rivelatori a strip per il tracciatore di FOOT.

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Napoli, 25-26 maggio 2017

Origin and Motivations

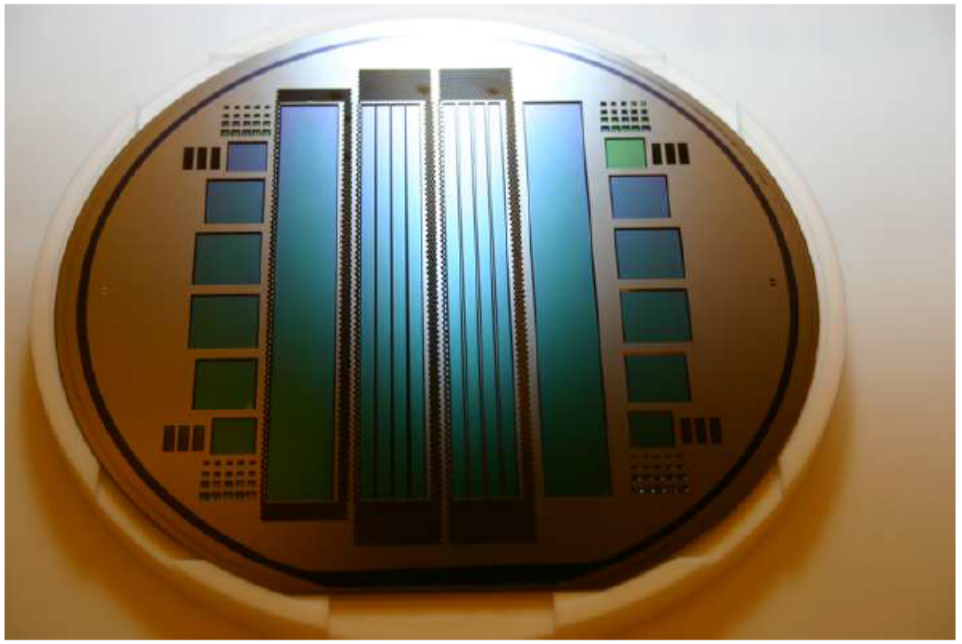
The work of this proposal has started after the last meeting of INFN CSN 3 in march, when it became clear the the Perugia group could no longer try to work on the pixel solution for the FOOT tracker and vertex.

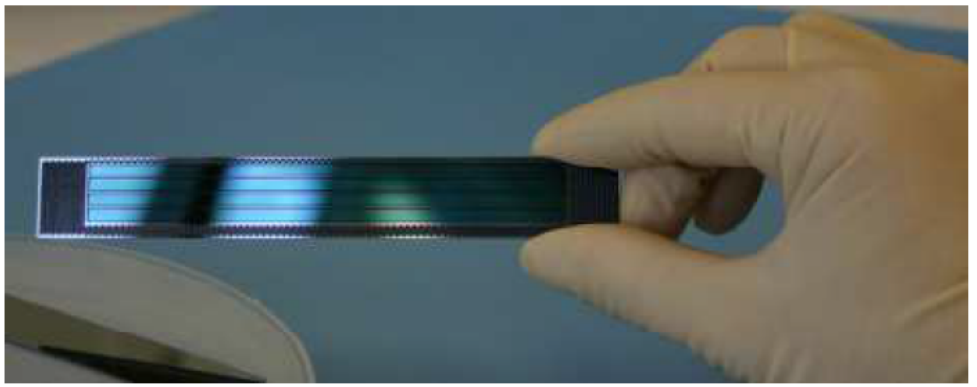
Scientific motivations lies in proposing a solution for the Inner Tracker that could overcome some of the problems that the pixel solution would face.

1) To reduce multiple scattering we need to reduce silicon thickness at least to 50 μm level.

→ this has already been done by several groups (ILC, UFSD)

Moser H. G. et al., **Thinned Silicon Detectors**, POS (Vertex 2007) 013

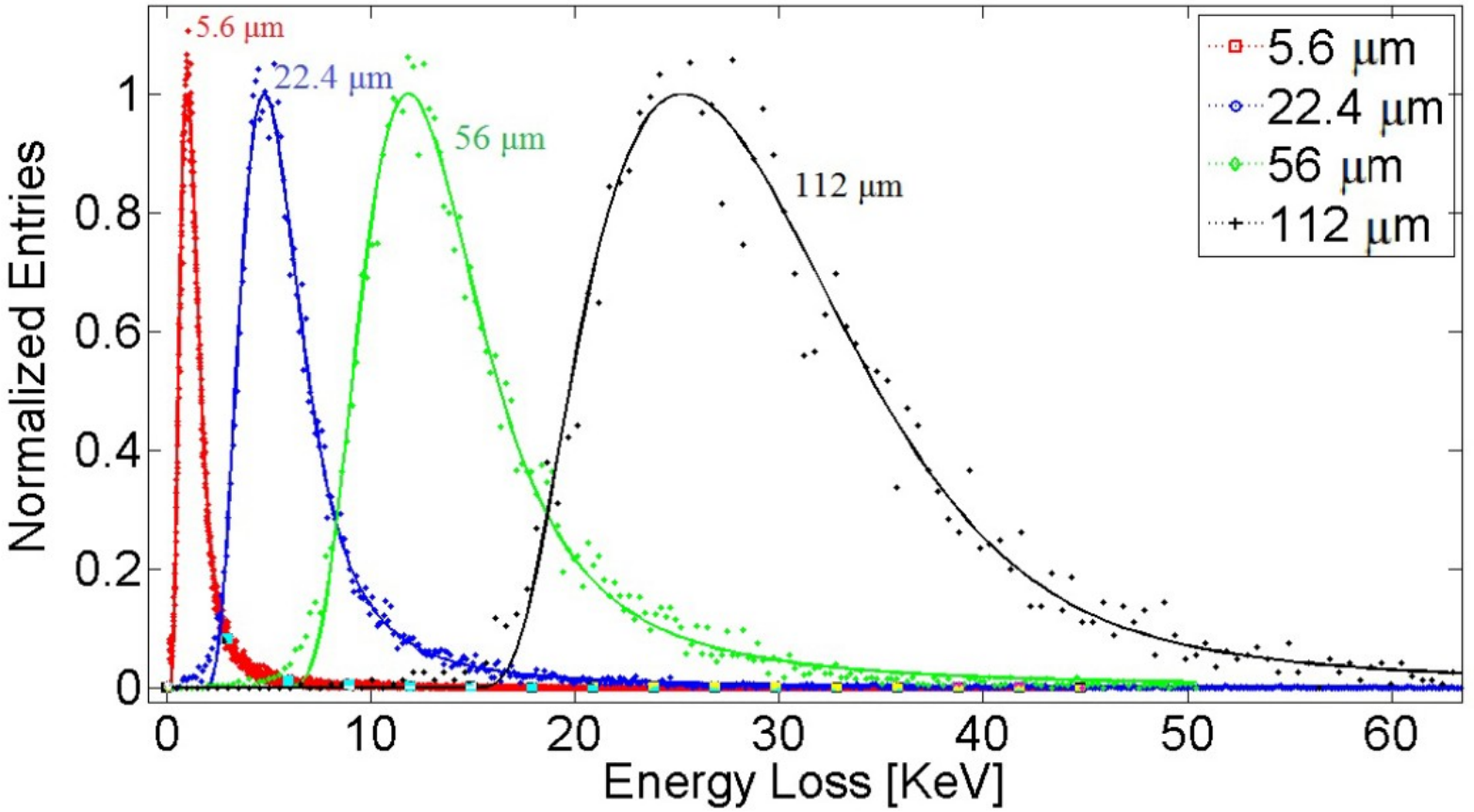




10.0 x 1.3 cm²

Figure 2: *Photograph of the backside of a 6" SOI wafer with areas thinned to 50μm. The large areas in the center correspond to ILC like modules, (10cm × 1.3cm), with and without reinforcement strips. The small structures in the periphery are test diodes.*

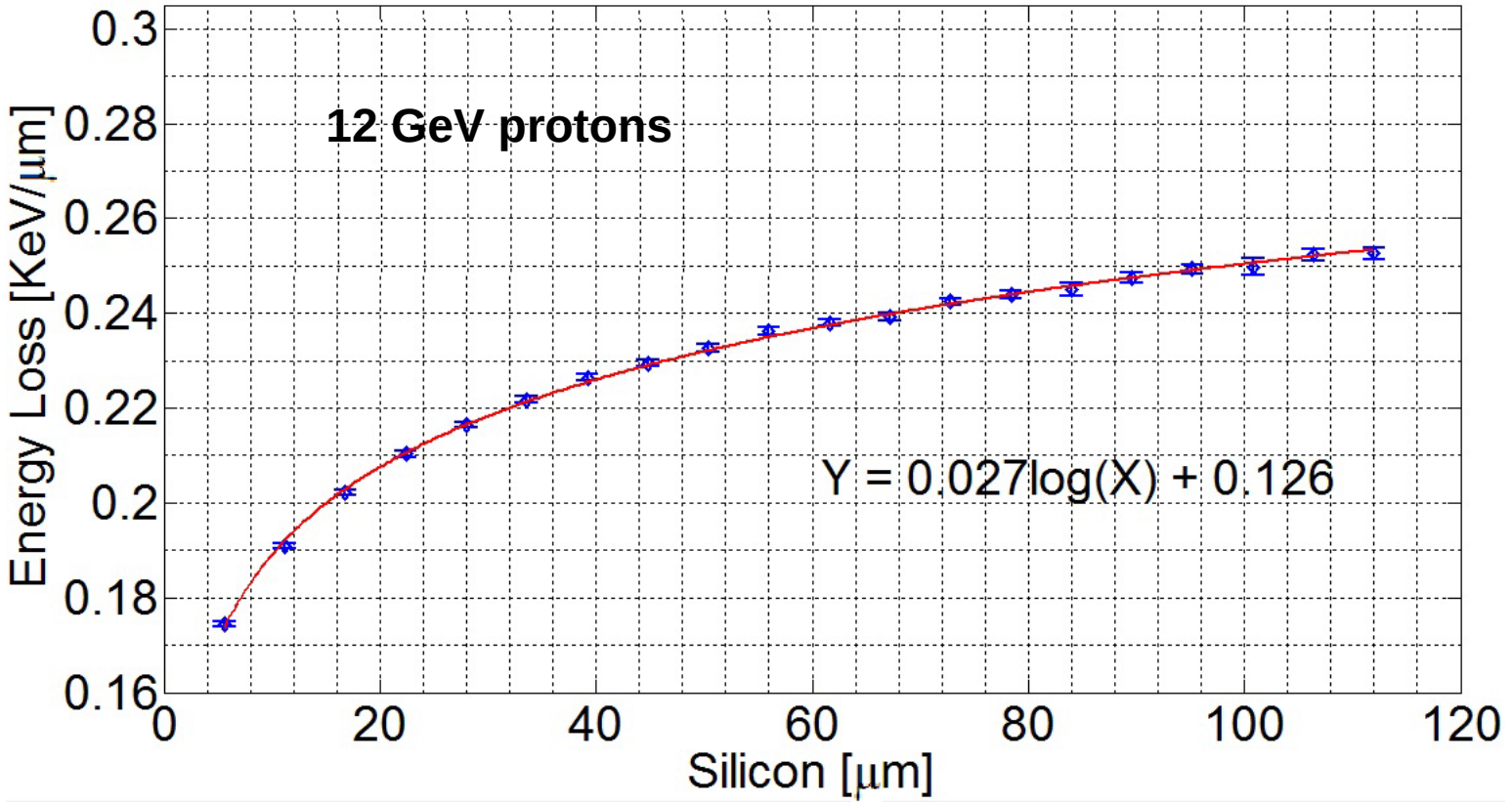
Thinning → signal reduction, more than proportionally below 100 μm



L. Servoli et al.: **Energy loss measurement for charged particles in very thin silicon layers.** Journ. of Instr. 6 P06013 (2011) 001-011

For 12 GeV protons @ 50 **μm thickness** we have:

MPV = 63 e-h / μm → 3150 e-h pairs (noise > 1000 electrons)

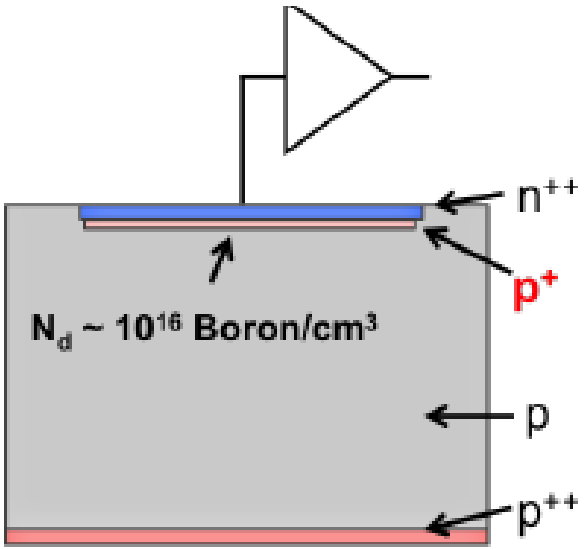


L. Servoli et al.: **Energy loss measurement for charged particles in very thin silicon layers.** Journ. of Instr. 6 P06013 (2011) 001-011

How to recover signal, hence S/N?

→ Signal amplification on strip LGAD:

$E \sim 300\,\mathrm{kV/cm}.$



Low gain avalanche detectors

Gain ~ 10 possible.

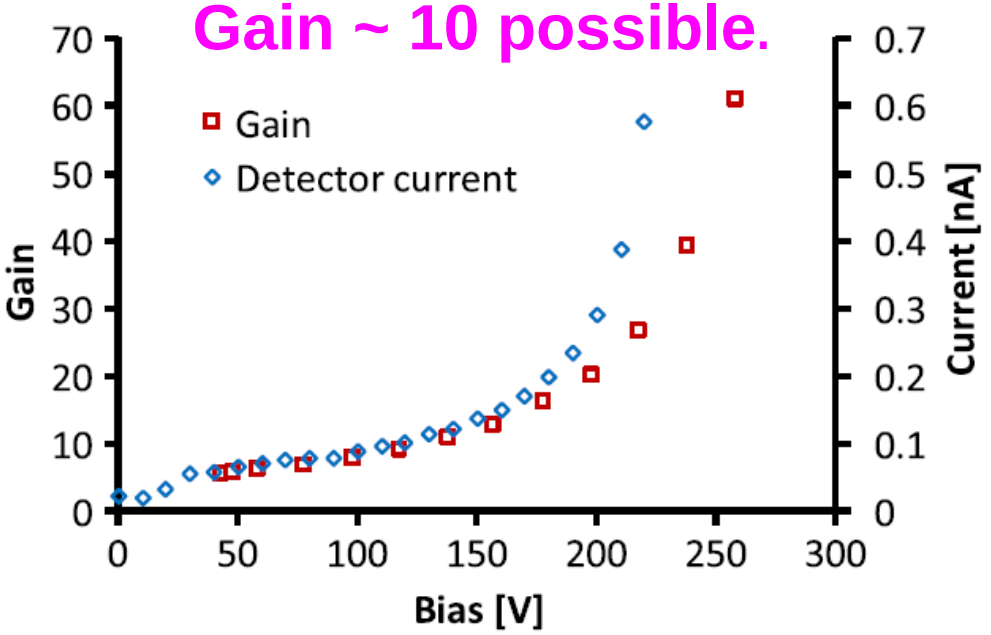


Fig. 1. Bias dependence of the leakage current and the signal gain for a 45 µm-thick UFSD sensor with an area of 1.7 mm^2. The gain determination is subject to an overall scale uncertainty of 20%. The similar exponential behaviour of gain and sensor current below 200 V bias is due to the common charge multiplication mechanism.

Radiation damage: $10^{14}\ n_{eq}/cm^2$ without loss of performance.

R. Arcidiaconoi et al.: **Test of UFSD Silicon Detectors for the TOTEM Upgrade Project,** arXiv:1702.05180 [physics.ins-det] 16 feb. 2017

Are already there thinned LGADs?

Yes. ***There is a batch in production at FBK, 50 μm thin to be delivered to N. Cartiglia group (Torino).***

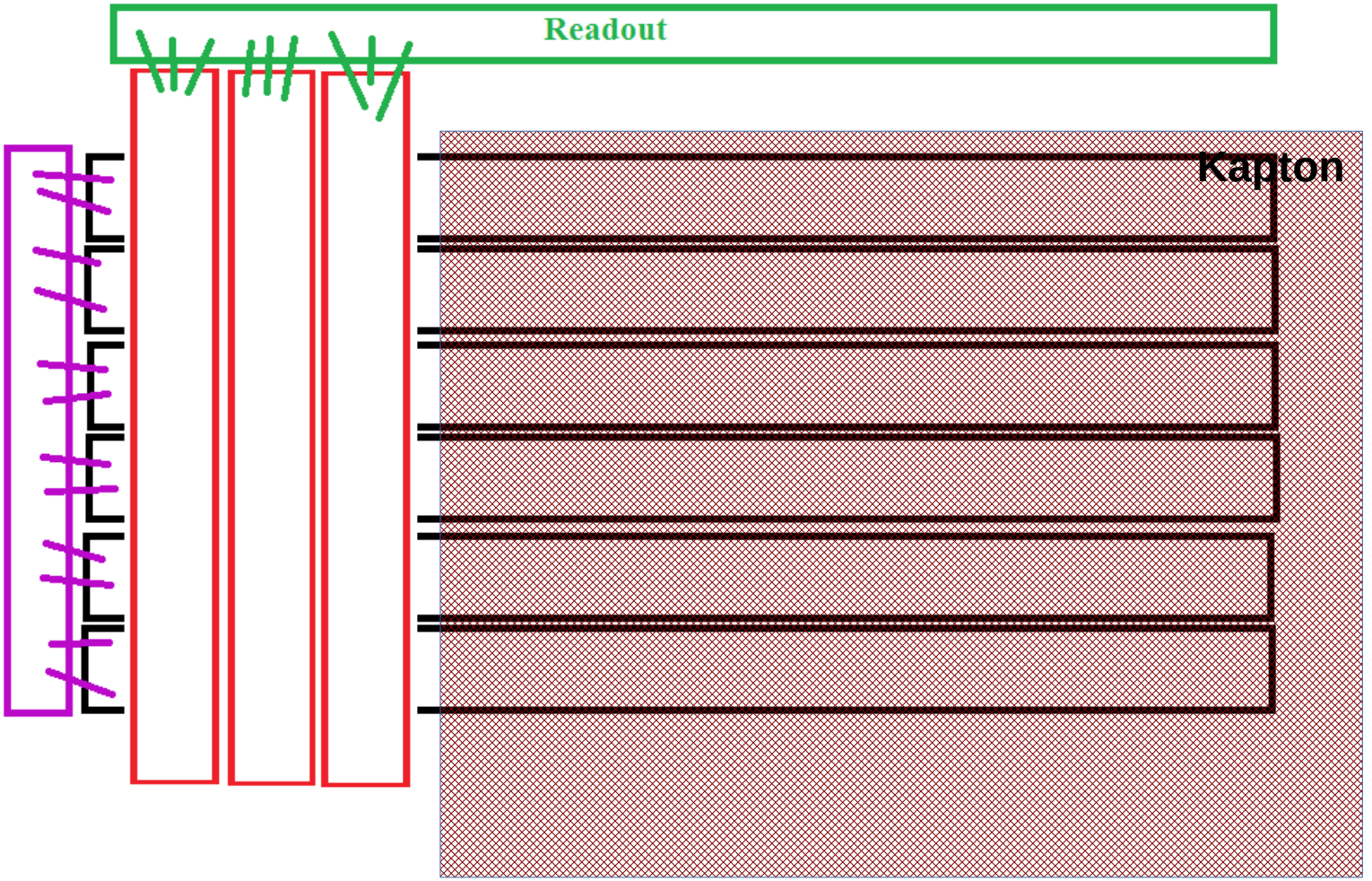
We have already discussed with him and he confirmed that:

1) thinning can be made in most of the 6” wafer area (9.5x9.5 cm^2 at maximum), excluding external regions, to be left thick for mechanical reasons.

2) he is willing to cooperate in an investigation on the suitability of such devices for proton and ion detection.

3) we could have some of the prototypes now in production to start some testing in summer.

Mechanical setup



→ Readout outside the beam region.

→ **Reduction of dead space**

Each silicon layer thinned to thickness: 50 micrometers ;

Two layers glued via biadhesive kapton foil, 30 micrometer thickness;

Total thickness: 115 micrometer silicon equivalent.

It could be even less if thinner silicon (25 micrometers) could be machined and used.

Support ring (aluminum? steel?) larger than the beam spot;

→ **sensor area with uniform density and thicknes**

How many readout channels?

To obtain spatial resolution < 30 μm → 125 μm strip pitch, analog readout. **(AMS).**

→ 8 x 8 cm^2 instrumented area → 80000 μm /125 μm = **640 strips per coordinate.**

→ **1 DAMPE readout chip: 64 channels => 10 chips per coordinate.**

→ **we need two planes with both coordinates, → 40 chips + 10 chips spare.**

→ **Hybrid for front-end chip (TFH): hosts readout chips + bias + services. (essentially same design of DAMPE hybrids)**

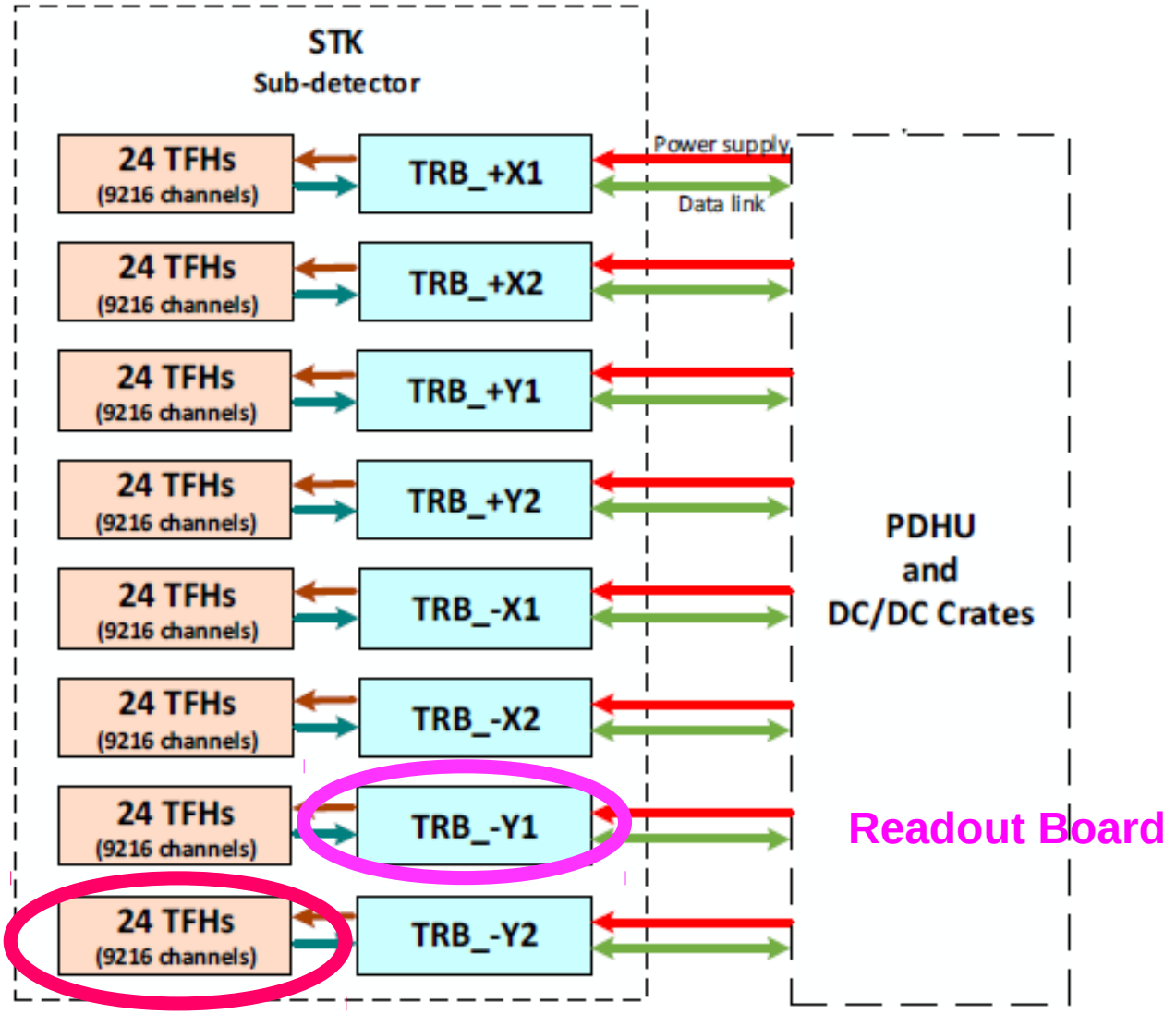
→ **Readout board (TBR) to host connection with computers and links to/from Hybrids**

Baseline: the DAMPE front-end – hybrid – readout board chain.

Reuse as much as possible:

DAQ chain based on DAMPE chain.

Preams: +- 200 fC



Hybrid with readout chip

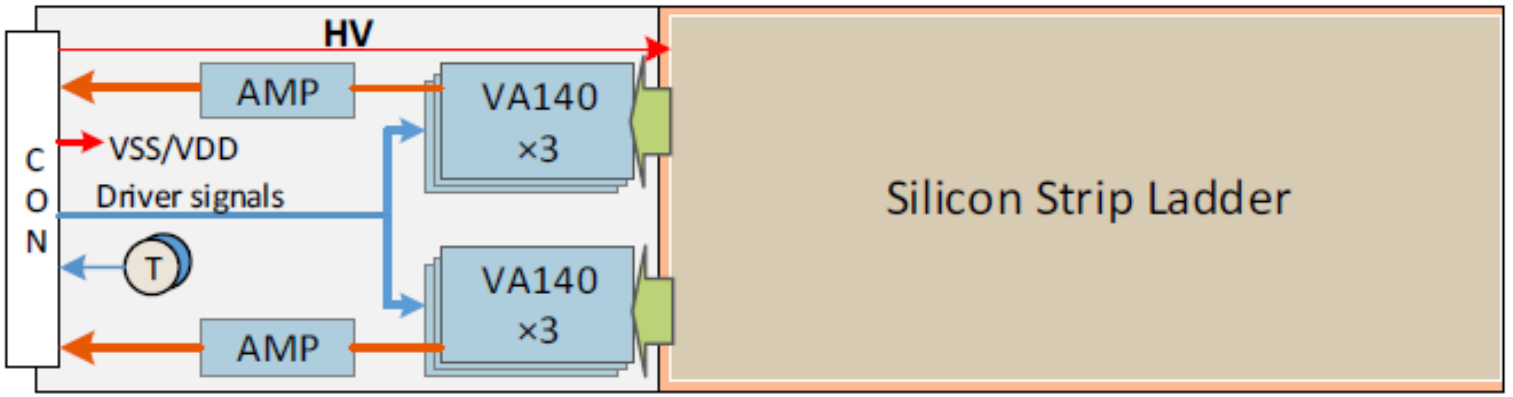
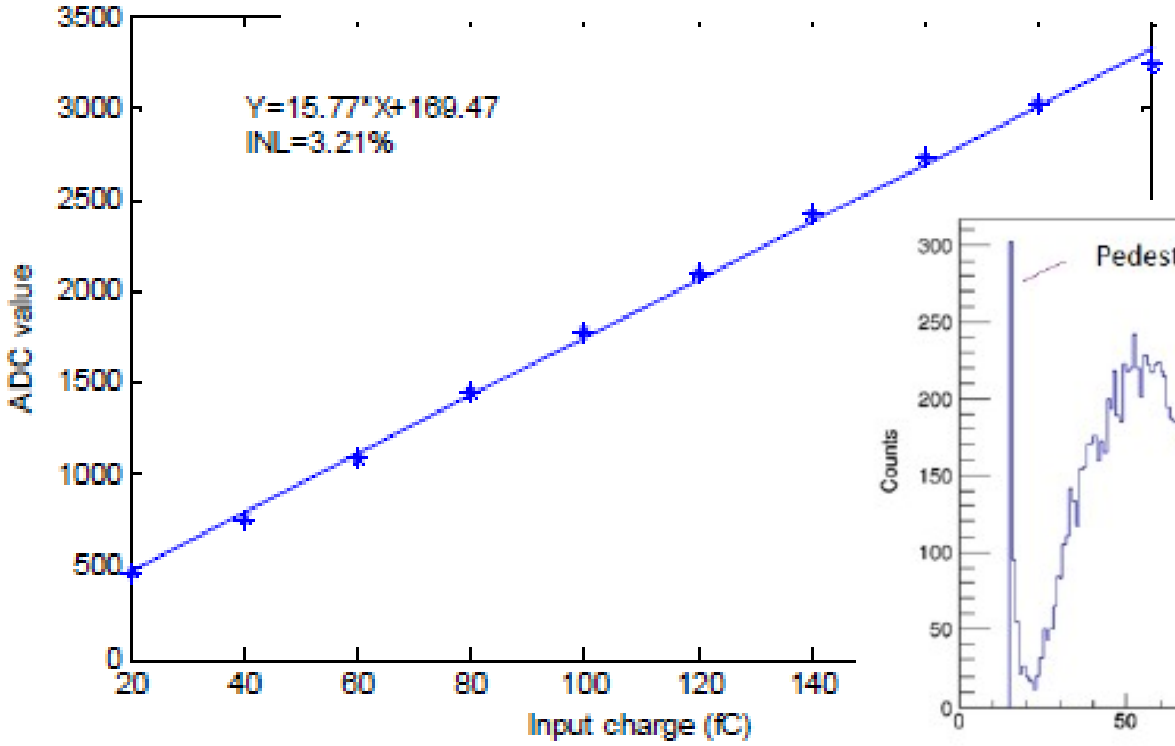
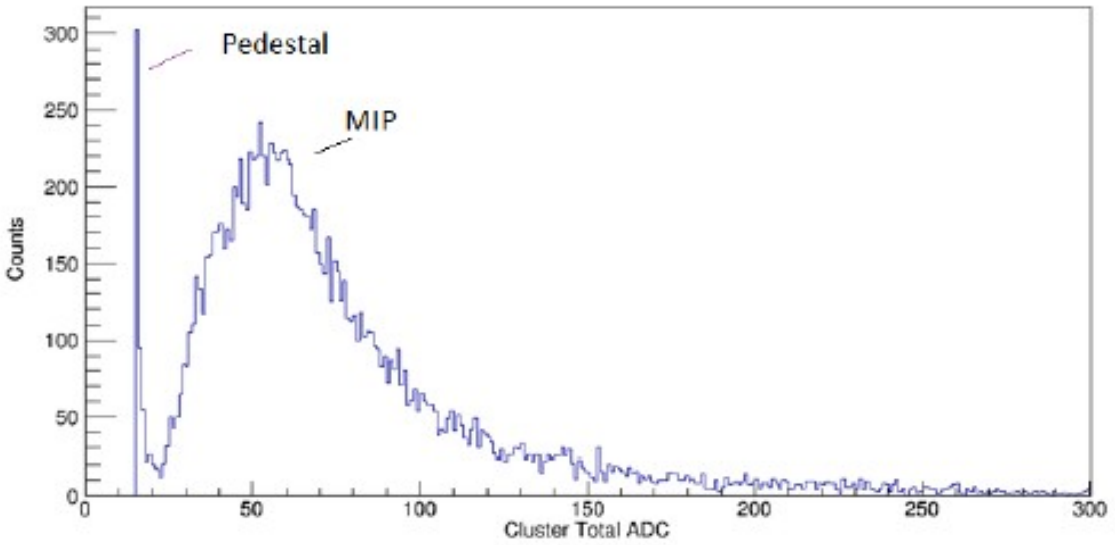
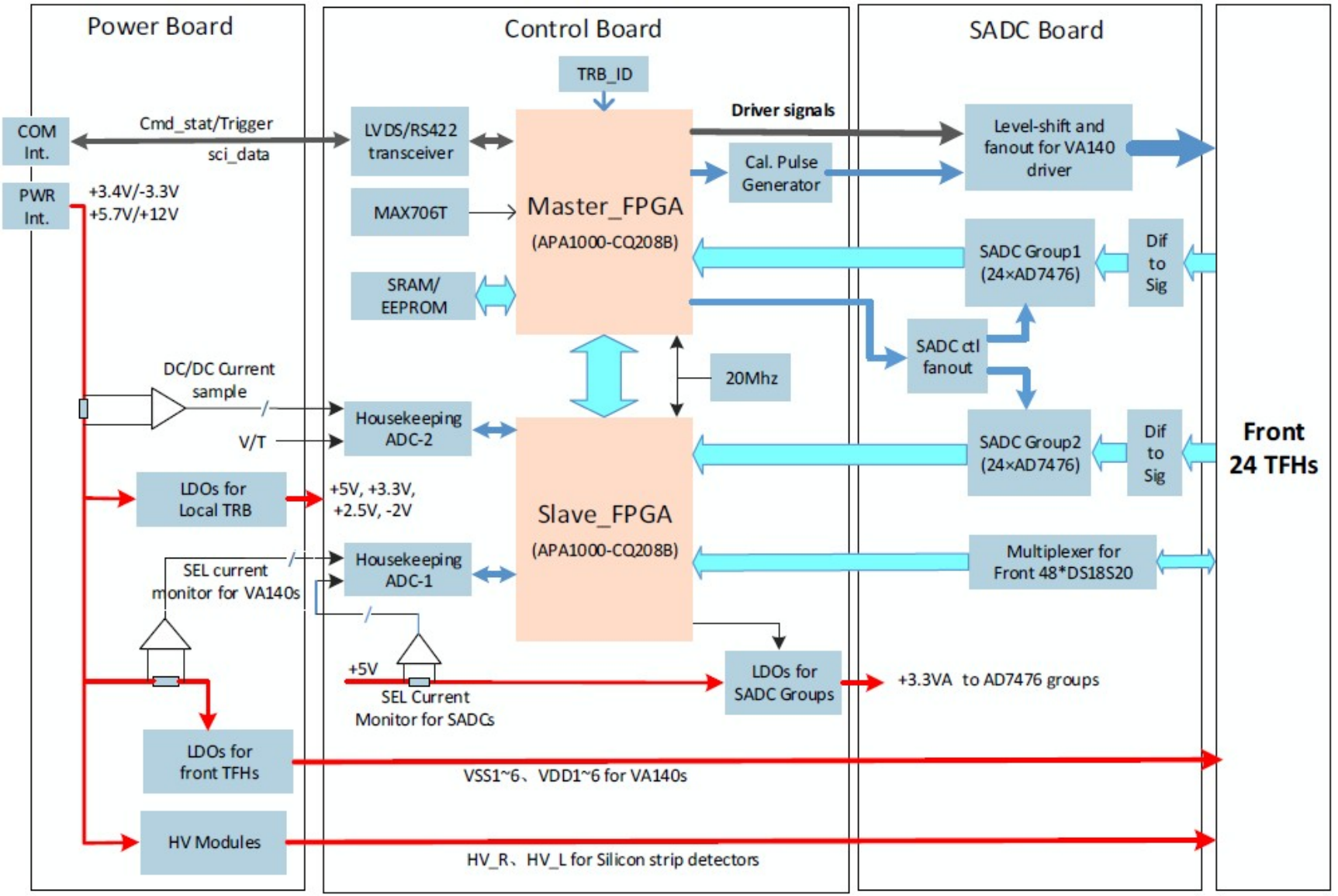


Fig. 6. Block diagram of a TFH





TRB board


Power Board
Control Board
SADC Board
TRB_ID
COM Int.
Cmd_stat/Trigger
sci_data
PWR Int.
+3.4V/-3.3V
+5.7V/+12V
LVDS/RS422 transceiver
MAX706T
SRAM/ EEPROM
Master_FPGA
(APA1000-CQ208B)
Driver signals
Cal. Pulse Generator
Level-shift and fanout for VA140 driver
SADC Group1 (24×AD7476)
Dif to Sig
SADC ctl fanout
SADC Group2 (24×AD7476)
Dif to Sig
20Mhz
DC/DC Current sample
V/T
Housekeeping ADC-2
LDOs for Local TRB
+5V, +3.3V, +2.5V, -2V
Slave_FPGA
(APA1000-CQ208B)
Housekeeping ADC-1
SEL current monitor for VA140s
Multiplexer for Front 48*DS18S20
+5V
SEL Current Monitor for SADCs
LDOs for SADC Groups
+3.3VA to AD7476 groups
LDOs for front TFHs
VSS1~6、VDD1~6 for VA140s
HV Modules
HV_R、HV_L for Silicon strip detectors
Front 24 TFHs

HV board

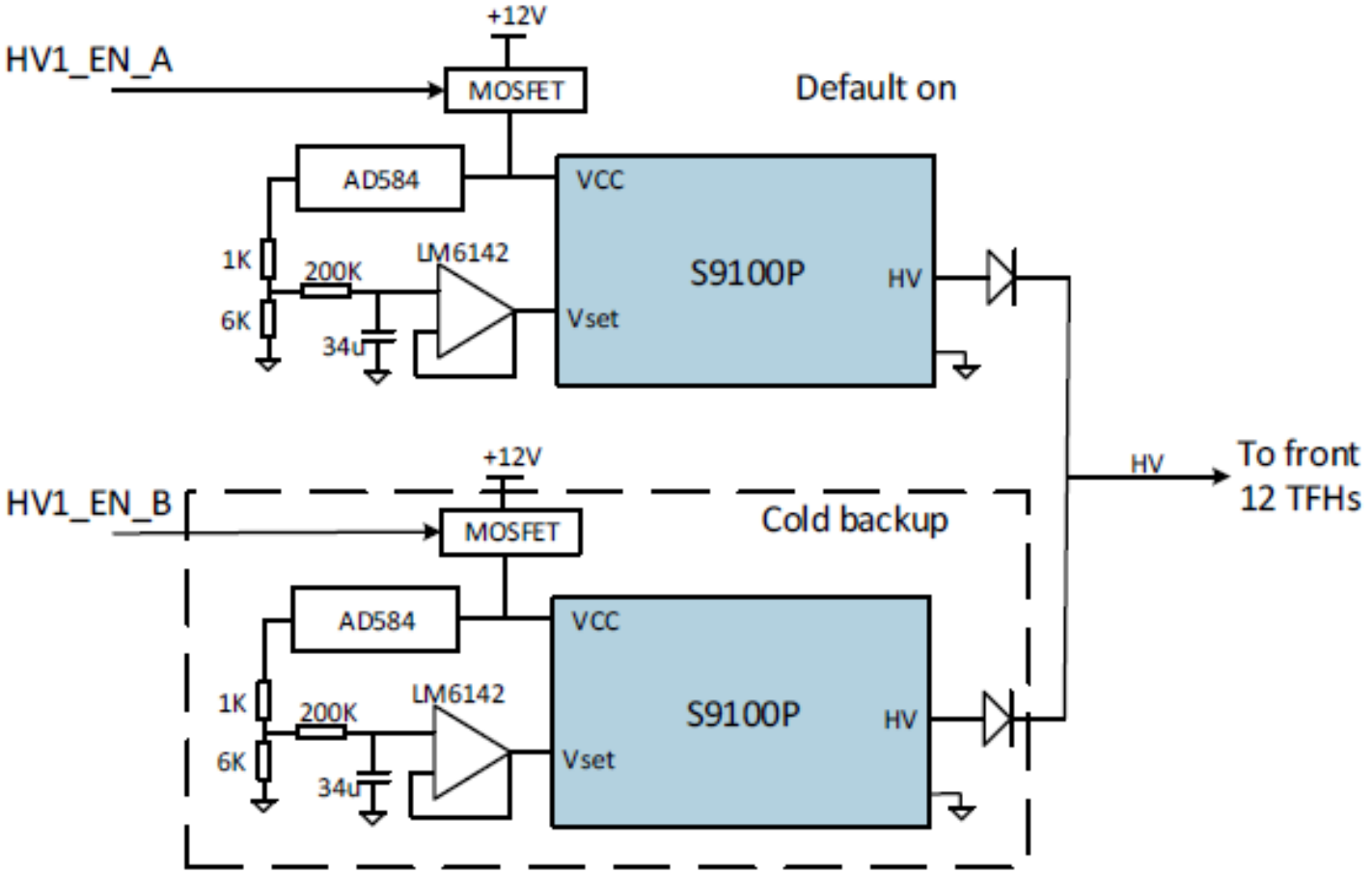


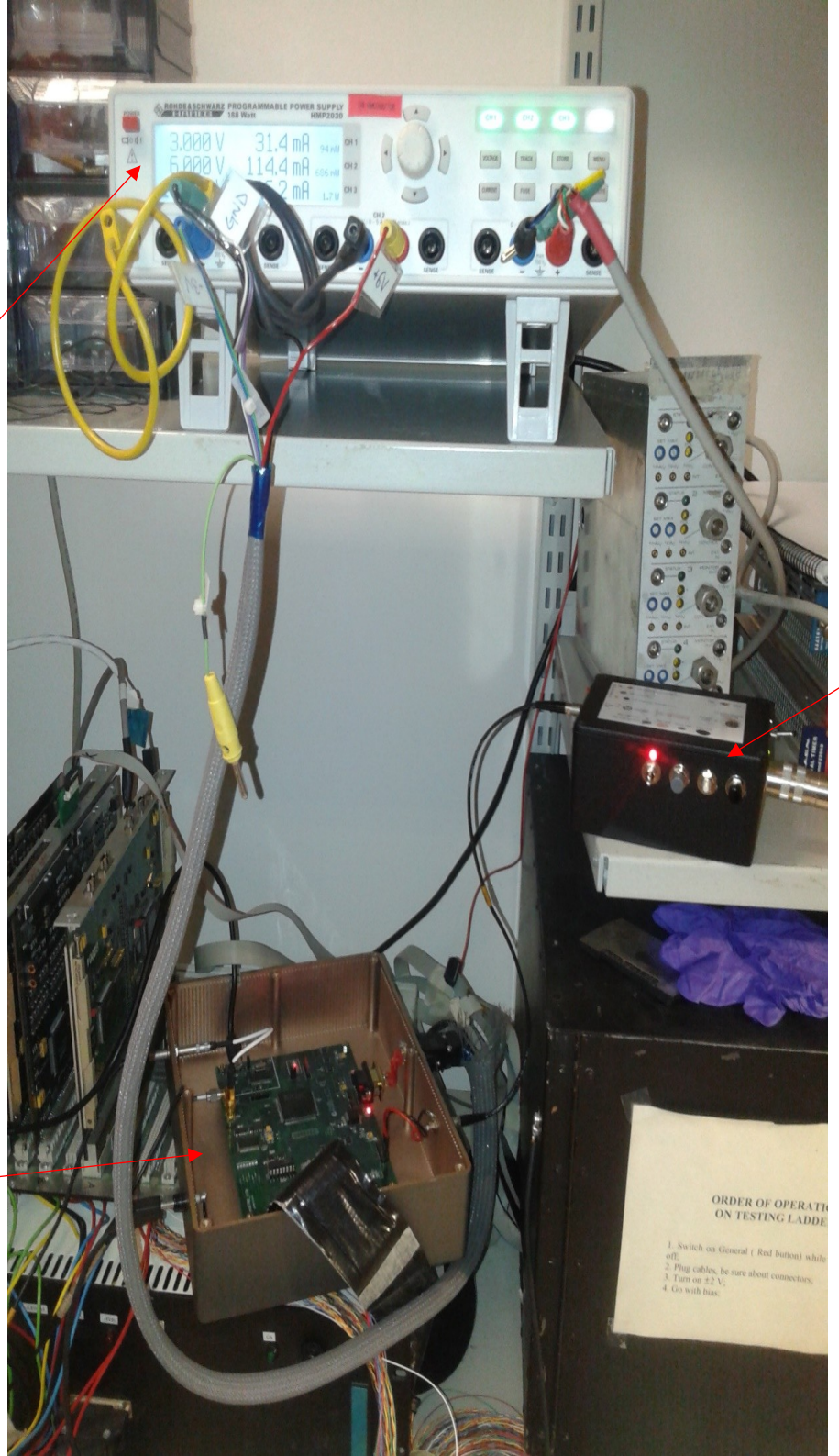
Fig. 8. Circuit for a HV-generator group

Laboratory Setup for Dampe Ladder Test

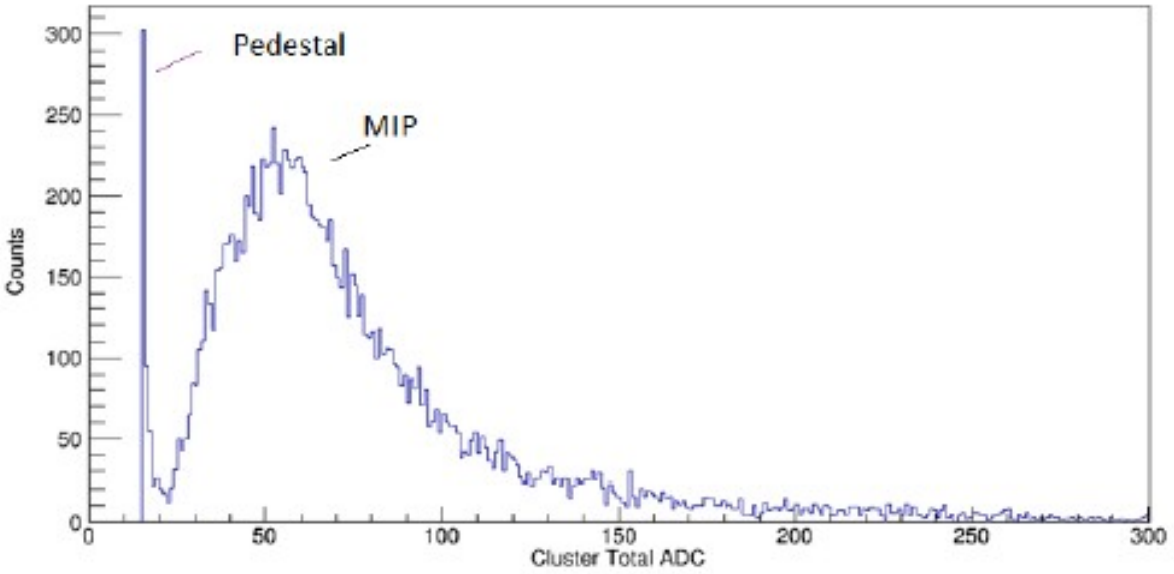
ROHDE&SCHWARZ
Programmable Power
Supply
HMO2030

BIAS Box

MiniTRB



Some rough computation on dinamic range and Signal…..



50 ADC / MIP (@300 μm)

→ 8.3 ADC /MIP (@ 50 μm)

→ 83 ADC / MIP (@ 50 μm with LGAD = 10)

Cost estimate

→ 1 FBK run = 80 k€ (12-15 wafers) . If MPW, our costs decrease.

In each wafer we could reserve 3 sensor 8 x 1 or 2 sensor 8 x 2 cm^2 to have 36-46 sensor 8x1 cm^2 or 24-30 sensor 8x2 cm^2.
In first hypothesys we do need 32 sensors + spares, and we will use about 30% of wafer. (24 k€)
In second hypothesys we do need 16 sensors and we use 40% of wafer. (32 k€)
Costs should decrease proportionally.

→ jig development to handle and mount sensors + kapton (5 – 10 k€)

→ each readout chip costs 300 € → 15 k€ (50 chips)

→ hybrid front end → 500 € /piece → 5 k€ (8 + 2 spare);

→ Readout board (ADC +, digital communication) : 5 k€ ;

Hence, total costs: 54 - 67 k€ ;

Next steps in 2017:

1) Refine idea and get all the relevant information, mainly on mechanical stabiity.

2) obtain test devices from N. Cartiglia and bond to available DAMPE readout.

3) test in laboratory and also at beam test (November @ CERN) and in a proton and ion beam.

4) mechanical test of thinned layer of silicon glued to biadhesive kapton foil.