Remote FPGA configuration

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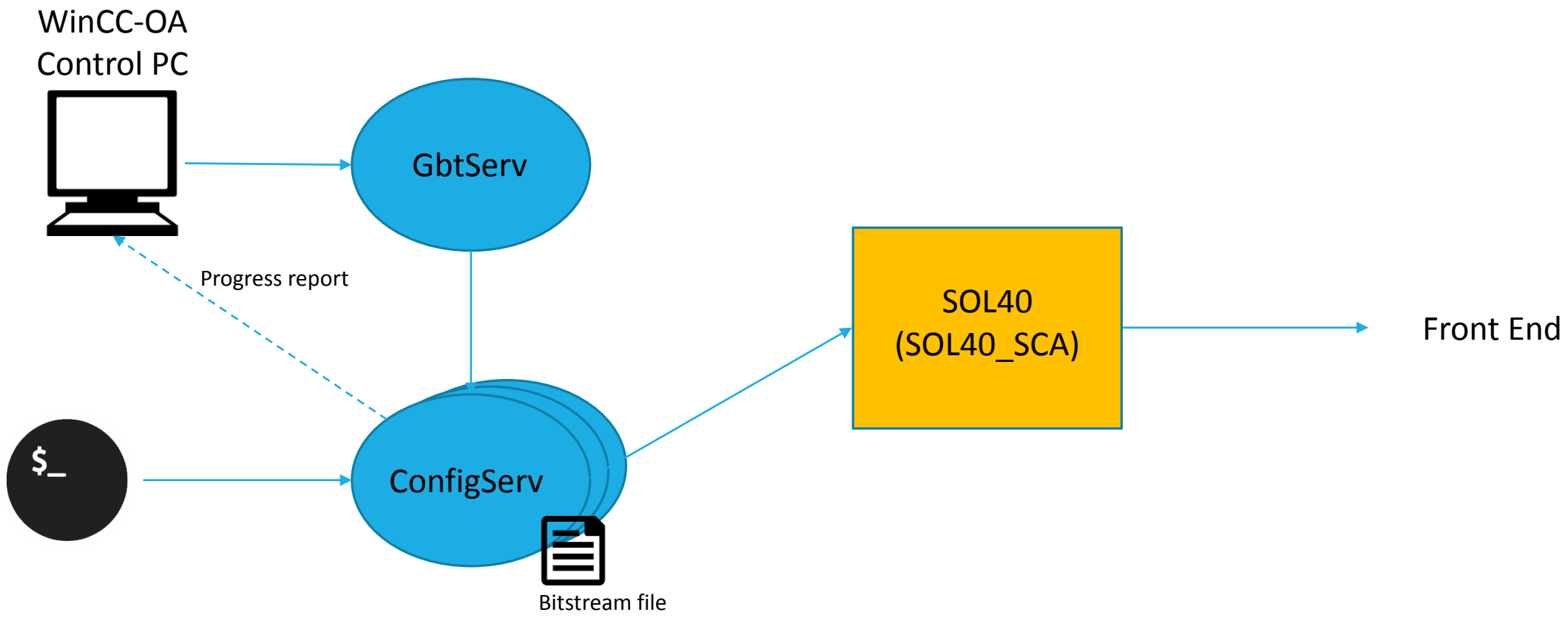
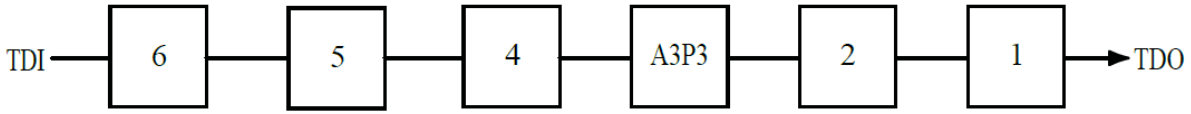
How it is done – control system integration



How to use (command line)

$ configure_kintex7 --gbt 3 --sca 0 --chain-len 6 --dev-index 2 --file pdmdb_top.6LinksOK.bit

$ configure_microsemi --gbt 3 --sca 2 --chain-len 6 --dev-index 2 --file cluster_fpga.dat –action PROGRAM



Additional parameters:

--control <control_reg> (see GBT-SCA manual, default 0x4200 for Kintex and 0x0 for Microsemi)

--frequency <val> (0 to 20000000, default 20Mhz)

--loglevel <val> (0 to 7, 7 is default)

--irlen <val> (default is 6 for kintex7 and 8 for microsemi)

Initially too much time!!

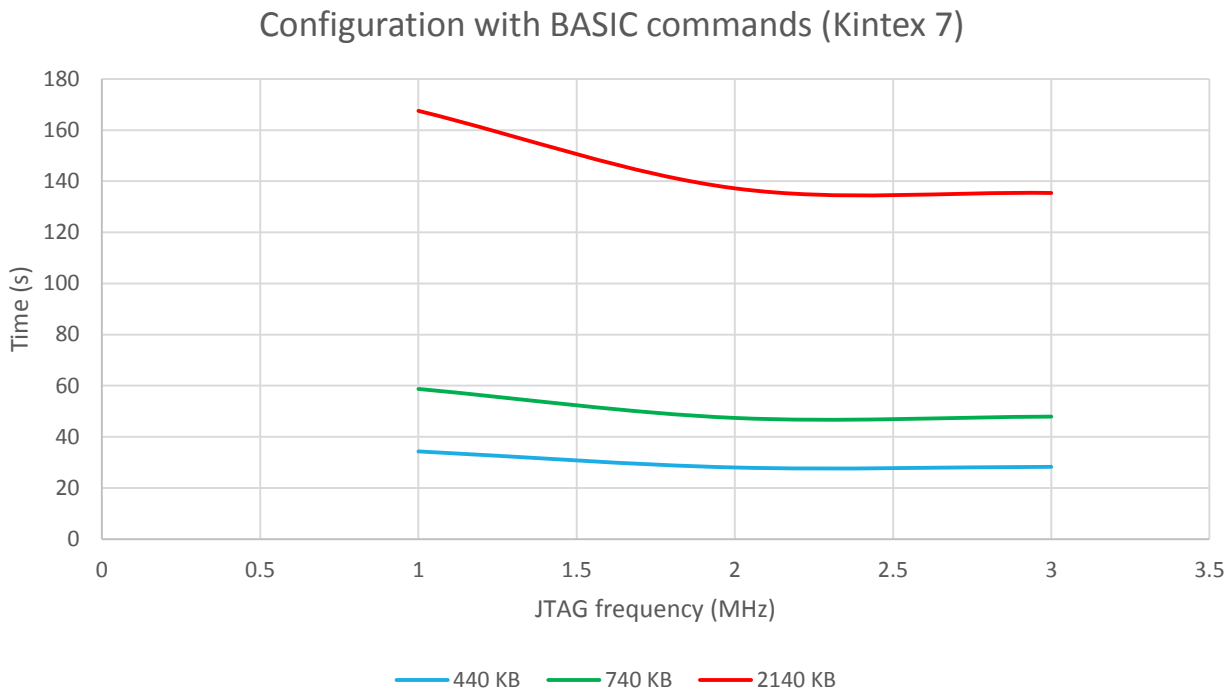
- Configuring a Kintex7 was taking 180 seconds at 20MHz JTAG frequency
- Configuring an IGLOO2 was taking 17 minutes

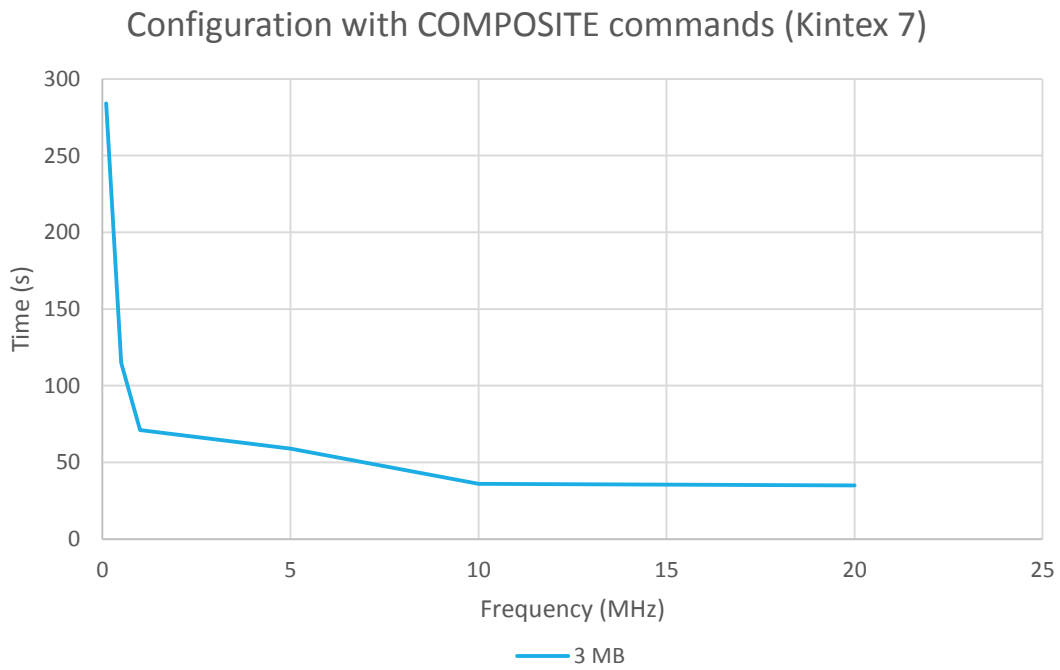
JTAG Composite commands (acceleration)

- Biggest factor for big configuration times is probing for replies in the SOL40_SCA from the software.
- Mitigated by implementing composite commands in firmware.

Basic commands	Composite commands
JTAG_W_TMS0(1, 2, 3) JTAG_W_CTRL JTAG_W_TDO0(1, 2, 3) JTAG_GO	JTAG_W_TMS JTAG_TDO_SCAN_OUT (5x reduction SCA software access)
JTAG_W_TMS0(1, 2, 3) JTAG_W_CTRL JTAG_GO JTAG_R_TDO0(1, 2, 3)	JTAG_W_TMS JTAG_TDO_SCAN_IN (5x reduction SCA software access)
JTAG_W_CTRL JTAG_GO JTAG_R_TDO0(1, 2, 3)	JTAG_TDO_SCAN_OUT (6x reduction SCA software access)

How long does it take ?





- Roughly 5x improvement for 3MB files on the Kintex 7 (180 s to 35 s)
- About 2.5x improvement for 5.6MB files on IGLOO2 (17 to 7 mins, to be improved)

Features now in place

FPGAs supported	Xilinx series 7 family	IGLOO2, SmartFusion2
Protocol used	JTAG	JTAG (check), SPI (debug phase)
Timing	~35 secs for 3MB file (15s compressed file)	7 min for 5.6MB file
Daisy chain	YES	YES
Actions	PROGRAM, READ_ID	PROGRAM, ERASE, VERIFY, READ_ID, READ_INFO
Partial Reconfiguration	NO	-
Progress report	YES	YES
ECS integration	Soon	

Tests performed

Subdetector	Successfully tested features	To be done
SciFi	JTAG FPGA config (microsemi), all actions	SPI FPGA config (microsemi)
CALO		JTAG FPGA config (microsemi)
Muon		SPI FPGA config (microsemi)
RICH	FPGA config daisy chain (compressed and uncompressed bitstream)	

When can we use it?

- Everything should be available with the next release of fwGbt libraries and the next merge to of TFCv4 branch to master
- GbtServer and tools should be released soon
- Will already be able to use the command line tools if you compile the minidaq firmware from TFCv4

Other news for the new release

- As requested, will be possible to send simple commands to the terminal in the CCPC through WinCC-OA (ls –a, pwd, etc..)
- Bug fix in SOL40_SCA that got the WinCC-OA managers and the GbtServer stuck when the control system tried to access SCAs that were not connected (pushed to TFCv4)
- Possible to configure the MiniDAQ firmware from the Control System (WinCC Project and ByteBlaster must be in the same machine)
- Closing and opening BAR0 and BAR2 access from WinCC-OA possible
- Loading ecs_driver from WinCC-OA possible