

CMS CPU benchmarking tests (short status)

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CPU Benchmarking testbeds

- Dedicated Worker nodes reserved for dedicated/controlled tests:

PIC (SLC6) → HT on/off

- E5-2640v3 2.60 GHz (td102.pic.es)
- E5-2650 2.00 GHz (td713.pic.es)
- E5-2650v2 2.60 GHz
- E5645 2.40 GHz (td608.pic.es)
- X5650 2.67 GHz (td550.pic.es)
- E5-2680v4 2.40GHz (new)

FNAL

- E5-2670v3 2.30GHz [48 threads/server]
- Xeon Phi Gen2 (Knight's Landing) 96 GB (lim.cores) [120 threads/server]
- ARM64 system 128GB [96 threads/server]
- E5-2680 v4 @ 2.40GHz [56 threads/server]

10 architectures

DB12 tests at PIC Tier-1

- Tests done so far on most available CPUs @ PIC Tier-1, increasing the number of processes until filling the machine (up to Logical Cores, HT on), running tenths of measures per config.

- DB12

- HS06

- KV

- ttbar GEN-SIM multithreaded (4 threads) CMSSW_8_4_0_patch2 from CVMFS

Special isolated simulation suite

- Time spent running tests:

- **DB12:** 6h (td102) + 32h (td550) + 13h (td608) + 20h (td713) = **71h**

- **HS06:** 55h (td102) + 48h (td550) + 52h (td608) + 54h (td713) = **209h**

- **KV:** 34h (td102) + 39h (td550) + 73h (td608) + 74h (td713) = **220h**

- **ttbar:** 89h (td102) + 72h (td550) + 48h (td608) + 47h (td713) = **256h**

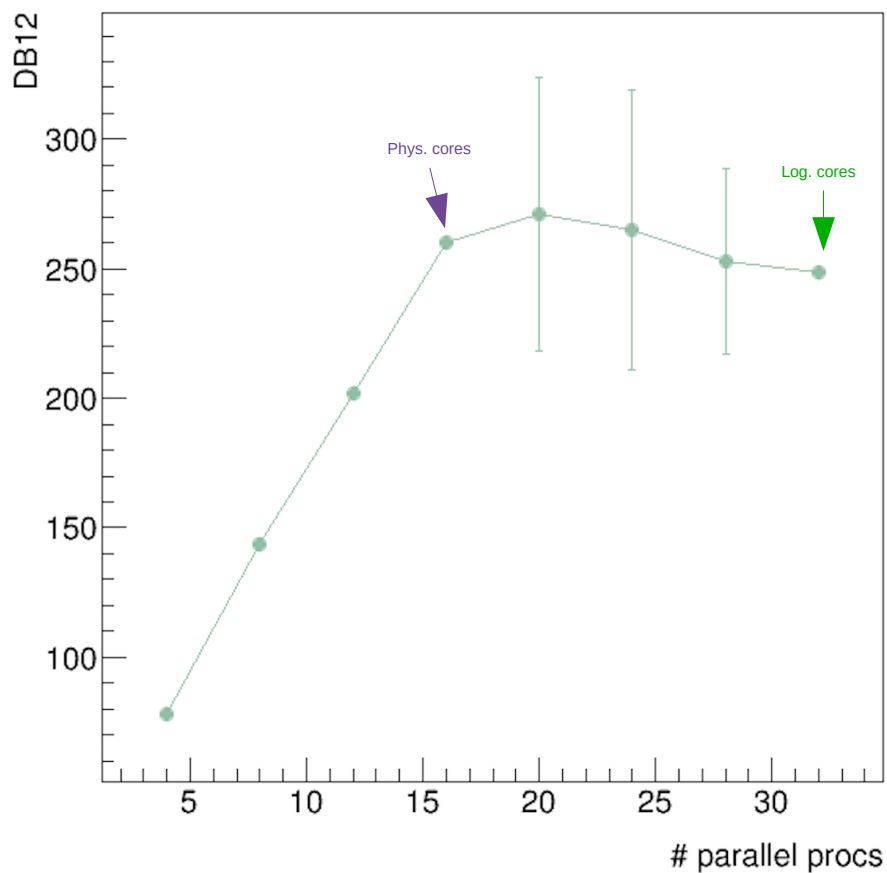
31.5 days CPUtime

DB12 and HS06 tests at PIC

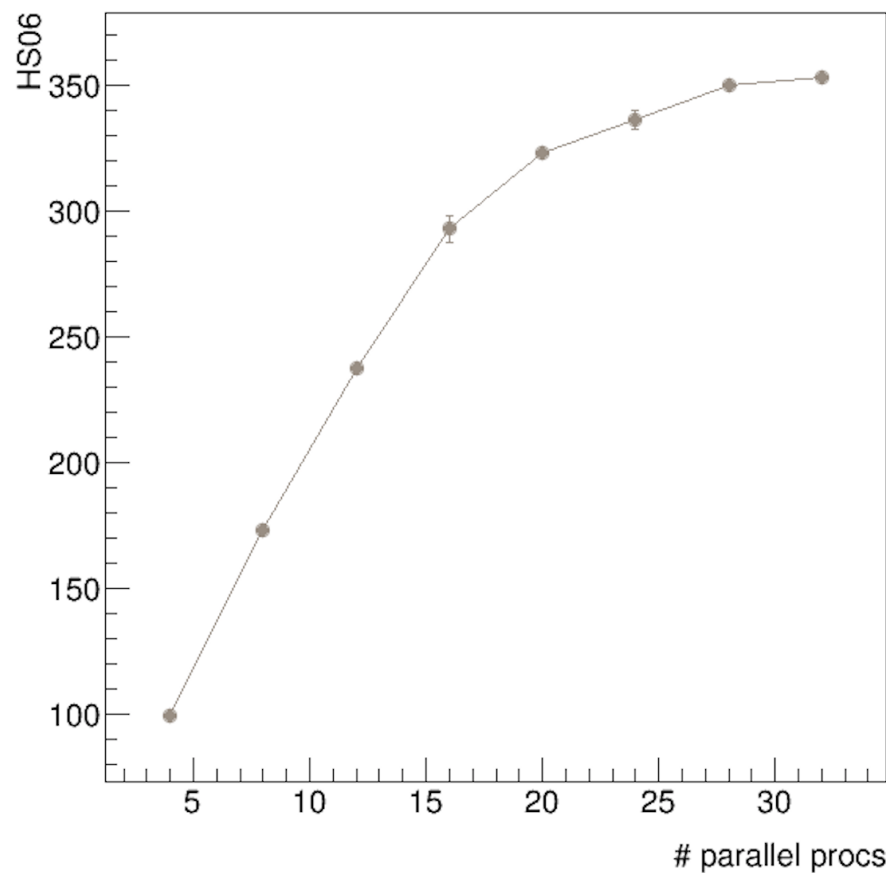
DB12 - Intel Xeon E5-2640v3 @ 2.60GHz

HS06 - Intel Xeon E5-2640v3 @ 2.60GHz

E2640v3-2.60



DB12



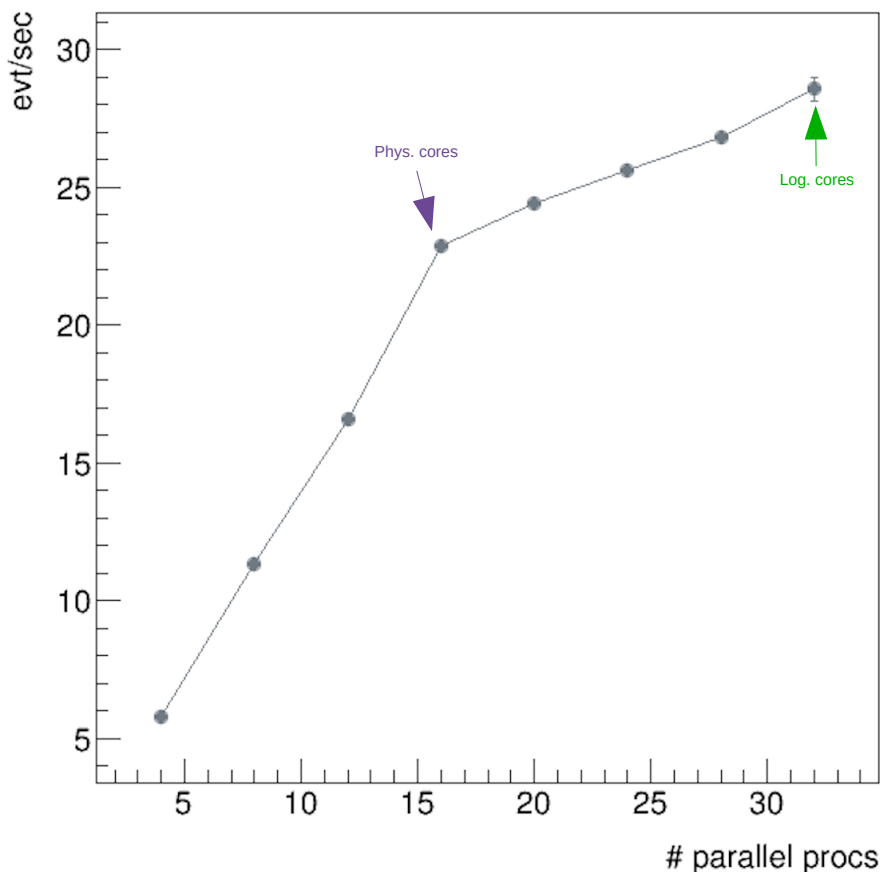
HS06

KV and CMS ttbar tests at PIC

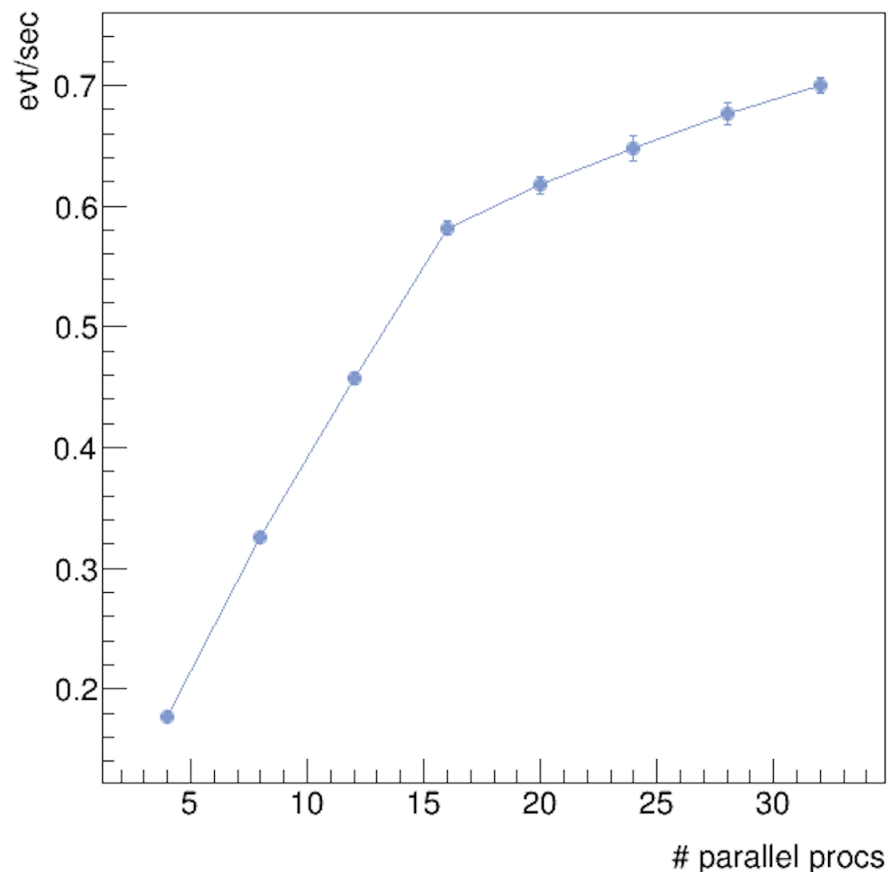
KV - Intel Xeon E5-2640v3 @ 2.60GHz

CMS ttbar sim. - Intel Xeon E5-2640v3 @ 2.60GHz

E2640v3-2.60



KV

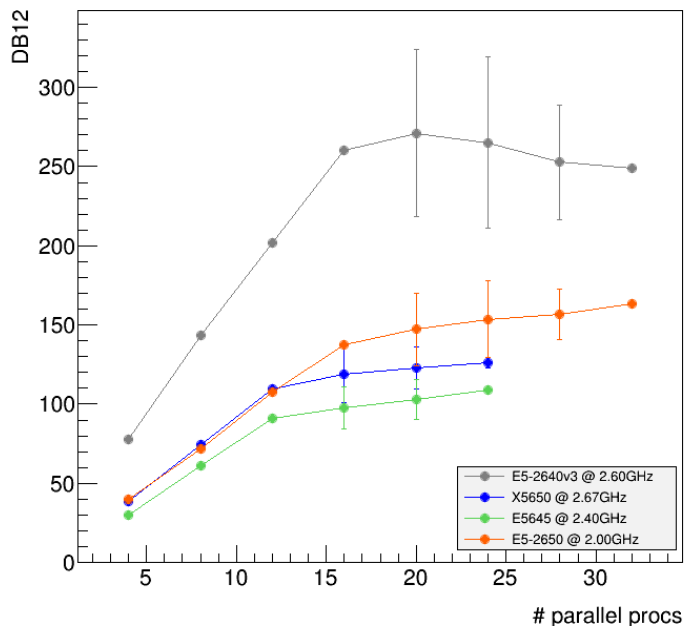


ttbar

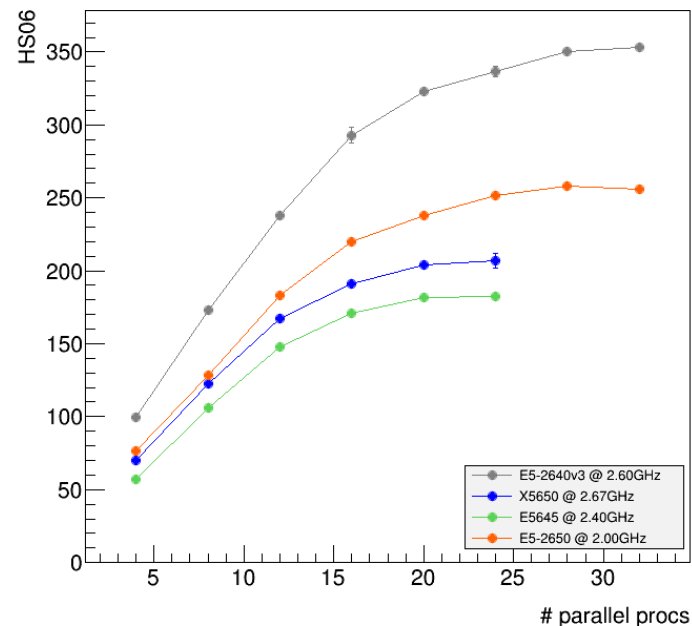
Tests made at PIC so far

SUMMARY

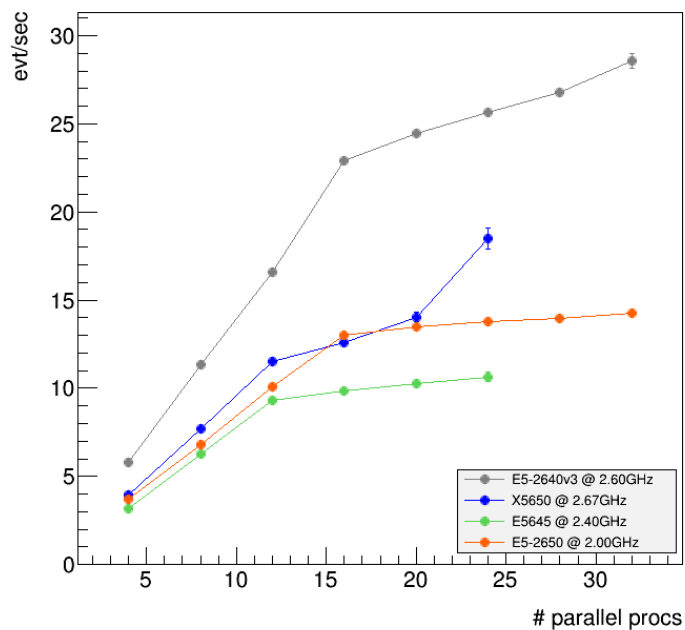
DB12 tests @ PIC Tier-1



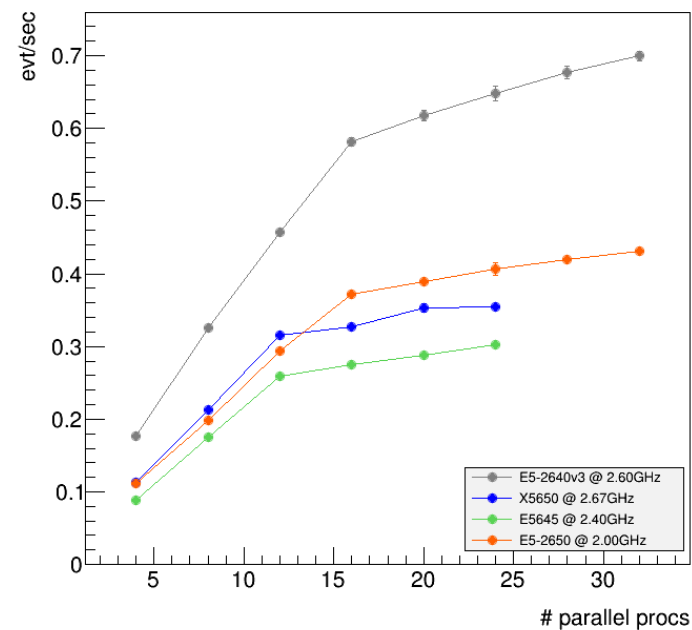
HS06 tests @ PIC Tier-1



KV tests @ PIC Tier-1

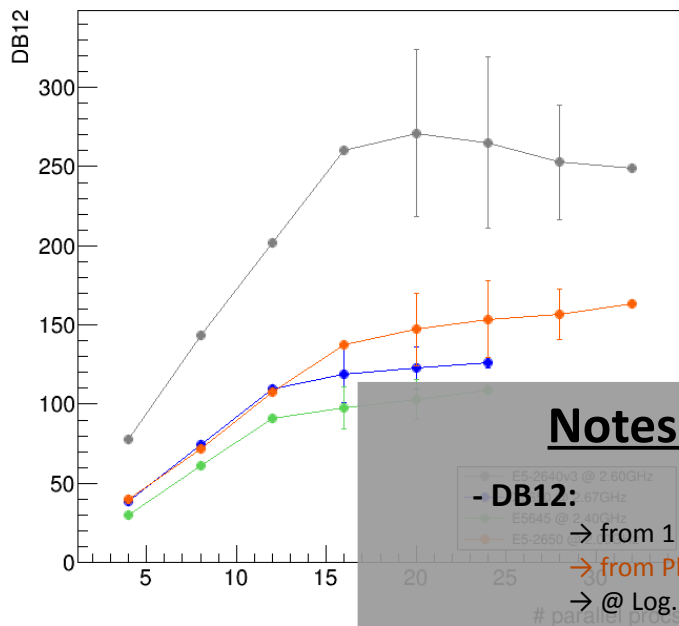


CMS ttbar sim. tests @ PIC Tier-1

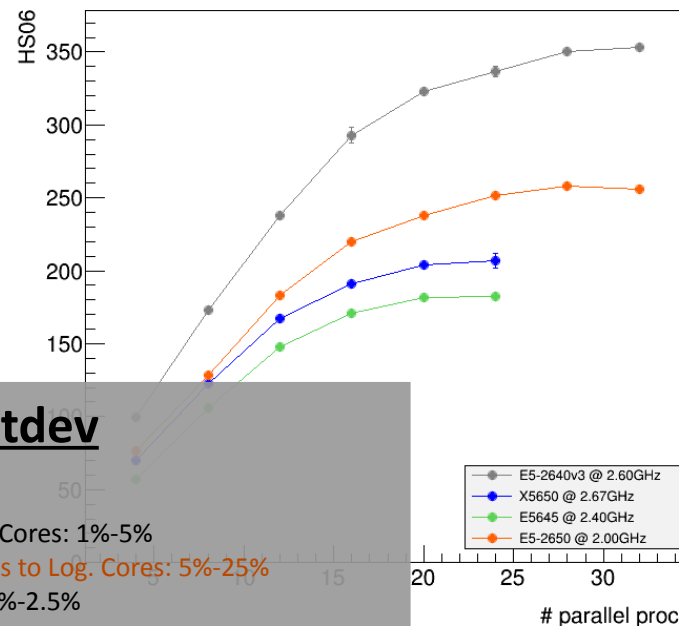


Tests made at PIC so far

DB12 tests @ PIC Tier-1



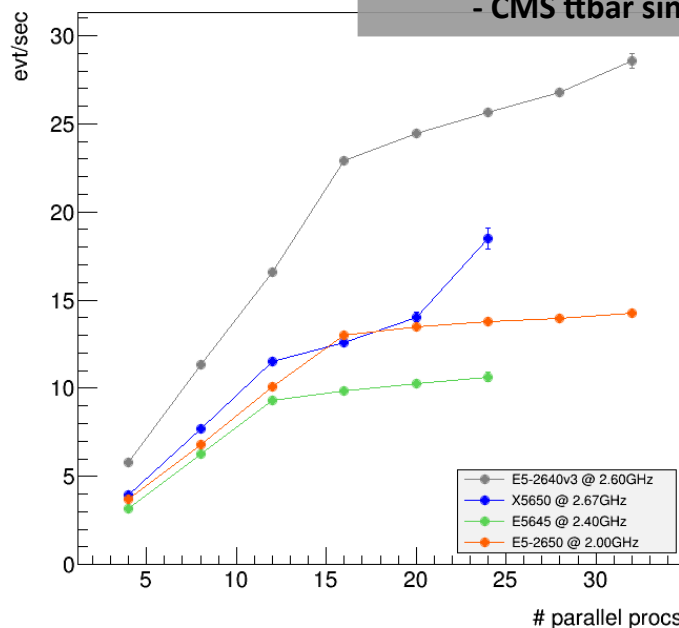
HS06 tests @ PIC Tier-1



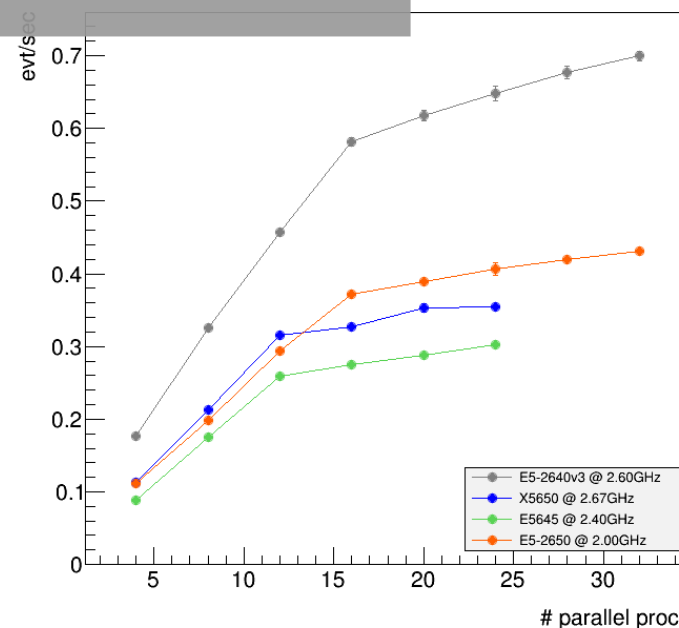
Notes on stdev

- DB12:
 - from 1 to Phys. Cores: 1%-5%
 - from Phys. Cores to Log. Cores: 5%-25%
 - @ Log. Cores: 1%-2.5%
- HS06: <2%
- KV: <3%
- CMS ttbar sim: <2%

KV tests @ PIC Tier-1



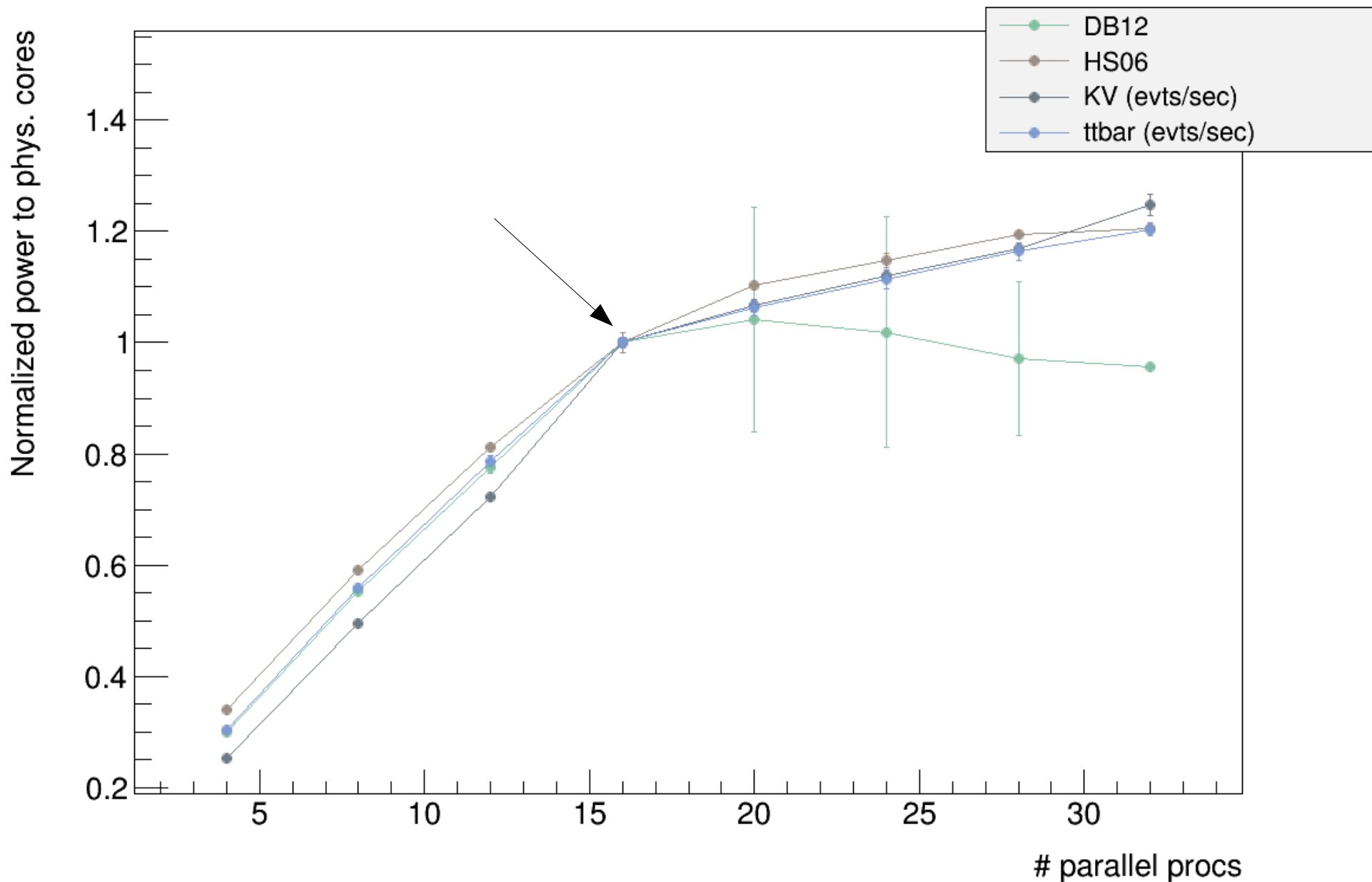
CMS ttbar sim. tests @ PIC Tier-1



SUMMARY

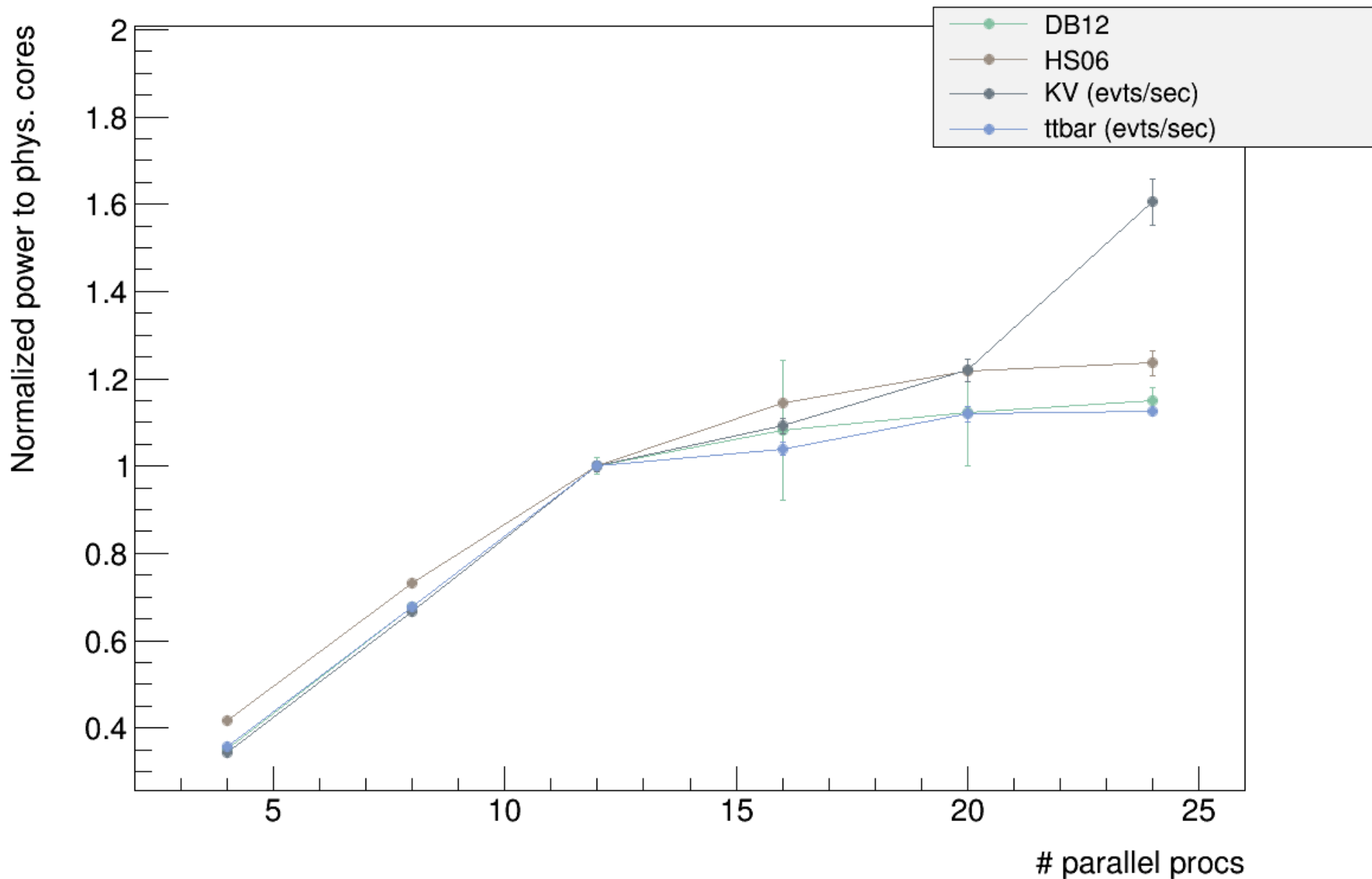
Tests made at PIC so far

CMS ttbar sim. - Intel Xeon E5-2640v3 @ 2.60GHz



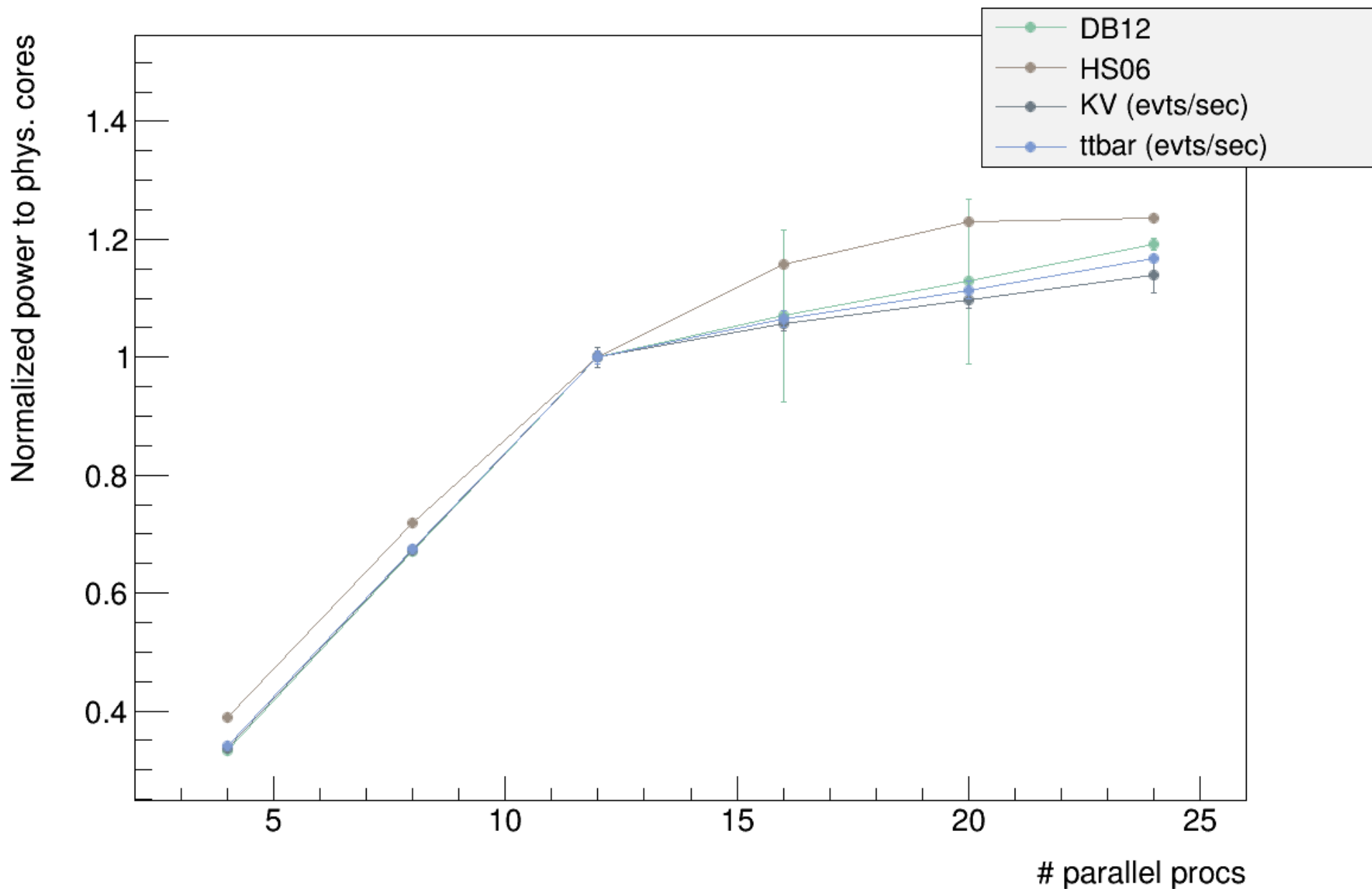
Tests made at PIC so far

CMS ttbar sim. - Intel Xeon X5650 @ 2.67GHz



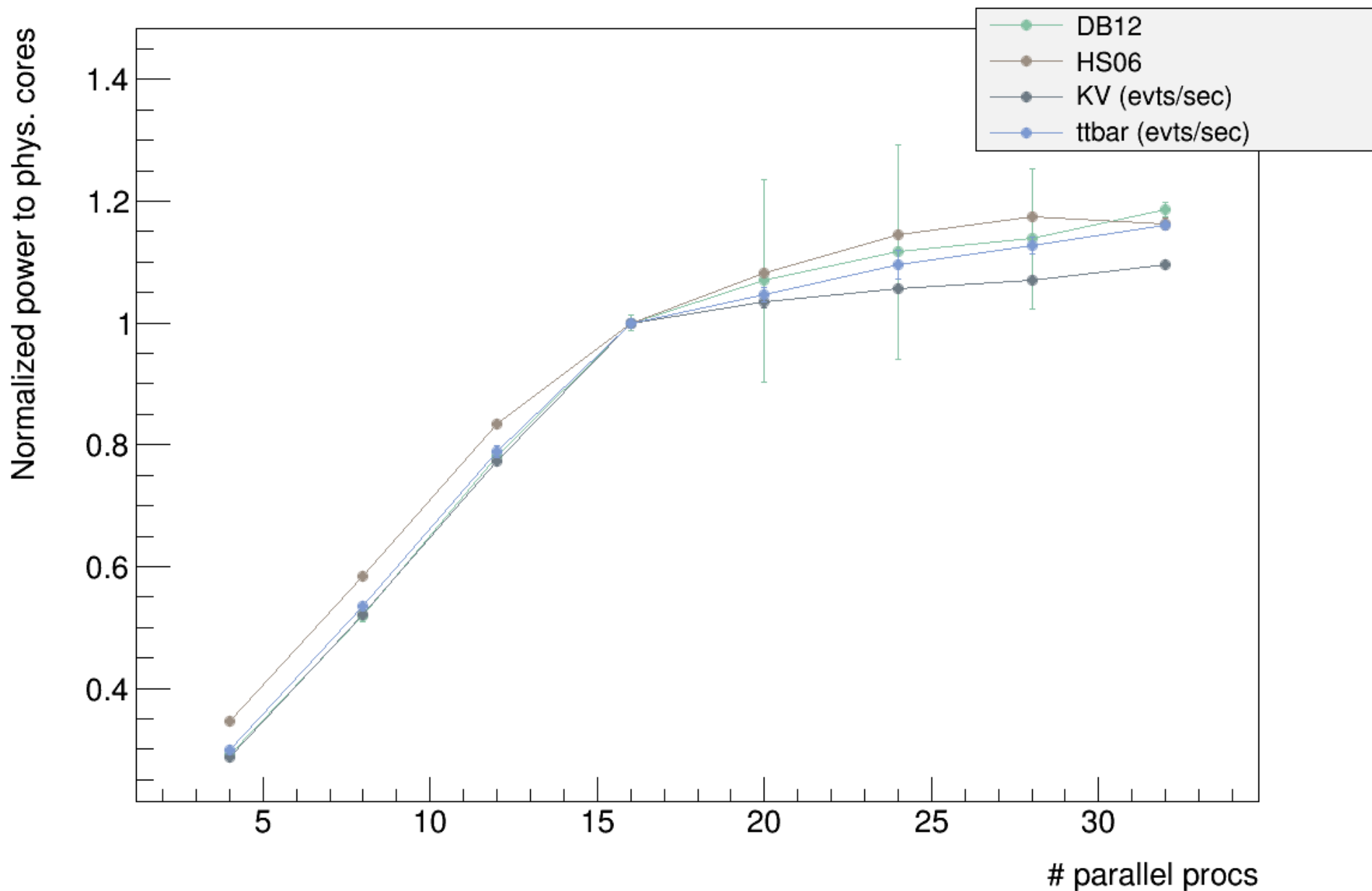
Tests made at PIC so far

CMS ttbar sim. - Intel Xeon Intel Xeon E5645 @ 2.40GHz

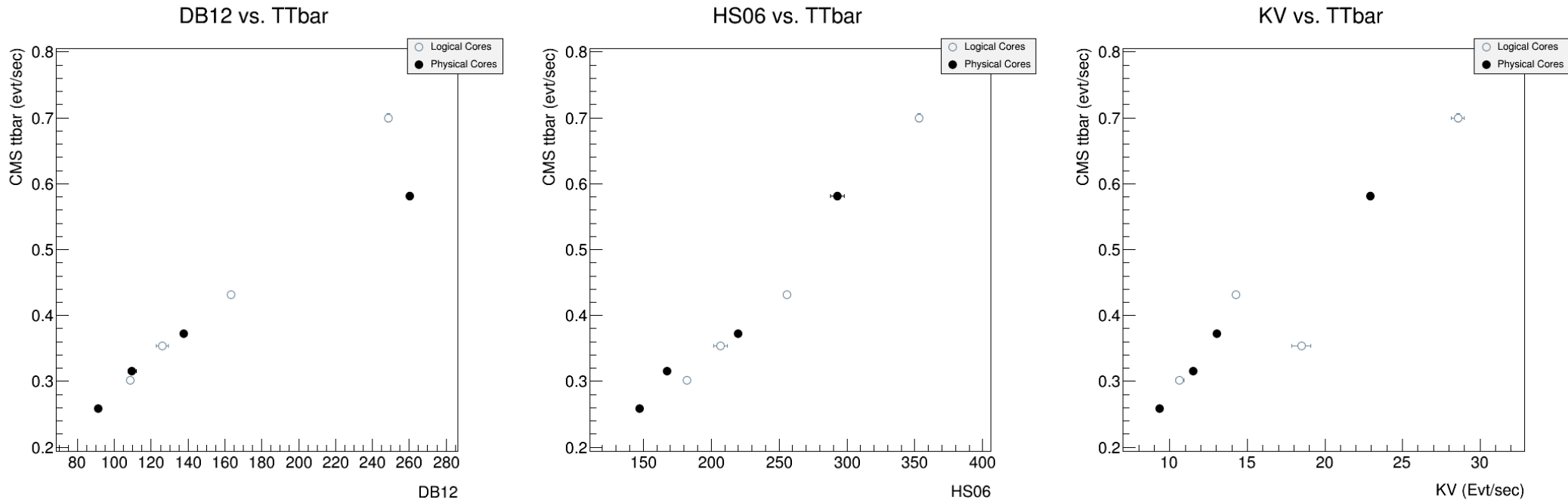


Tests made at PIC so far

CMS ttbar sim. - Intel Xeon E5-2650 @ 2.00GHz



Tests made at PIC so far



- We need to include more architectures to draw conclusions from these studies
- Fits to check linearity?
- All these values have been obtained with sufficient statistics (error bars)
- Shall we run other benchmarks, for completeness?
- Action: add all this info to the twiki

Thanks!