DS345_V2_MPW2

LAYOUT

ORSAY

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LAYOUT

Stack Up :

L1 (Top) : Signals + Gnd

L2 : Gnd

L3 : Signals + PS + Gnd

L4 : PS (VDD, VDDA , P1V7_A, P1V7_D) + Gnd

L5 : PS (VDDA, VREF) + Gnd

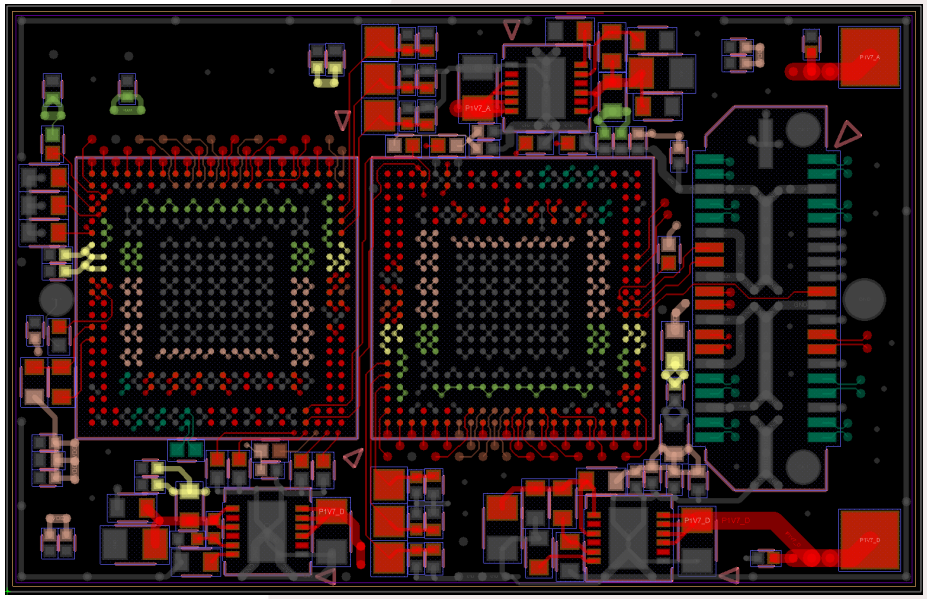
L6 : Signals + Gnd

L7 : Gnd

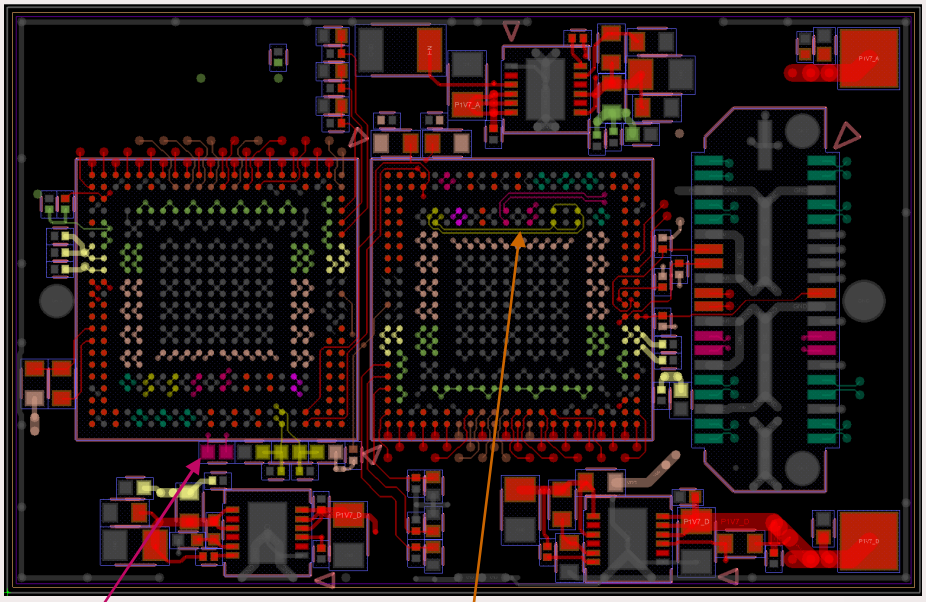
L8 (Bottom) : Signals (all inputs) + Gnd

TOP LAYER (L1)

DS345_v1_MPW2



DS345_v2_MPW2



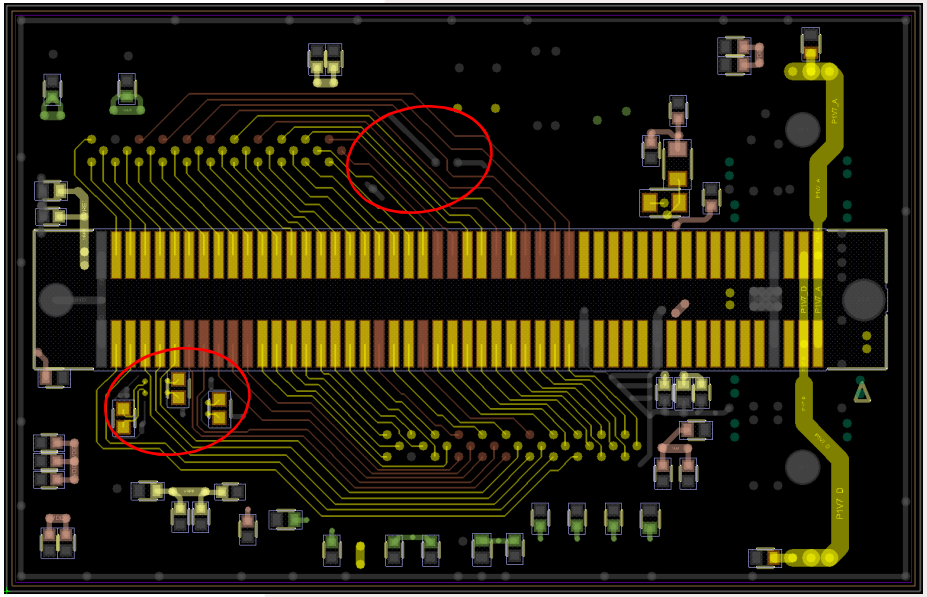
Rter (ClkSoin)

ñClkADCin, ClkBXin, DinN, NBFlowStopinò
6 differentiel pairs ñunused inputsò are present.

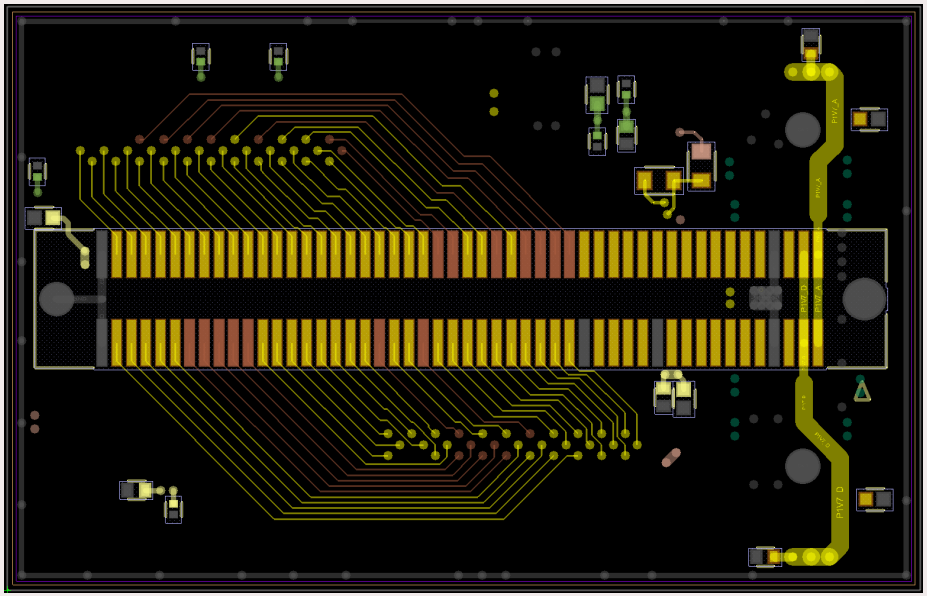
- **Decoupling capacitors to be added.**

BOTTOM LAYER (L8)

DS345_v1_MPW2



DS345_v2_MPW2

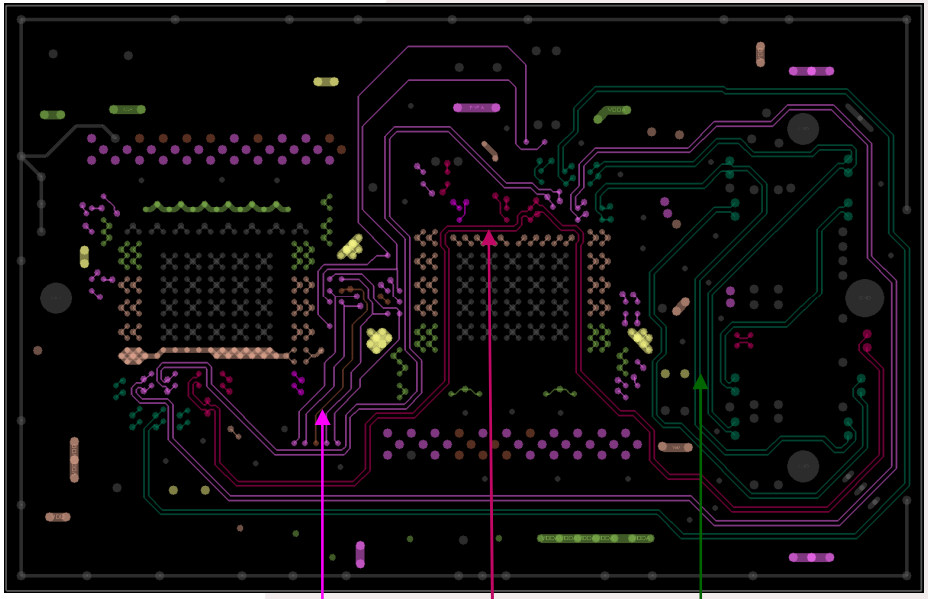


- Input signals (brown colors : noise)
- No termination resistors, no gnd between inputs.

- **Decoupling capacitors to be added.**

SIGNAL LAYER (L3)

DS345_v1_MPW2

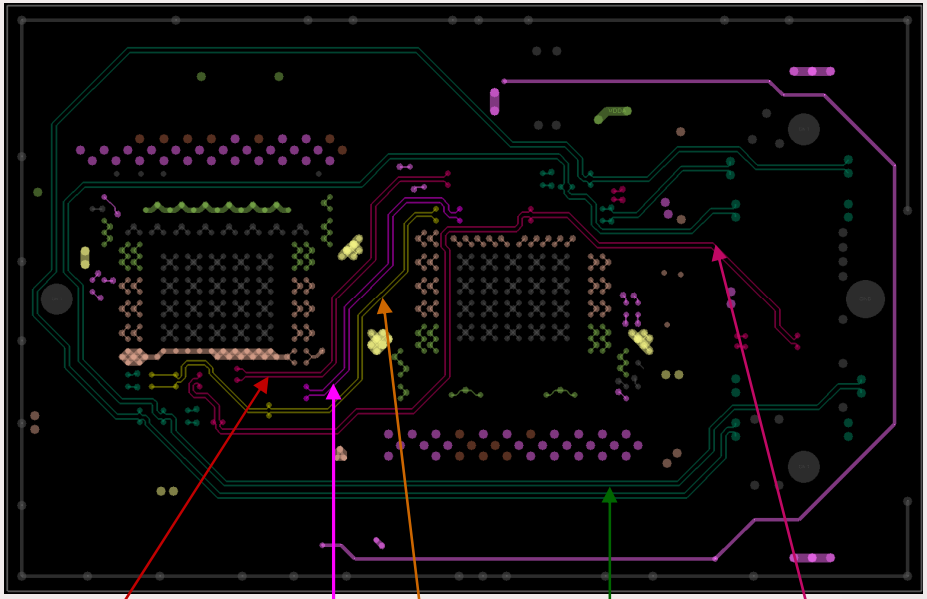


Configuration

ClkSOin

Daisy Chain Signals

DS345_v2_MPW2



SerialOut (between SAMPAs)

NBFlowStop

Daisy Chain Signals (TRG, HB_TRG)

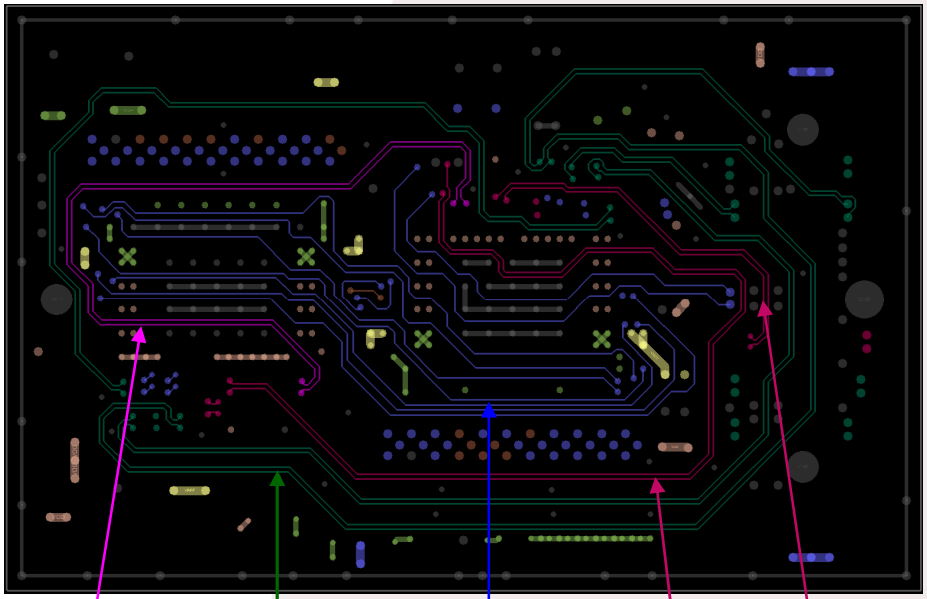
ClkSOin

ñClkADCin, ClkBXin, DinN, NBFlowStopinò 6 differentiel pairs ñunused inputsò are present.

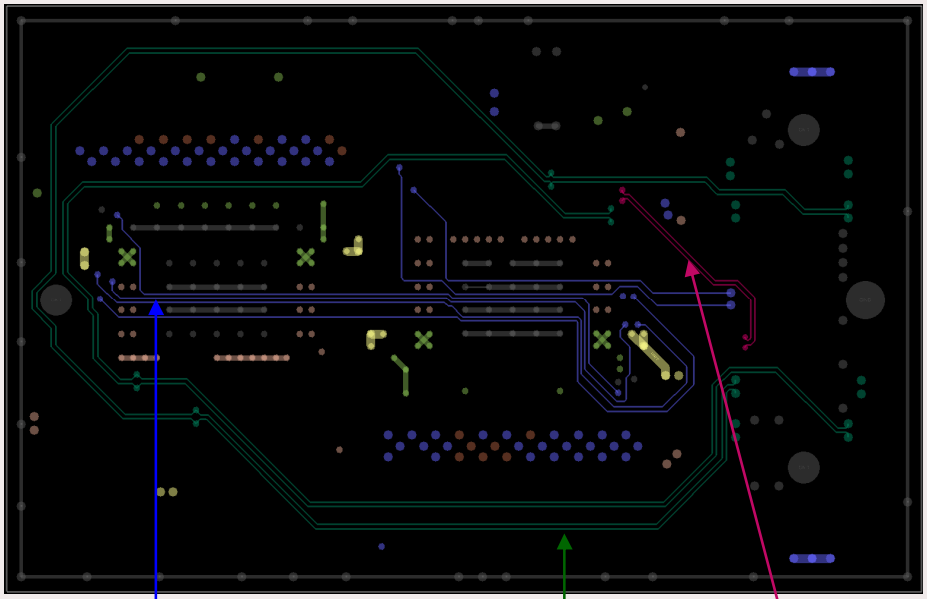
- **SerialOut and NBFlowStop are Present.**

SIGNAL LAYER (L6)

DS345_v1_MPW2



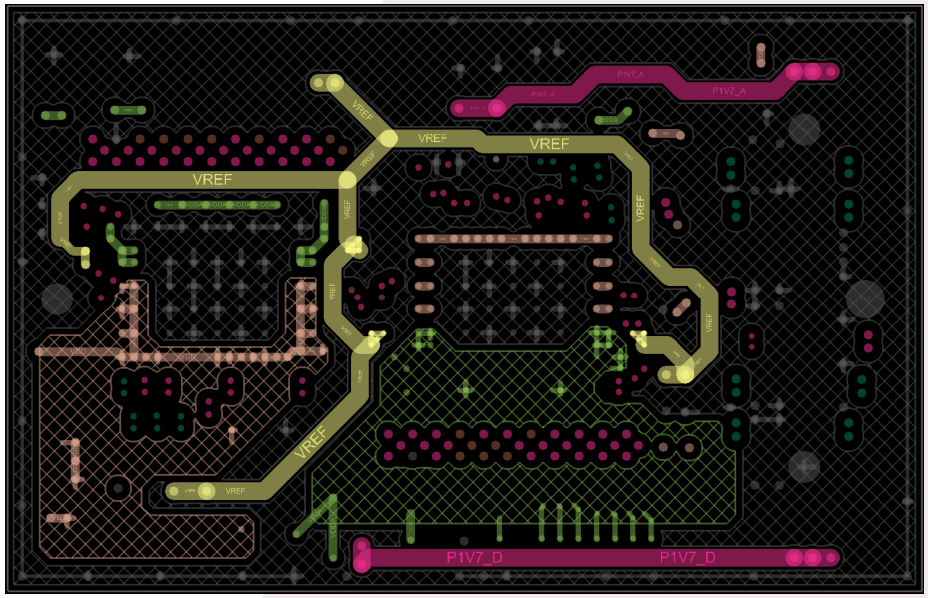
DS345_v2_MPW2



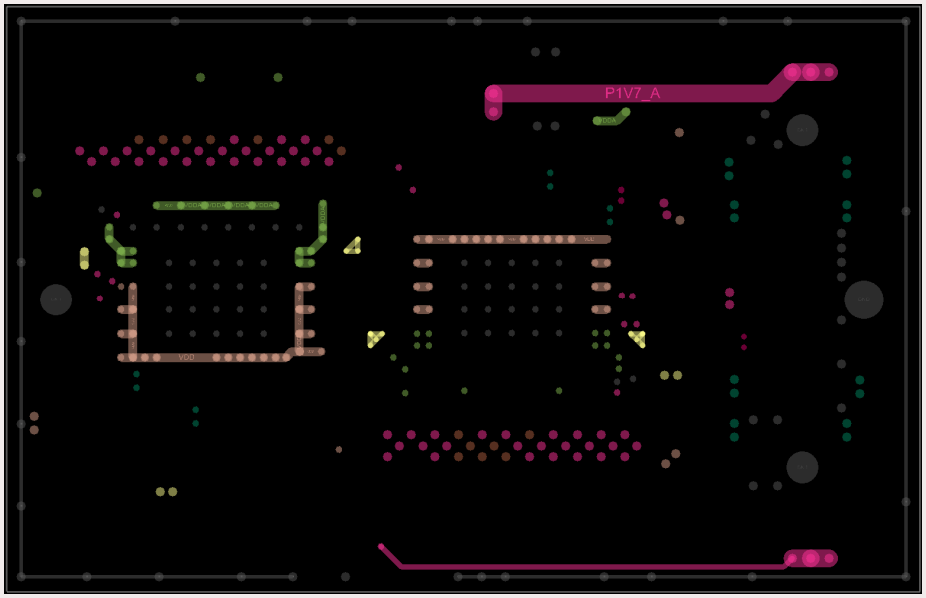
- **SerialOut and NBFlowStop are Present.**

POWER LAYER (L4)

DS345_v1_MPW2



DS345_v2_MPW2



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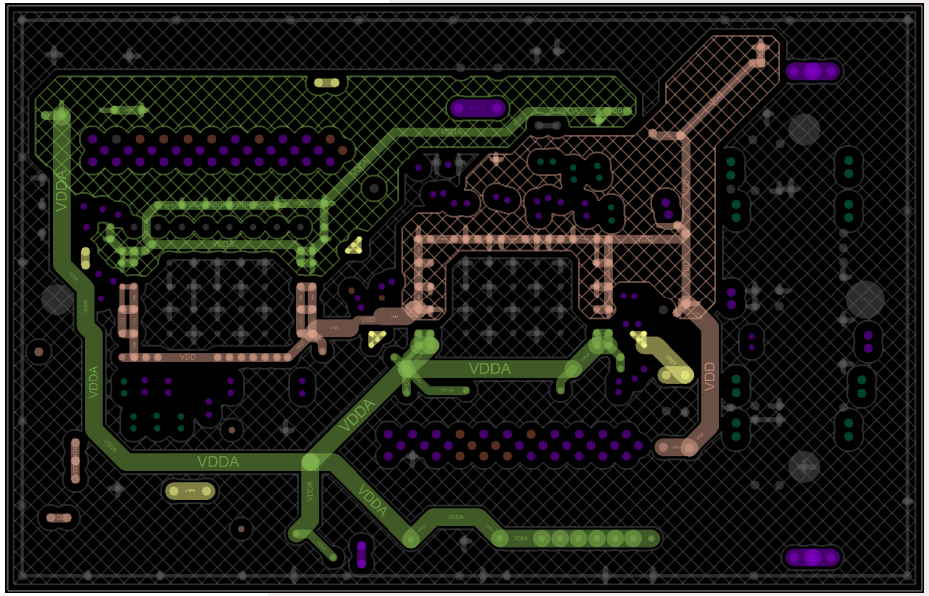
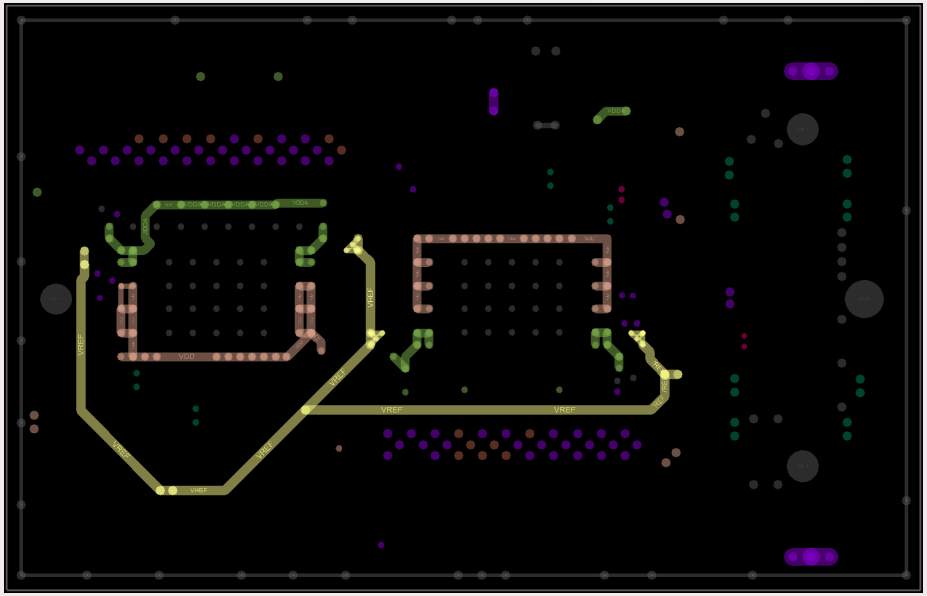
POWER LAYER (L5)

DS345_v1_MPW2



DS345_v2_MPW2



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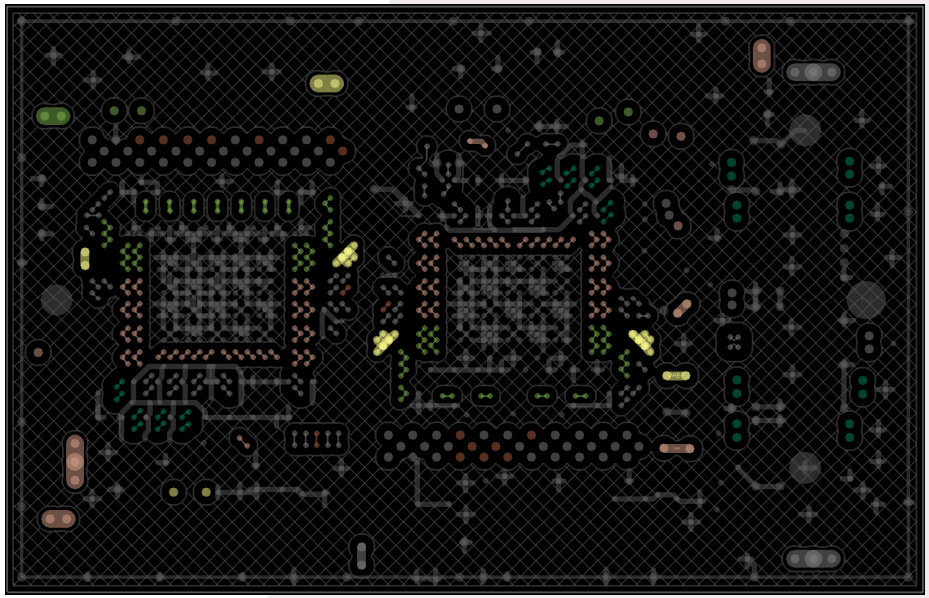
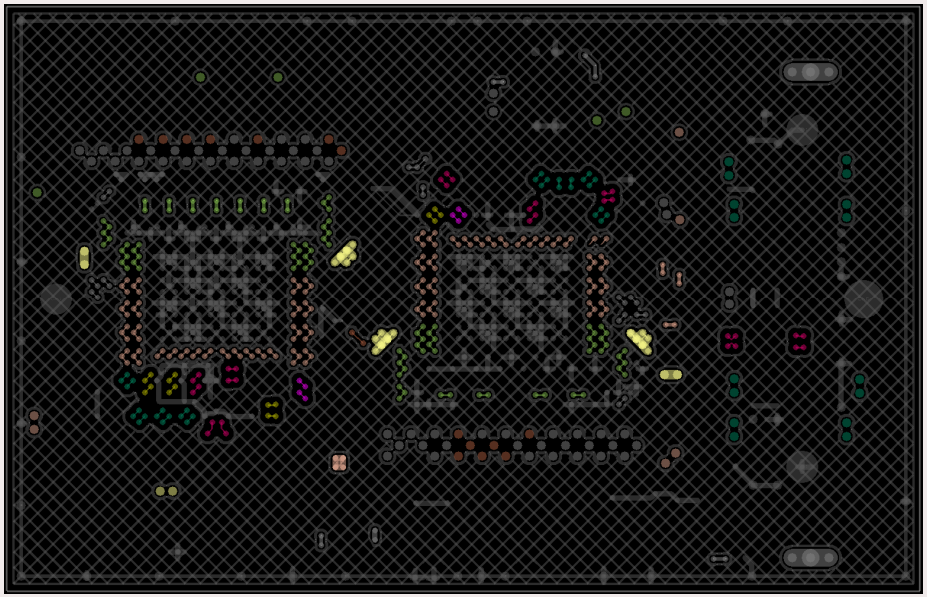
GROUND LAYER (L2)

DS345_v1_MPW2



DS345_v2_MPW2



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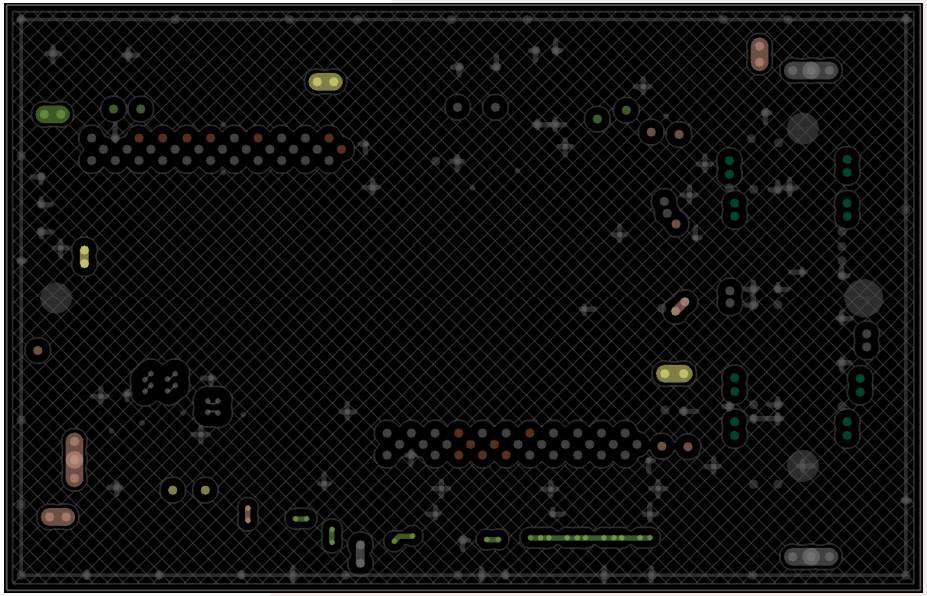
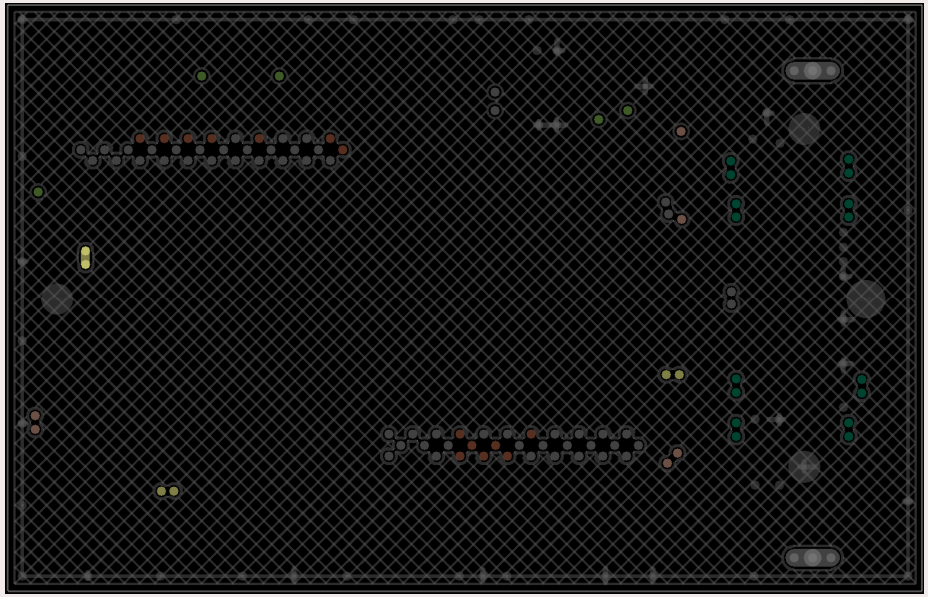
GROUND LAYER (L7)

DS345_v1_MPW2



DS345_v2_MPW2



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CONCULSION

To do

- Placement of decoupling capacitors
- Power Layer
- Repositioning of differentiel pairs due to Crosstalk
- Gnd Layer

Planning

- Layout design : 31st March 2017
- PCB production : 3rd April 2017