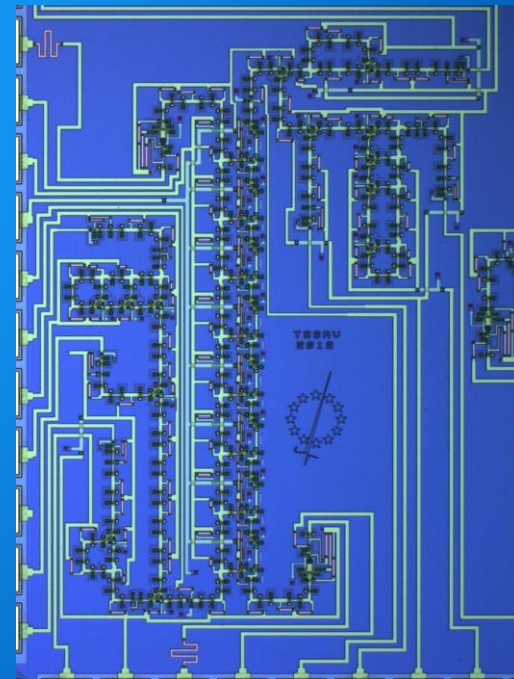
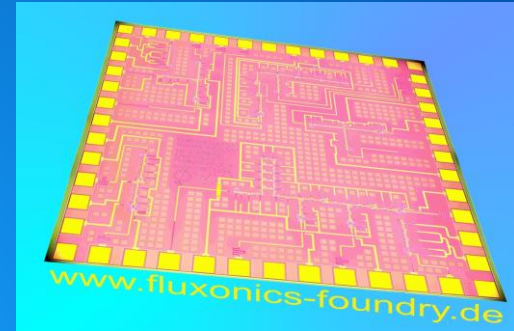


Superconducting electronics

from Josephson effects to quantum computing

by Pascal Febvre and Paul Seidel

Superconducting electronics – Part 5 Digital electronics



Outline

- Basic principles for superconducting electronics
- The Josephson junction
- The SQUID (Superconducting QUantum Interference Device)
- Digital electronics based on Josephson junctions
 1. The superconducting latching logic of the 80's
 2. The Rapid-Single-Flux-Quantum (RSFQ) logic
- Introduction to comparators
- Analog-to-digital conversion with Josephson junctions
 1. hysteretic junctions
 2. non-hysteretic junctions
- The DC-to-SFQ interface as a comparator
- The Quasi-One-Junction SQUID comparator
- The balanced comparator
- Applications of RSFQ logic

Vector potential & electrical potential

Maxwell equations + $\vec{B} = \vec{\nabla} \wedge \vec{A}$ & $\vec{E} = -\frac{\partial \vec{A}}{\partial t} - \vec{\nabla} U$

B & E uniques though the number of couples (A,U) is infinite (depends on the chosen gauge)

Lagrange function $L(r, \dot{r}, t) = \frac{1}{2} m \dot{r}^2 + q \dot{r} A(r, t) - q U(r, t)$

Hamilton function $H(r, p, t) = \frac{1}{2m} [p - q A(r, t)]^2 + q U(r, t)$

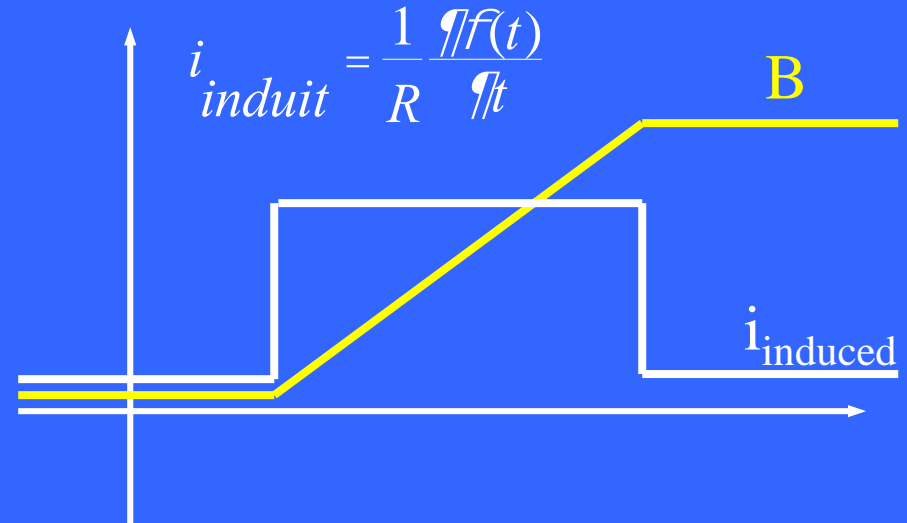
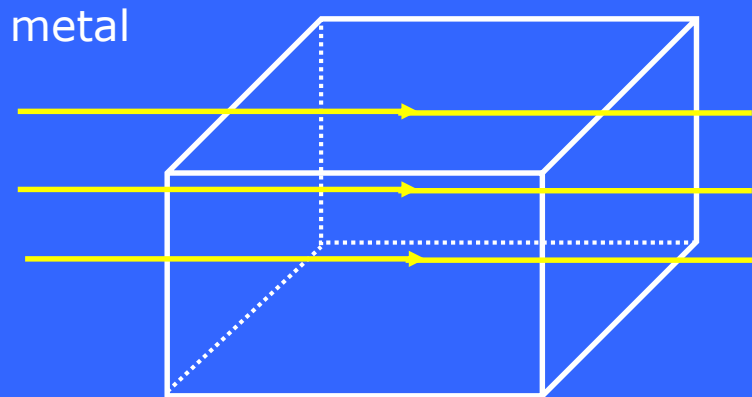
with time-dependent Schrödinger equation, lead to :

$$\vec{J} = \frac{\rho \hbar}{2m_e} \left(\vec{\nabla} \phi - \frac{2\pi}{\Phi_0} \vec{A} \right) \quad \text{where } \Phi_0 = \frac{h}{2e} \text{ is the quantum of magnetic flux}$$

Relation between magnetic flux & phase (1/2)

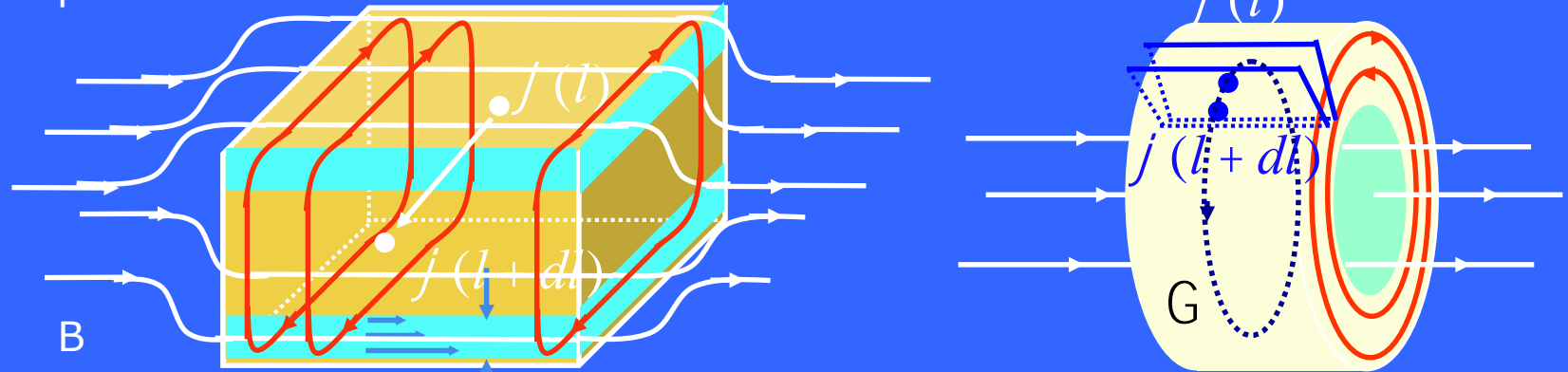
Case of normal metals:

Faraday's law:



Relation between magnetic flux & phase (2/2)

superconductor



**Meissner currents
(diamagnetism)**

l_L : London penetration depth

$$\vec{J} = \frac{\rho \hbar}{2 m_e} \left(\vec{\nabla} \varphi - \frac{2\pi}{\Phi_0} \vec{A} \right) = \vec{0} \text{ on } \Gamma \quad \longrightarrow \quad \oint_{\Gamma} \vec{\nabla} \varphi \cdot d\vec{l} = 2n\pi = \frac{2\pi}{\Phi_0} \Phi_{loop}$$

$$\Phi_{loop} = n \Phi_0$$

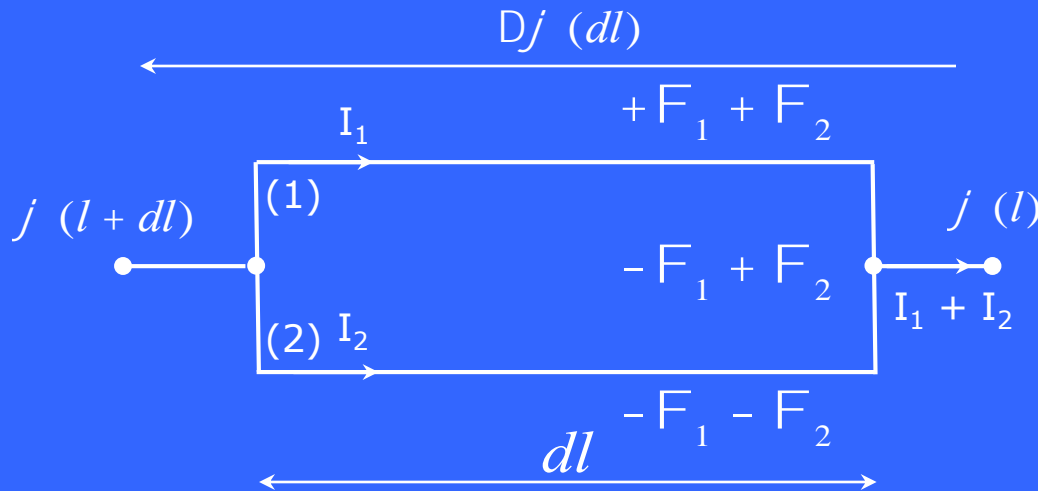
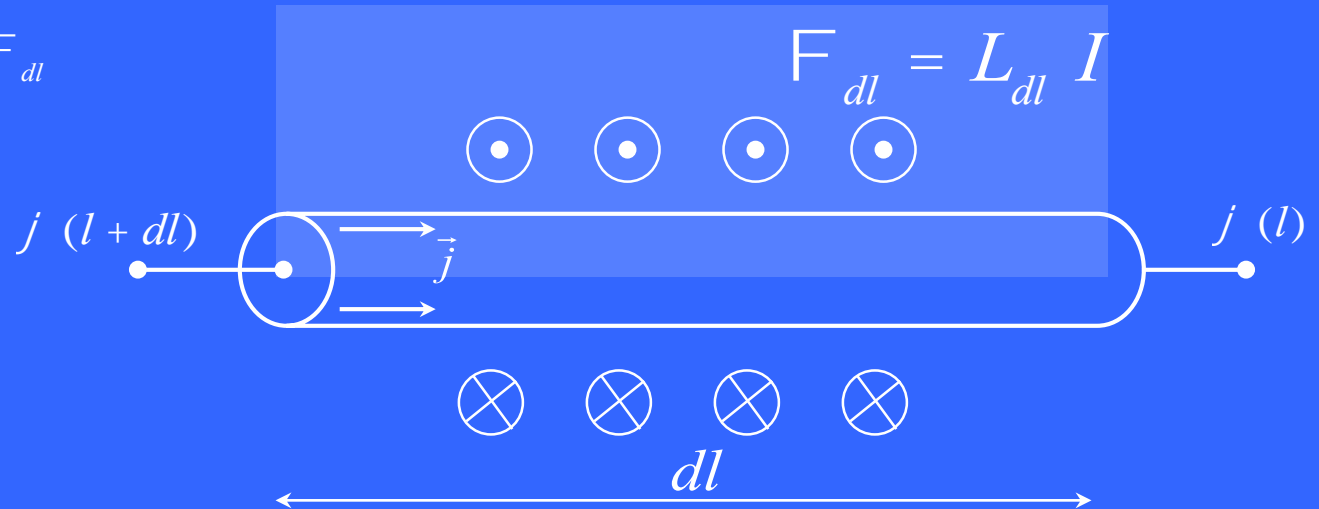
Flux quantization

$$j(l+dl) - j(l) = \frac{2\rho}{F_0} F_{length dl}$$

Phase - flux relation
Aharonov-Bohm effect

Phases, flux and inductances

$$j(l+dl) - j(l) = \frac{2\rho}{F_0} F_{dl}$$



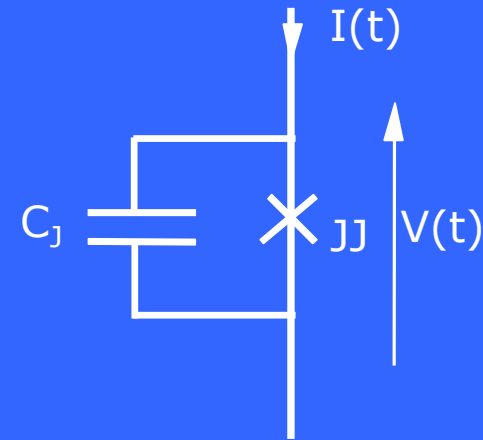
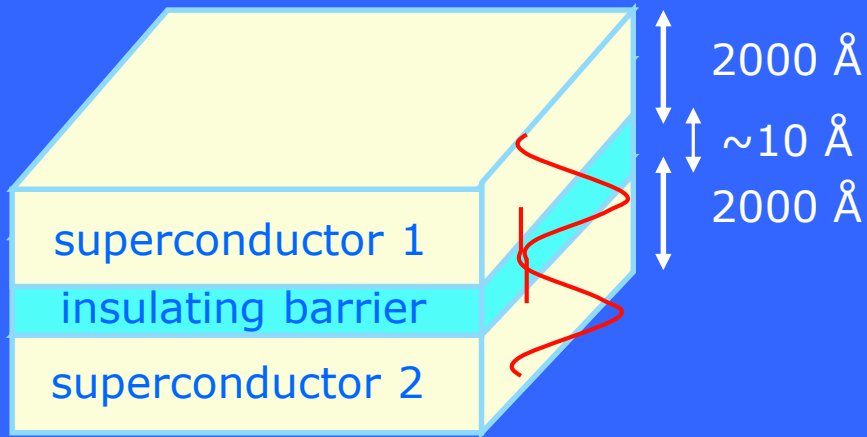
$$-F_1 + F_2 = 2n\rho$$

$$\rightarrow L_1 I_1 = L_2 I_2$$

if no flux in the loop ; same current distribution as with

$$R_1 I_1 = R_2 I_2$$

The Josephson junction



$y_i = y_{i_0} e^{ij_i(t)}$ $j = j_1 - j_2$: phase difference between the two wavefunctions

Josephson equations:

$$I_J = I_c \sin j(t)$$

$$\frac{\hbar j(t)}{\hbar t} = \frac{2\rho}{F_0} V(t)$$

DC Josephson effect at $V = 0$:

$$I_{J0} = I_c \sin j_0$$

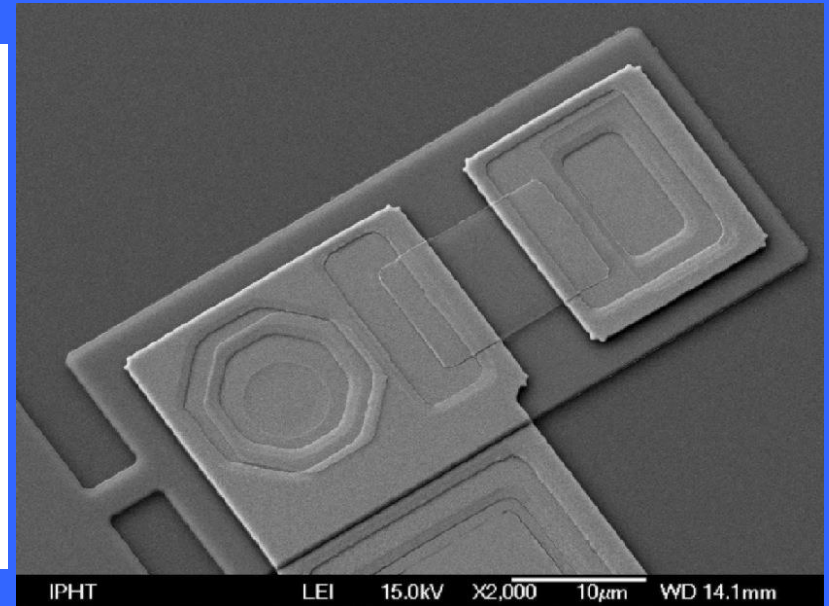
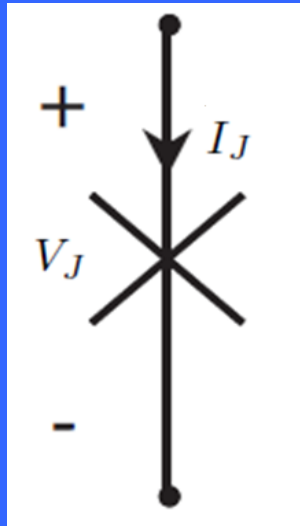
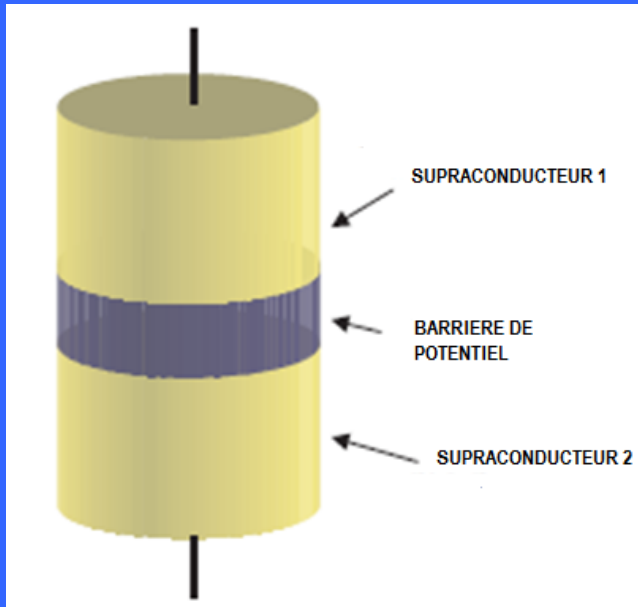
ac Josephson effect at $V_0 = \text{cste}$:

$$I_J = I_c \sin \left(\frac{2\rho}{F_0} V_0 t \right) = I_c \sin (2\rho f_J t)$$

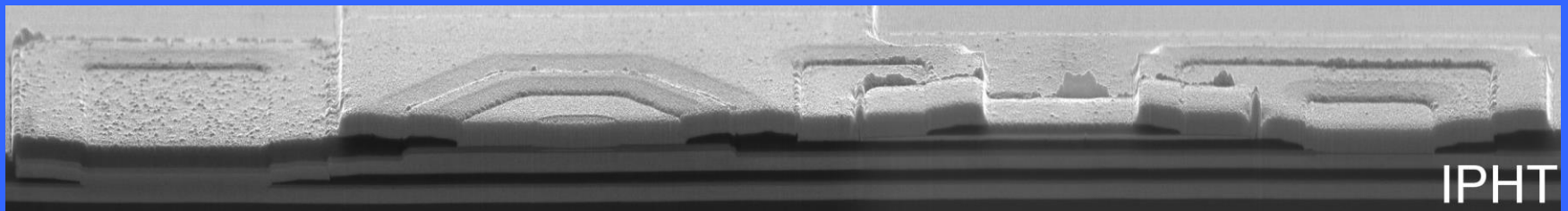
with $f_J = 484 \text{ GHz/mV}$ (Josephson relation)

The Josephson junction

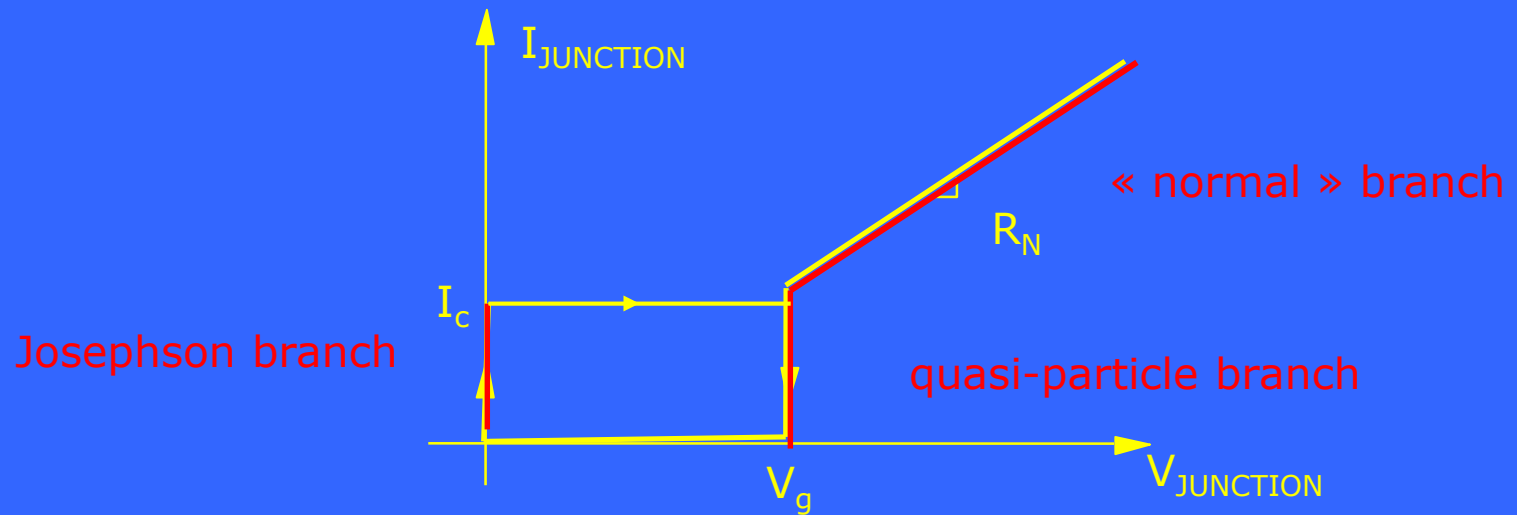
Josephson junction: equivalent to the transistor for semiconductor electronics



Materials commonly used: Nb/Al-AlO_x/Nb @4.2 K



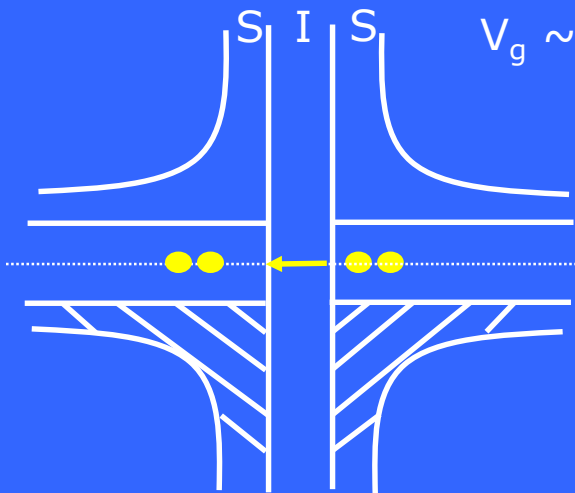
I-V characteristic of a Josephson junction



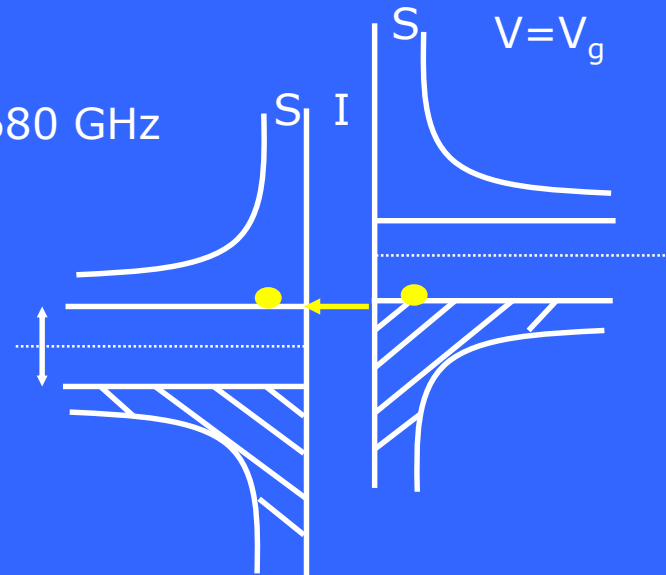
$V=0$

for niobium:

$V_g \sim 2.85$ mV and $f_g \sim 680$ GHz



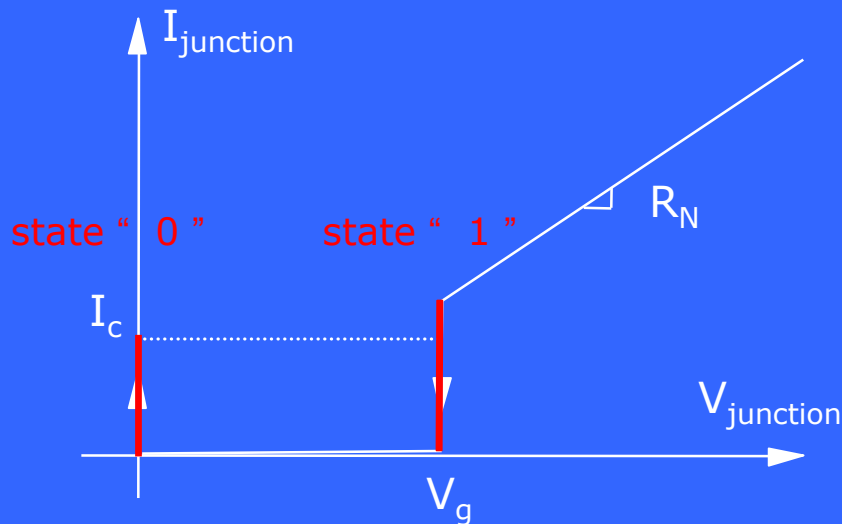
$$eV_g = 2D$$



The superconducting latching logic of the 80's

Absence of resistance of superconductors combined with characteristic frequencies of a few hundreds GHz →

- development of a static logic in the eighties (IBM ; MITI)
- based on hysteretic Josephson junctions



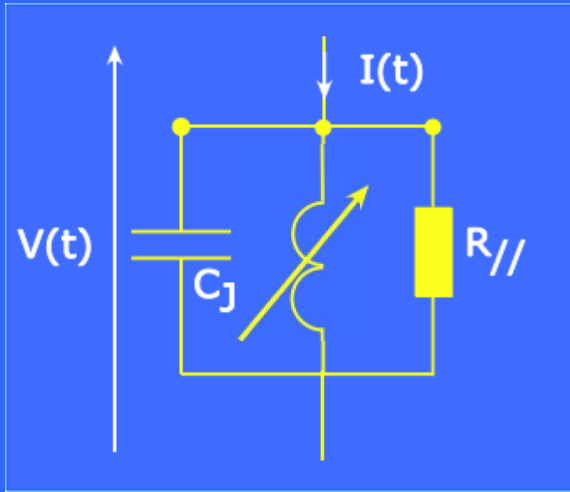
Outcome:

- clock frequencies of a few GHz limited by the punch-through effect
- with the drawback of cryogenic cooling
- period of intense research & development still used today

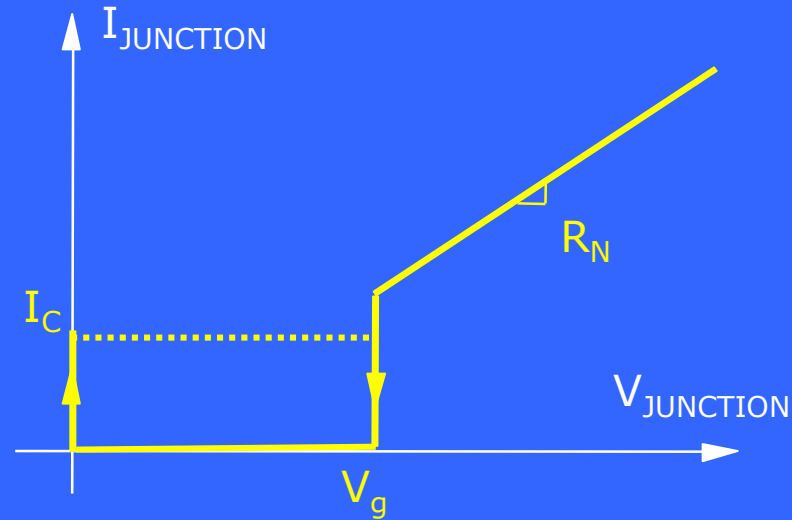
End of the eighties: Konstantin K. Likharev & his team (Moscow State University) proposed a superconducting logic based on quanta of magnetic flux :

a dynamic logic which relies on the use of shunted Josephson junctions

Josephson junction electrodynamics



$$I(t) = I_C(t) + I_J(t) + I_R(t)$$



$$I_J(t) = I_c \sin j(t)$$

$$I_C(t) = C_J \frac{\partial V(t)}{\partial t}$$

$$I_R(t) = \frac{V(t)}{R_{//}}$$

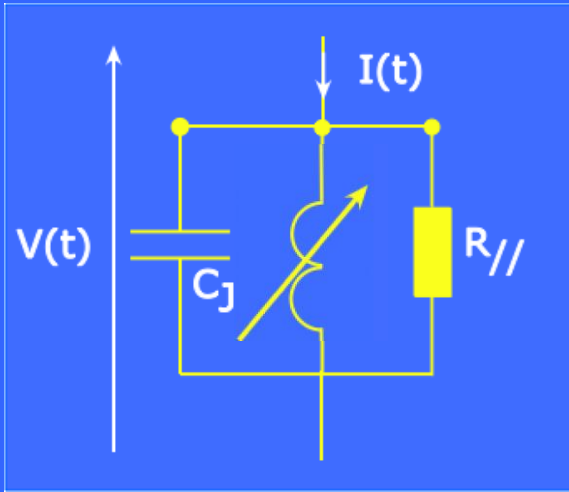
2nd Josephson equation (Faraday's law): $V(t) = \frac{F_0}{2\rho} \frac{\partial j(t)}{\partial t}$

$$\longrightarrow V(t) = \frac{F_0}{2\rho} \left[\frac{1}{I_c \cos j(t)} \frac{\partial I_J(t)}{\partial t} \right] = L_J \frac{\partial I_J(t)}{\partial t}$$

$$L_J = \frac{L_{J_0}}{\cos j(t)} \quad \text{with} \quad L_{J_0} = \frac{F_0}{2\rho I_c} \quad \text{Josephson inductance}$$

\longrightarrow JJ = non-linear parallel RLC circuit

Characteristic time constants & frequencies



$$\frac{I(t)}{I_c} = L_{J_0} C_J \frac{\sin^2 j(t)}{\hbar^2 t^2} + \frac{L_{J_0}}{R_{//}} \frac{\sin j(t)}{\hbar t} + \sin j(t)$$

Anharmonic oscillator

Electrical approach

Physical approach
(BCS theory)

Plasma period
of the L-C circuit :

$$t_p = 2\rho\sqrt{L_{J_0}C_J}$$

$$t_p = \sqrt{\frac{2\rho F_0 C_s}{j_c}}$$

L-R circuit time constant :

$$t_c = \frac{L_{J_0}}{R_{//}}$$

$$t_c = \frac{2F_0}{\rho^2 V_g}$$

Nb: 0.15 ps
NbN: 0.07 ps

R-C circuit time constant :

$$t_{RC} = R_{//} C_J$$

$$t_{RC} = \frac{\rho V_g C_s}{4 j_c}$$

Linearized approach

$$\text{If } j(t) \ll 1 \quad \frac{I(t)}{I_c} = L_{J_0} C_J \frac{\ddot{j}(t)}{t^2} + \frac{L_{J_0}}{R_{//}} \frac{\dot{j}(t)}{t} + j(t)$$

Damping coefficient: $\chi = \frac{1}{2R_{//}} \sqrt{\frac{L_{J_0}}{C_J}}$

Quality factor: $Q = \frac{1}{2\chi} = R_{//} \sqrt{\frac{C_J}{L_{J_0}}}$

For damped oscillatory regimes, transients evolve as: $e^{-\frac{t}{2R_{//}C_J}} = e^{-\frac{t}{2t_{RC}}}$

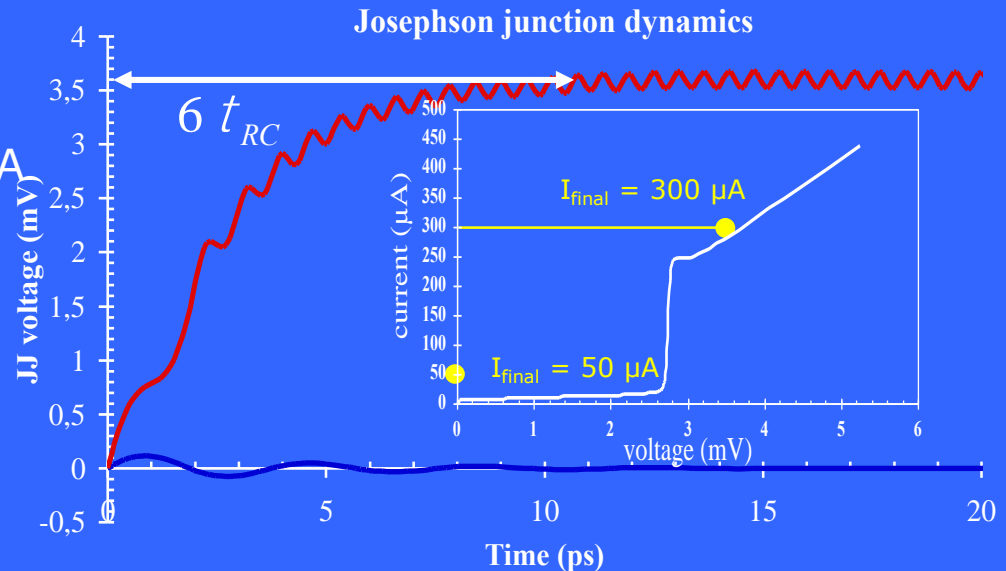
Example:
SIS junction used in radio-astronomy:
 $R_N = 12 \text{ } \Omega$; $C_J = 190 \text{ fF}$; $I_c = 200 \text{ } \mu\text{A}$

$$t_{LR} = 0.13 \text{ ps}$$

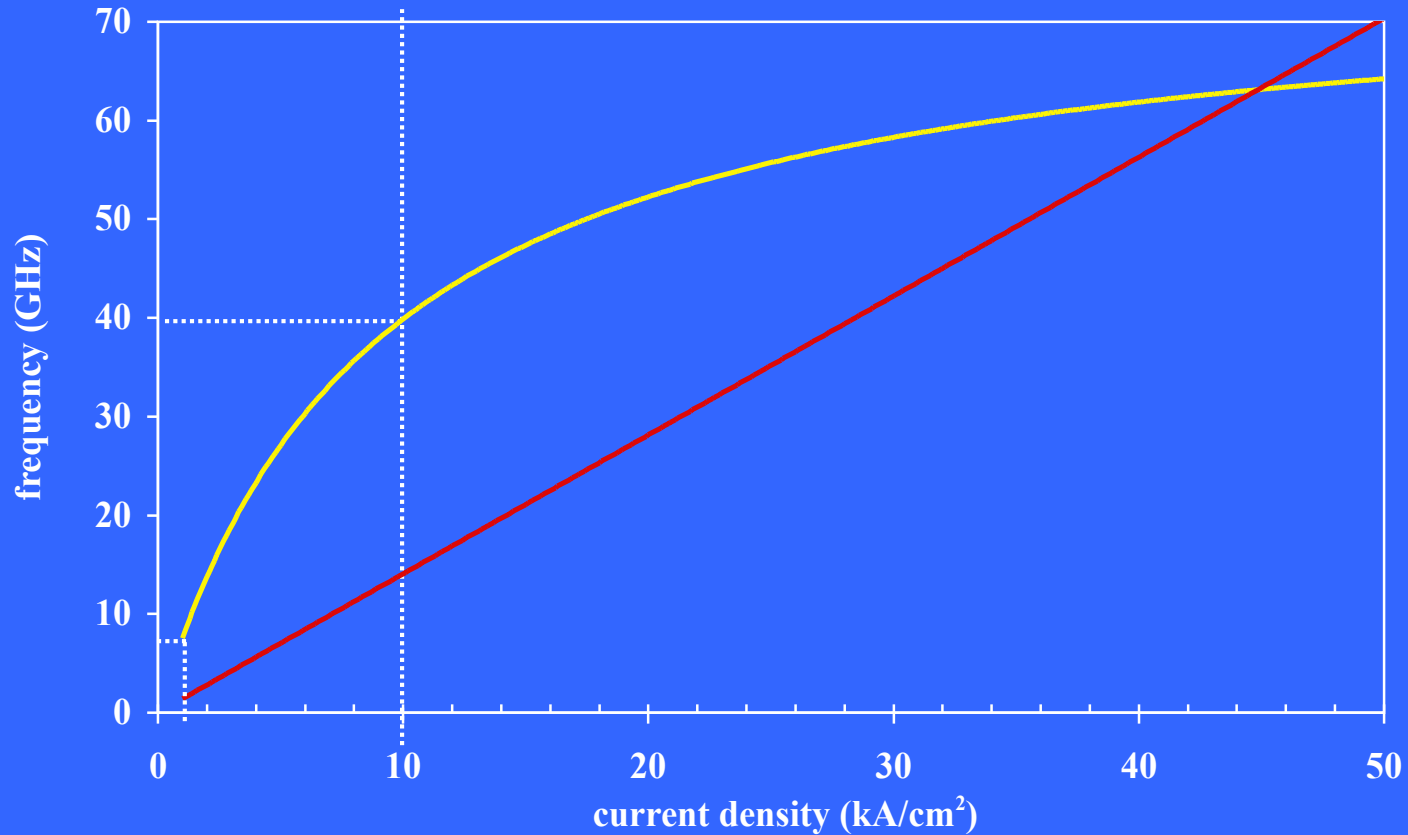
$$t_p = 3.5 \text{ ps}$$

$$t_{RC} = 2.3 \text{ ps}$$

Criteria : $f_{\max} = \frac{1}{12 t_{RC}}$



Limitations of the static logic



Reduce the switching time



Reduce the R-C time constant



Reduce R

Minimising the switching time

$$t_p = 2\rho\sqrt{L_{J0}C_J} \quad t_{LR} = \frac{L_{J0}}{R_{//}} \quad t_{RC} = R_{//}C_J$$

L-C circuit plasma period

L-R circuit time constant

R-C circuit time constant

McCumber parameter defined by:

$$b_c = \frac{t_{RC}}{t_{LR}} = \frac{R_{//}^2 C_J}{L_{J0}} = \frac{2\rho R_{//}^2 C_J I_c}{F_0}$$

Minimum switching time obtained for :

$$t_{RC} = t_{LR} \left(= \frac{t_p}{2\rho} \right) : b_c = 1$$

New time constant

$$t_0 = \sqrt{\frac{F_0 C_s}{2\rho j_c}} = \frac{F_0}{2\rho R_{shunt} I_c}$$

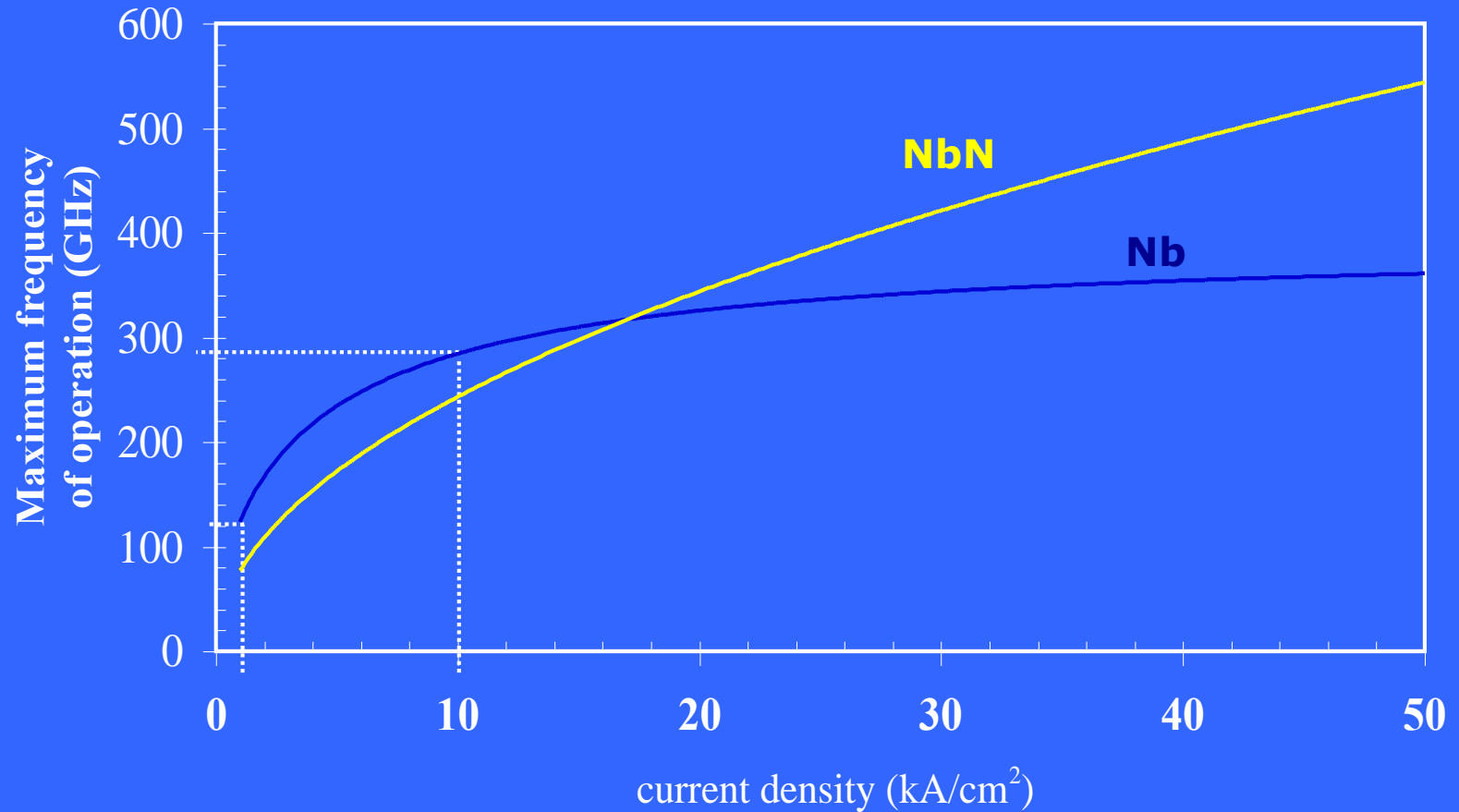
$$t_0 (ps) \gg \frac{1}{\rho V_c (mV)} \text{ with } V_c = R_{shunt} I_c$$

$$R_{//} \gg R_{shunt}$$

Criteria: $f_{\max} = 1/(2\pi\tau_0)$

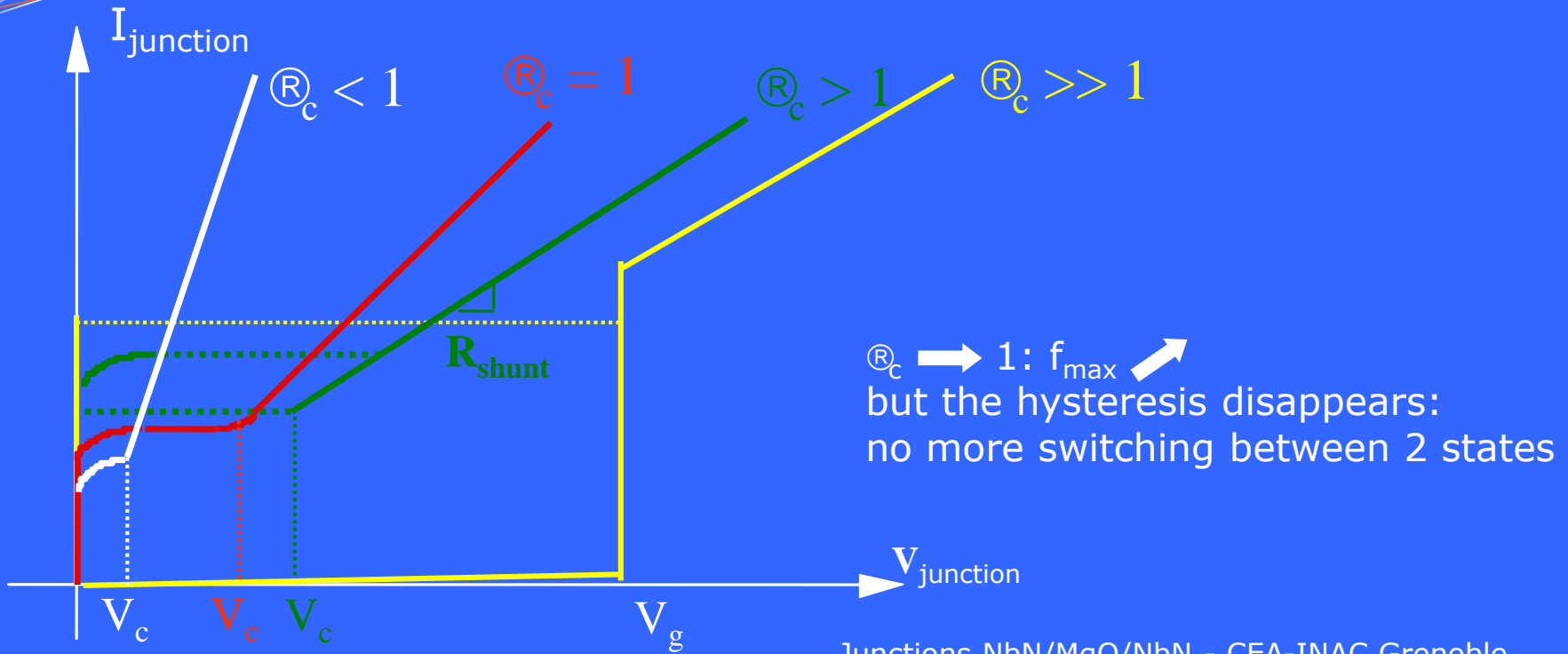
$$f_{\max}(\text{GHz}) = 500 \times V_c(\text{mV})$$

Maximum frequency of operation

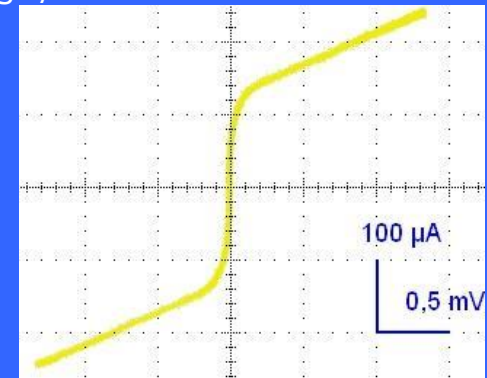
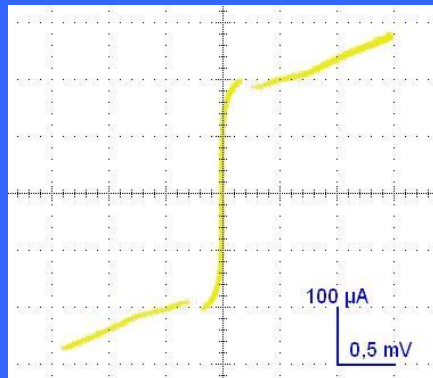
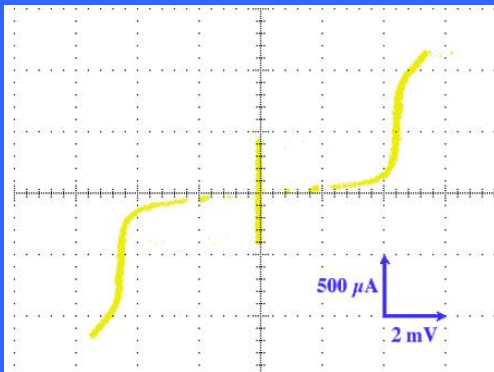


Valid for externally-shunted SIS junctions

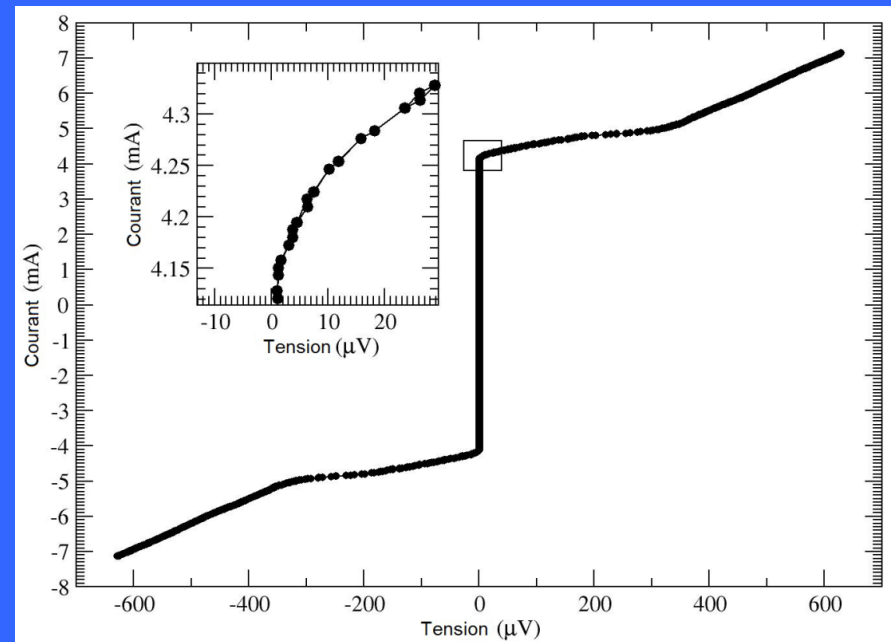
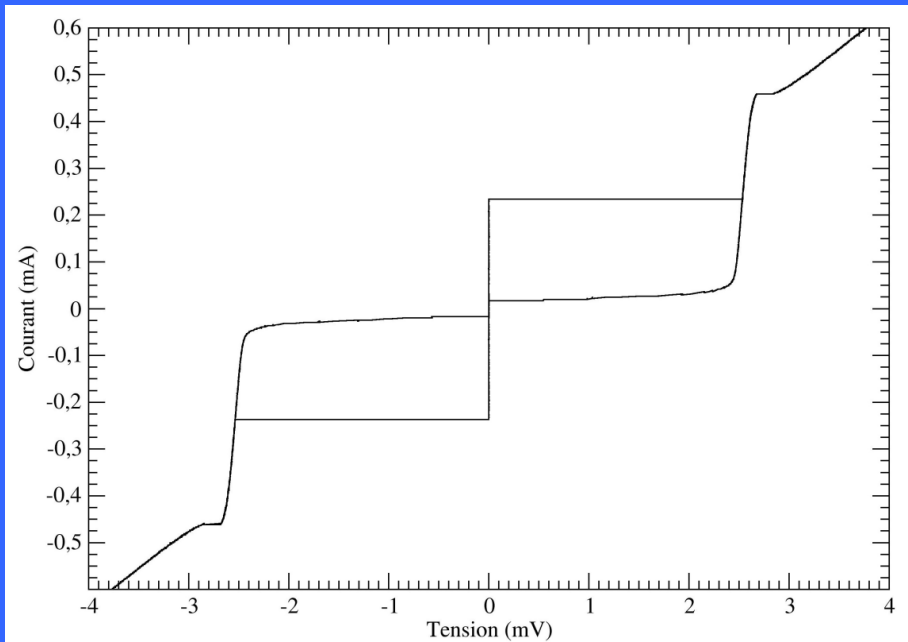
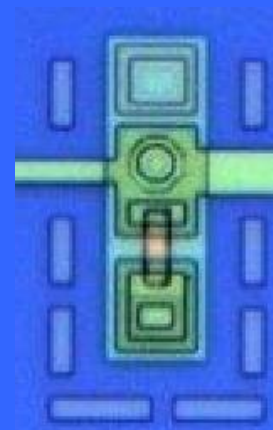
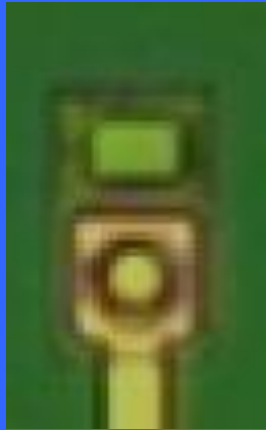
Influence of the McCumber parameter



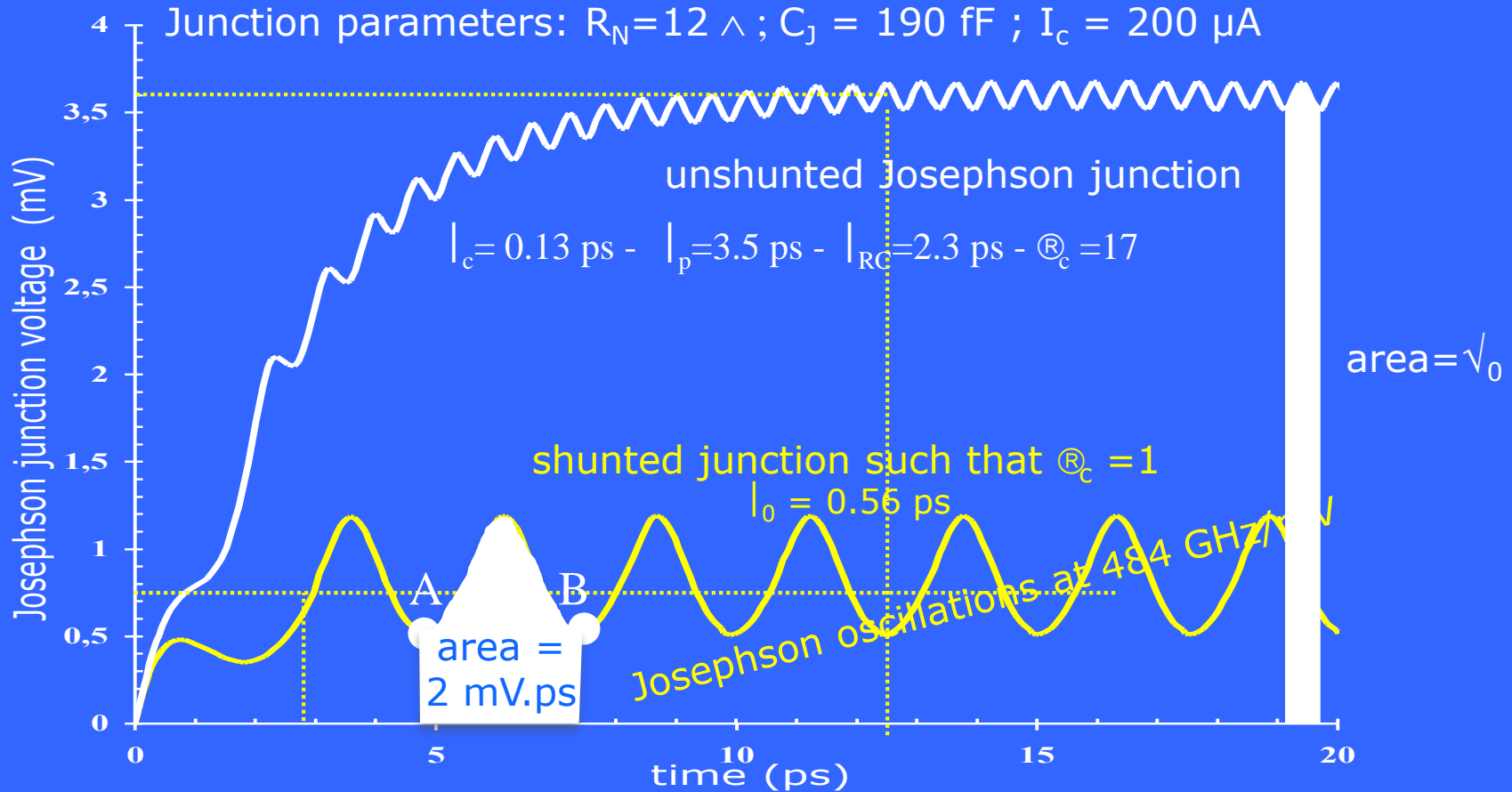
Junctions NbN/MgO/NbN - CEA-INAC Grenoble



I-V characteristics of Josephson junctions



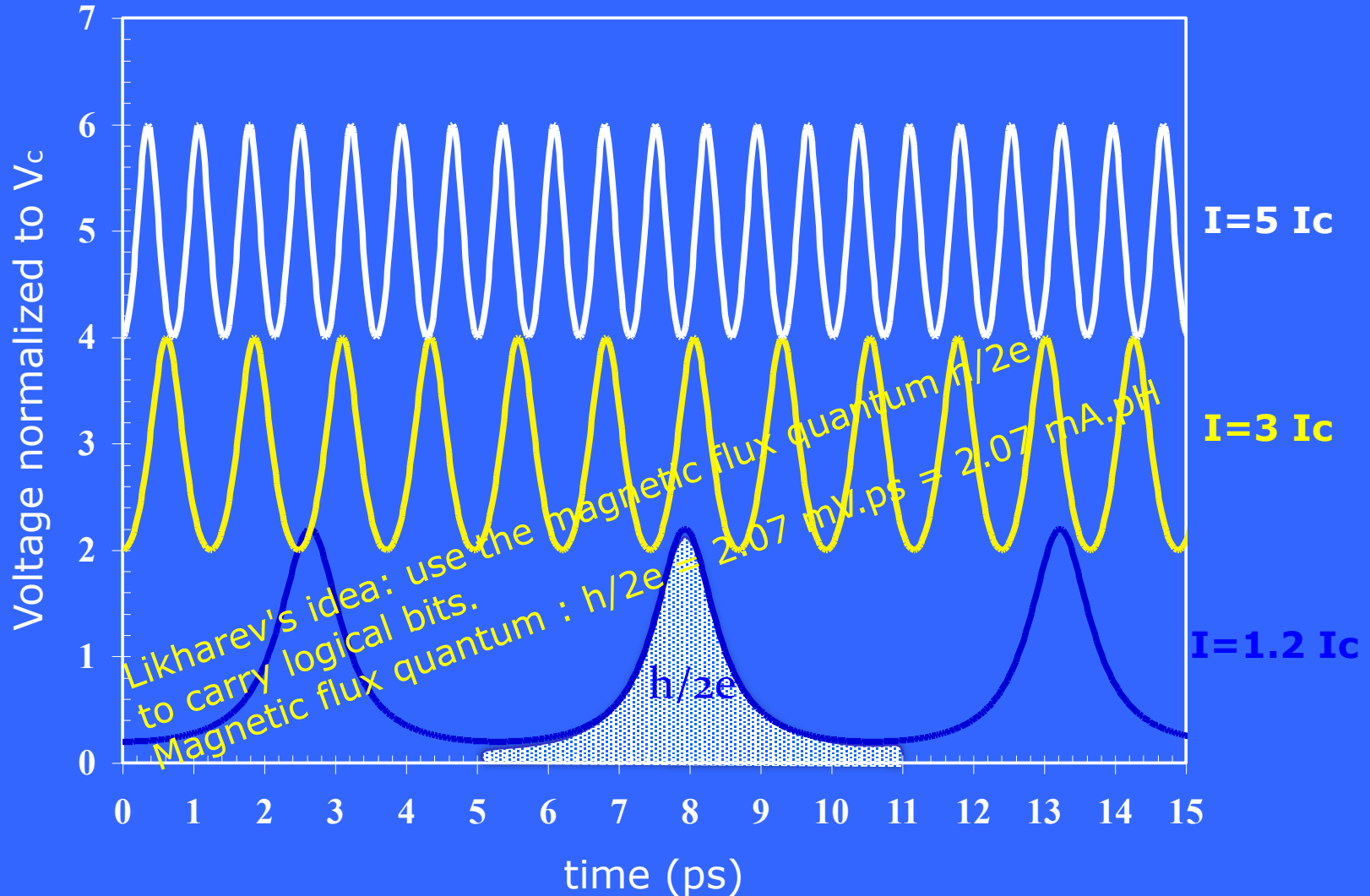
Josephson junction dynamics



$$I = C_J \frac{dV(t)}{dt} + \frac{1}{R_{shunt}} V(t) + I_c \sin j(t) \rightarrow \begin{cases} D_j = 2\rho \\ \dot{V}(t) dt = F_0 \end{cases}$$

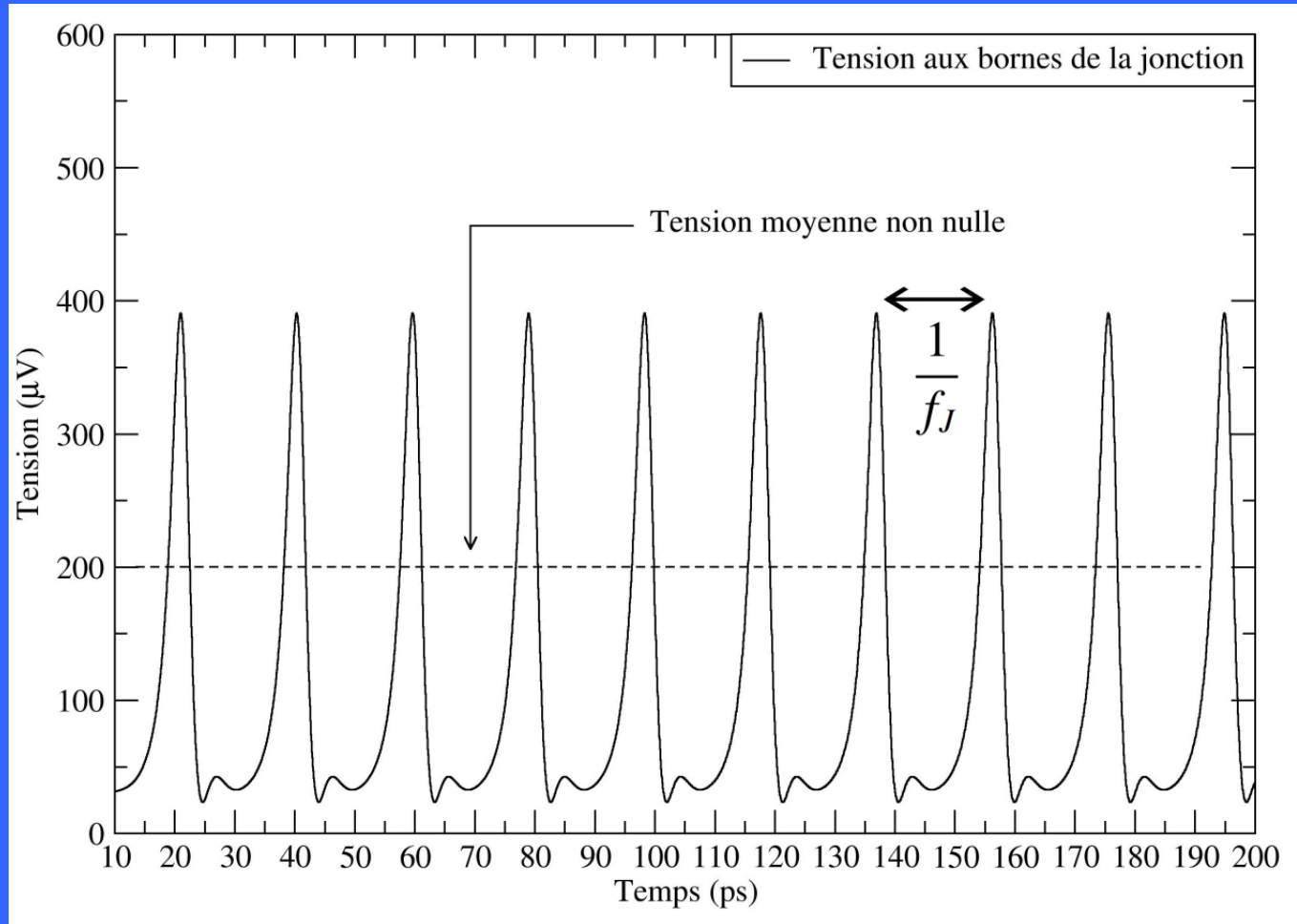
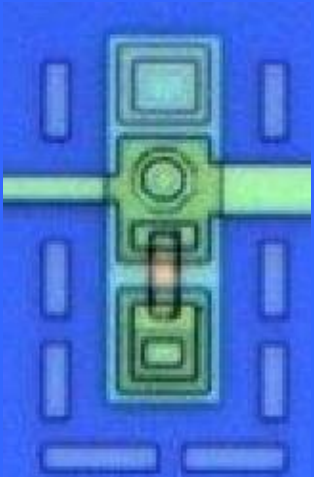
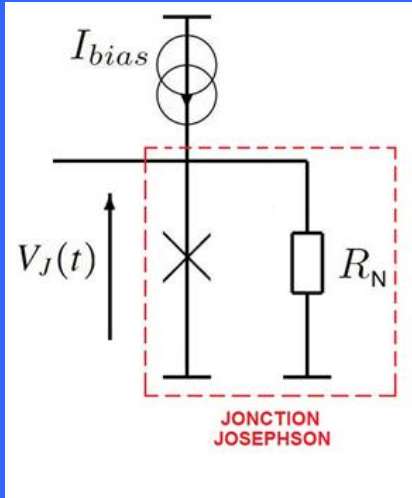
Dynamics of shunted Josephson junctions

Magnetic flux quantum: $h/2e = 2.07 \text{ mV.ps} = 2.07 \text{ mA.pH}$

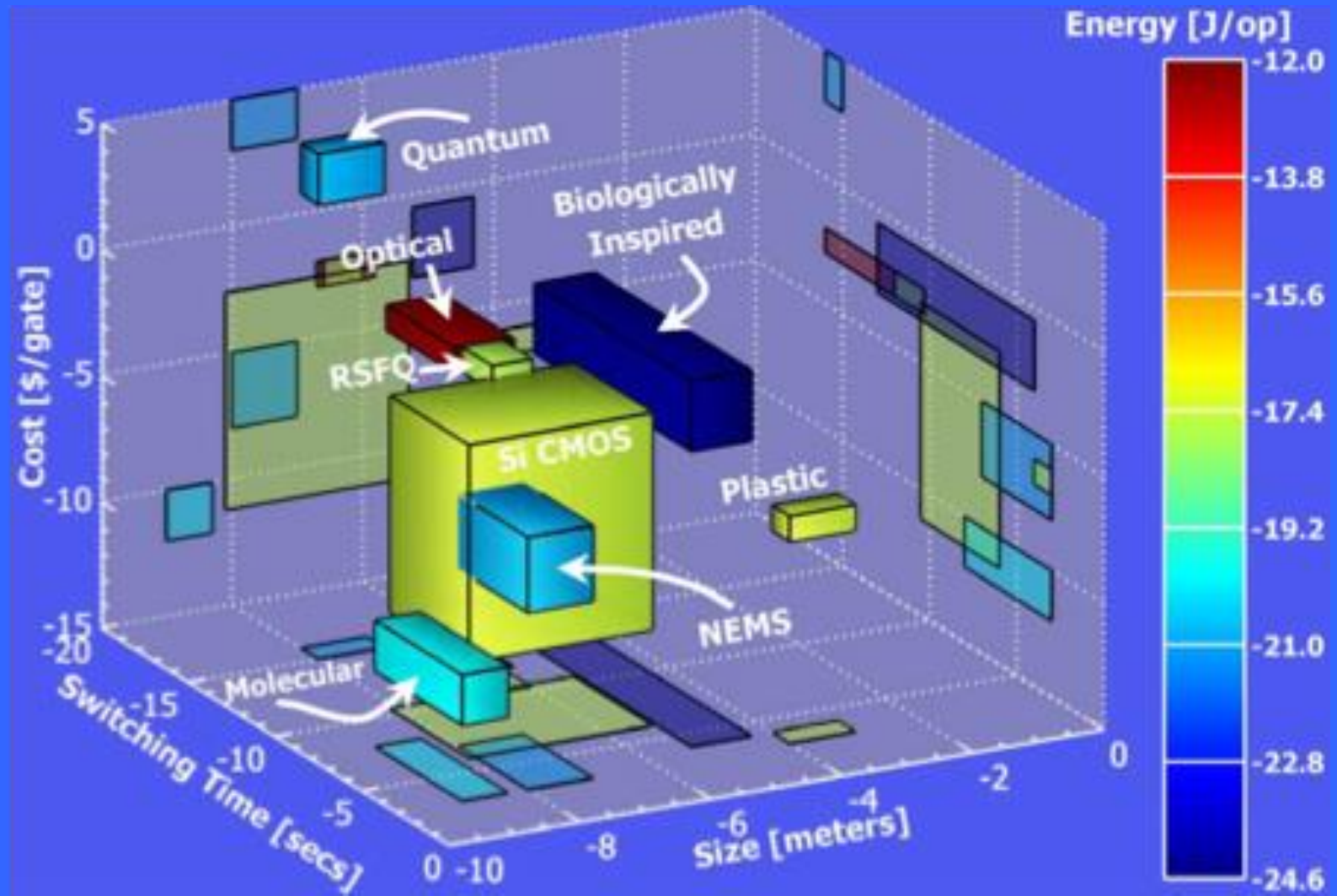


This dynamic logic is called Rapid Single Flux Quantum (RSFQ)

On-chip RSFQ clock

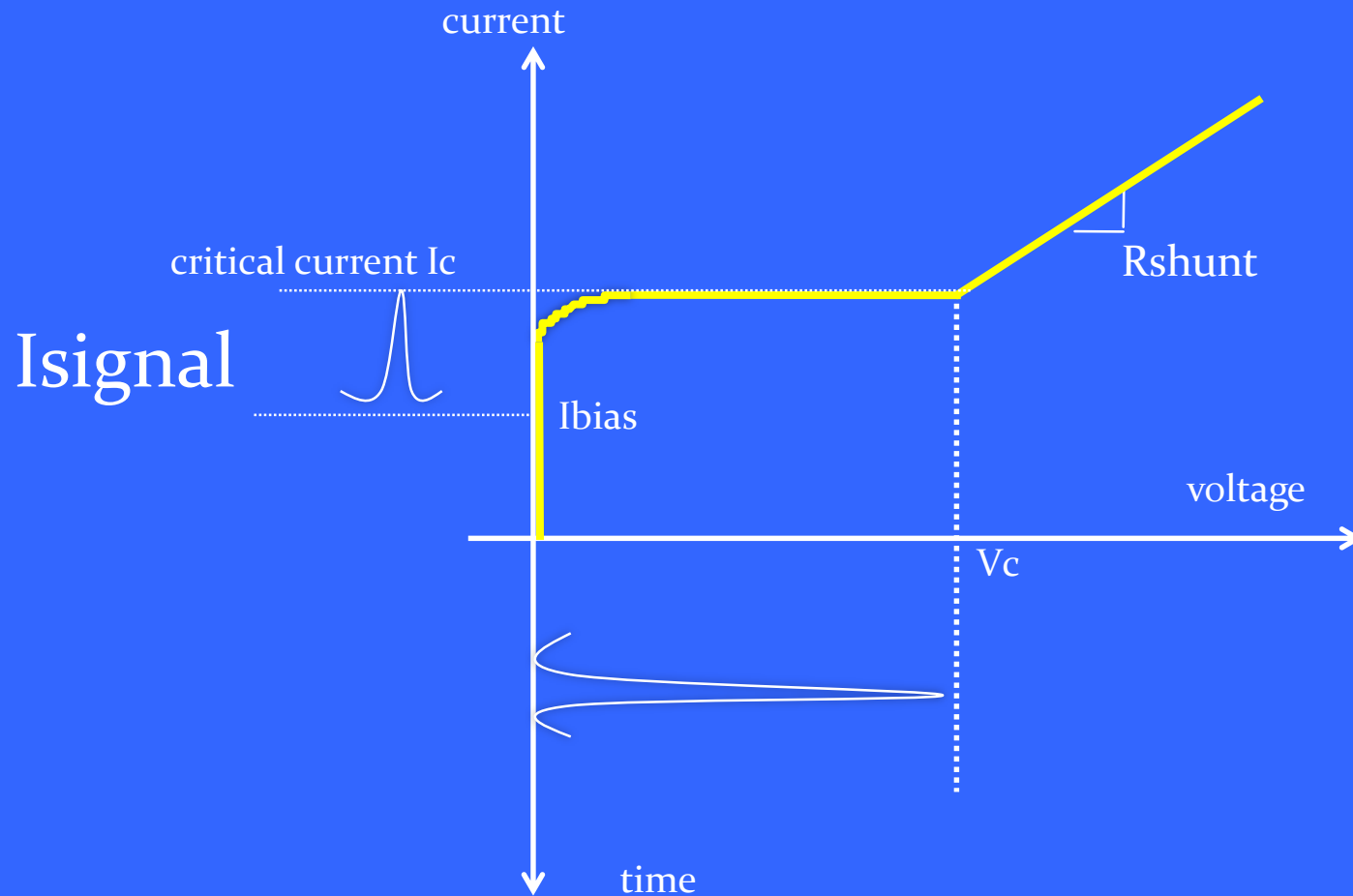


Technological status

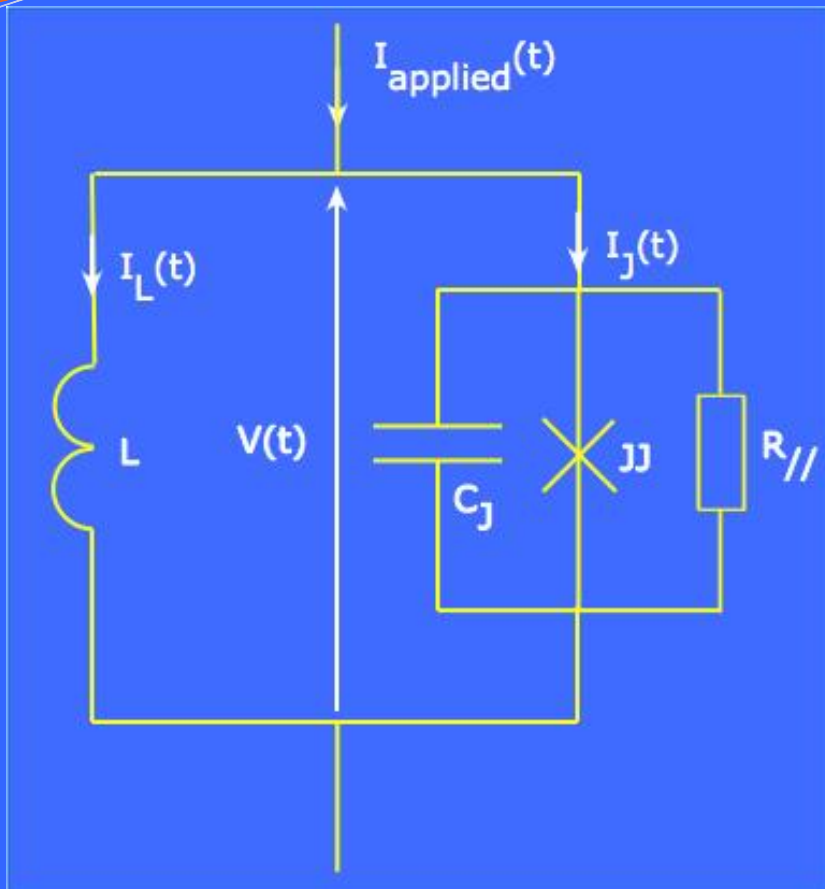


Source: ITRS 2004

How to manage single pulses?



Processing magnetic flux quanta



Kirchhoff's laws:

Nodal rule: $I_{\text{applied}} = I_L + I_J$

Loop rule: $\oint_{\text{loop}} \dot{V}_i = 0$

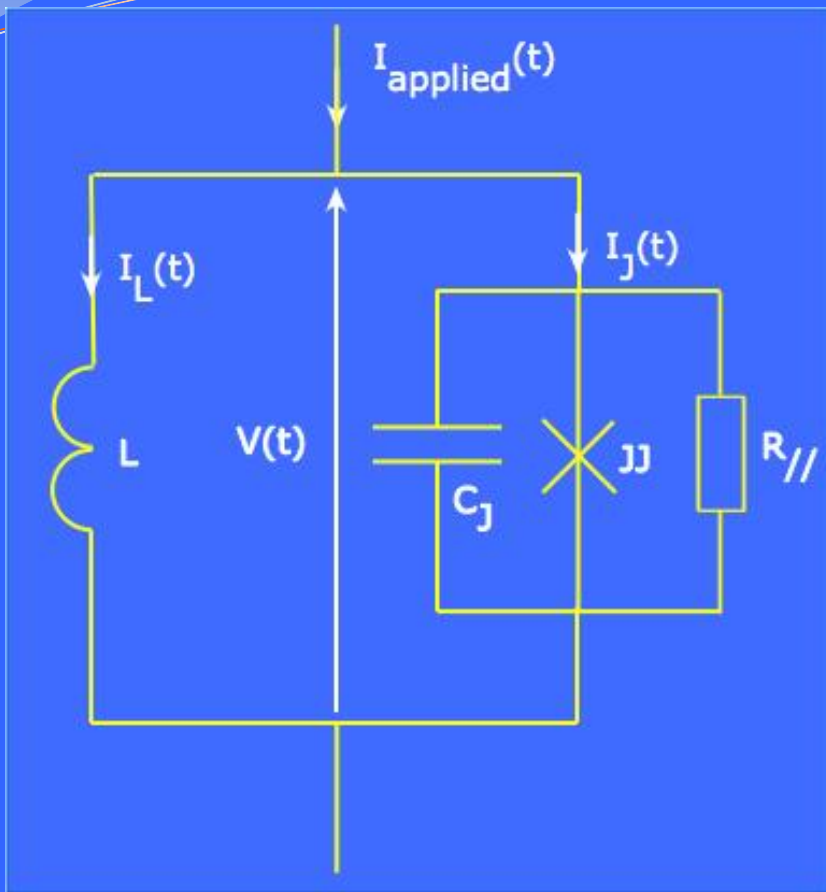
Integration over a loop:

$$\int \left(\sum_{\text{loop}} V_i \right) dt = \int 0 dt = \text{constant}, \quad \text{" time interval}$$

$$\sum_{\text{loop}} \int V_i dt = \frac{F_0}{2\rho} \sum_{\text{loop}} Dj_i = \text{constant} = n F_0$$

Modified Kirchhoff's law (law of phases): $\sum_{\text{loop}} Dj_i = 2n\rho$

Processing flux quanta - static analysis (1/2)



DC-SFQ converter
or
ac SQUID (e.g. rf SQUID)
or
Schmidt trigger

Nodal rule : $I_{applied} = I_L + I_C \sin j$

$$\frac{2\rho LI_{applied}}{F_0} = \frac{2\rho LI_L}{F_0} + \frac{2\rho LI_c}{F_0} \sin j$$

$$j_{ext} = \frac{2\rho}{F_0} LI_{applied} \quad j_L = \frac{2\rho}{F_0} F_L$$

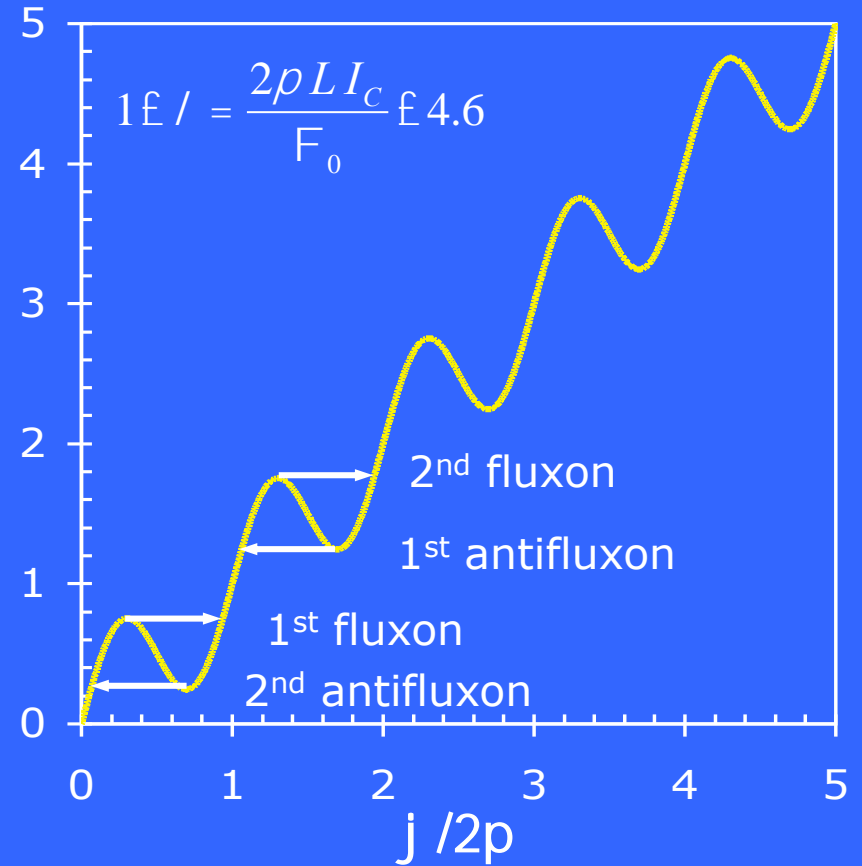
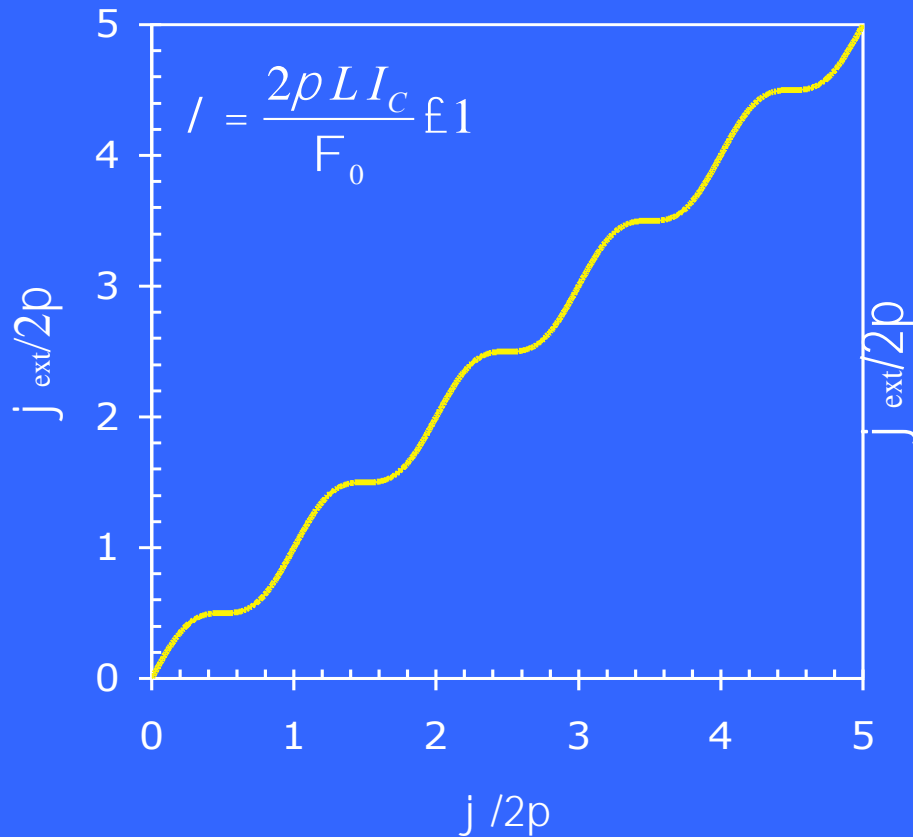
$$l = \frac{2\rho LI_c}{F_0} \quad 2\Phi_0 * \text{maximum number of flux quanta storable before JJ switching}$$

$$\rightarrow j_{ext} = j_L + l \sin j$$

Loop rule : $j_L - j = 2n\rho$

$$j_{ext} = 2n\rho + j + l \sin j$$

Processing flux quanta - static analysis (2/2)



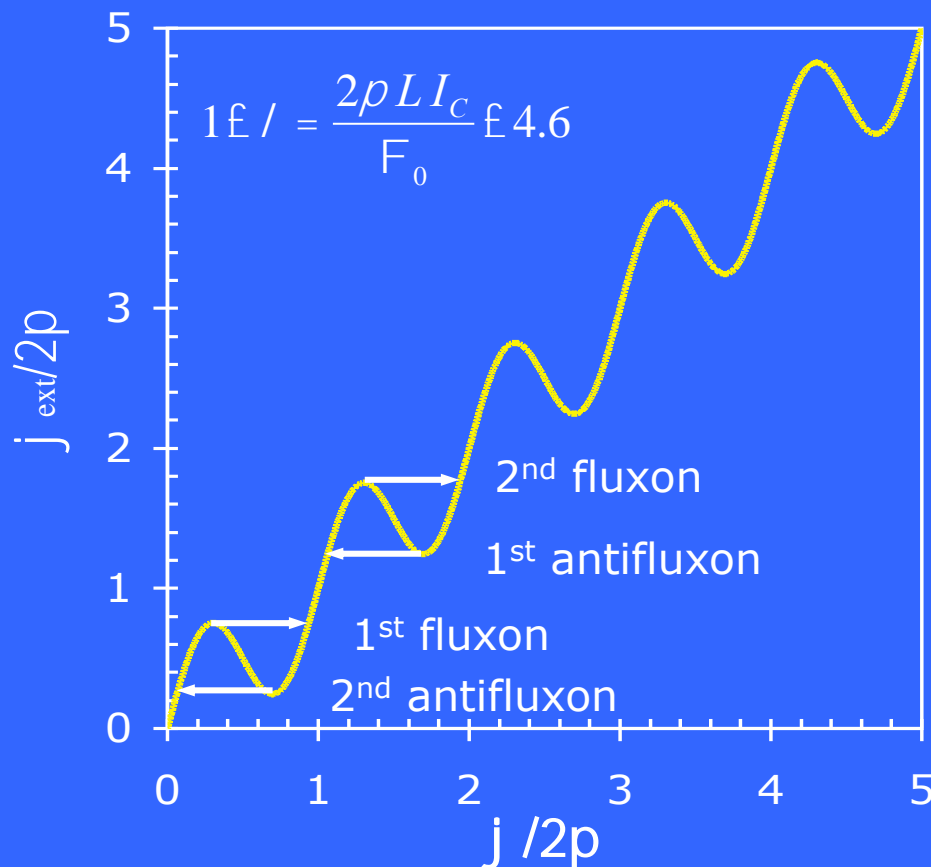
Generation of quantized pulses (1/2)

The first fluxon enters the loop for:

$$j_{ext} \left(1^{st} \text{ fluxon} \right) = \arccos \left(-\frac{1}{l} \right) + \sqrt{l^2 - 1}$$

The second fluxon enters the loop for:

$$j_{ext} \left(2^{nd} \text{ fluxon} \right) = j_{ext} \left(1^{st} \text{ fluxon} \right) + 2\rho$$



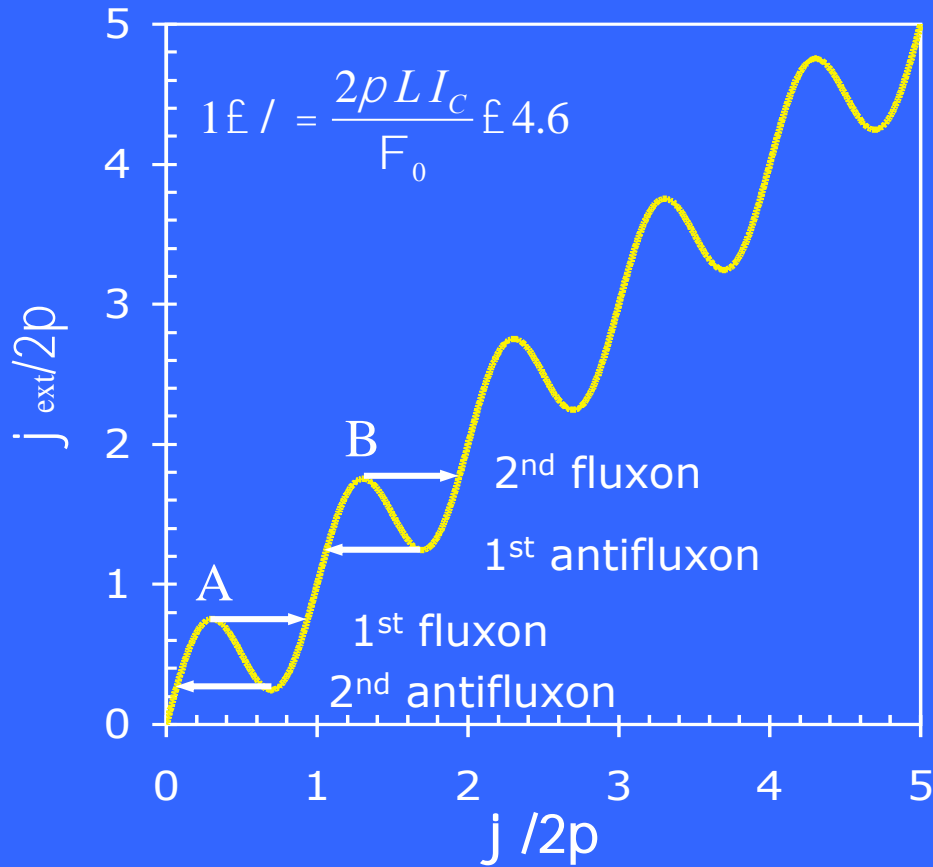
The first antifluxon enters the loop for:

$$j_{ext} \left(1^{st} \text{ antifluxon} \right) = 2\rho - \arccos \left(-\frac{1}{l} \right) - \sqrt{l^2 - 1}$$

The second antifluxon enters the loop for:

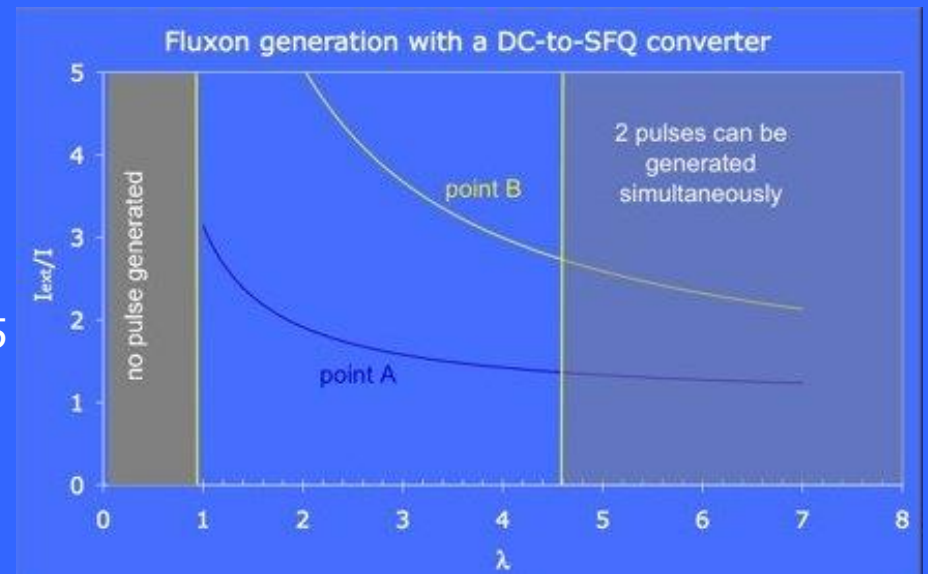
$$j_{ext} \left(2^{nd} \text{ antifluxon} \right) = j_{ext} \left(1^{st} \text{ antifluxon} \right) - 2\rho$$

Generation of quantized pulses (2/2)

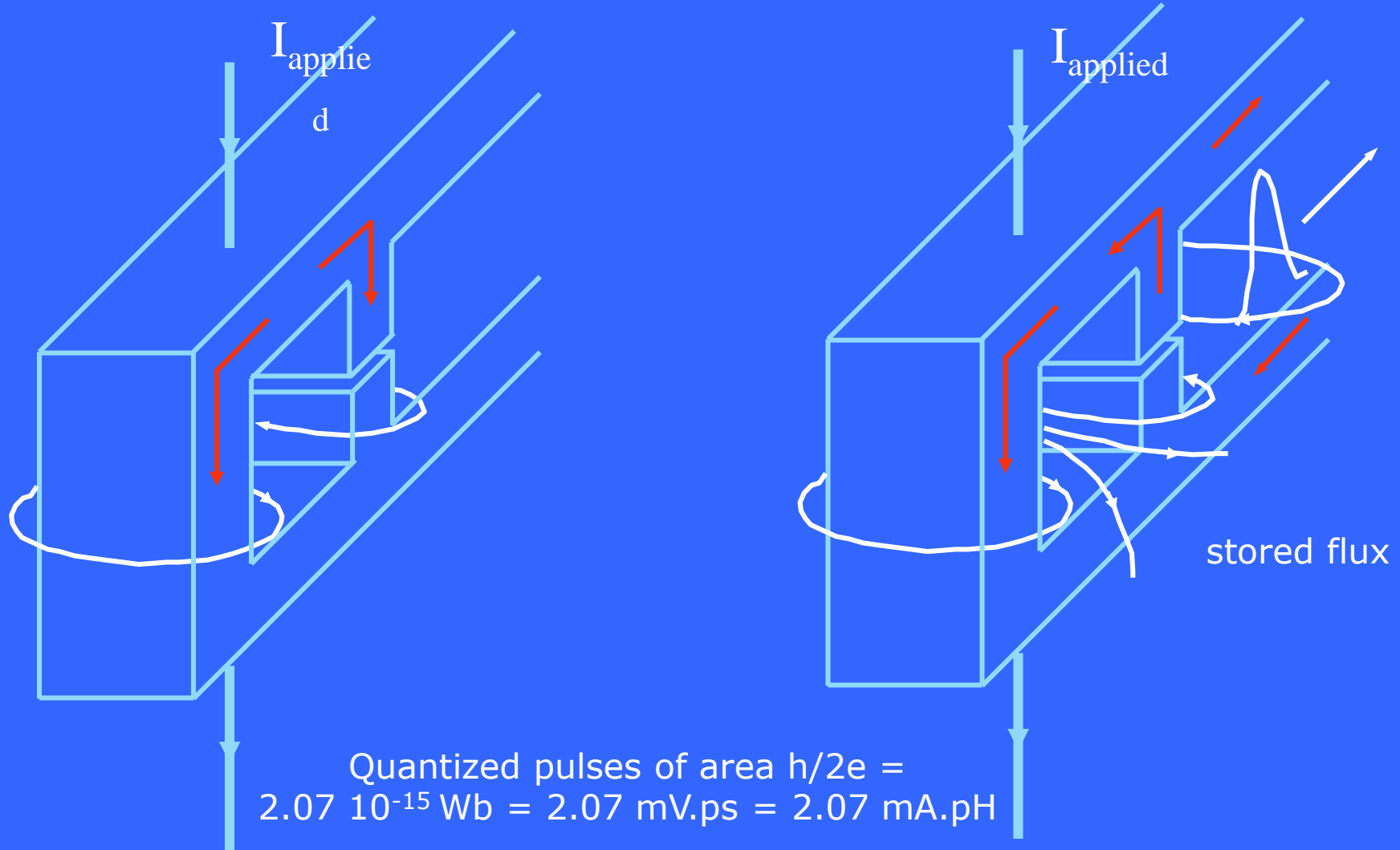


$$\frac{I_{ext}}{I_c}(\text{point A}) = \frac{1}{I} \left[\arccos\left(-\frac{1}{I}\right) + \sqrt{I^2 - 1} \right]$$

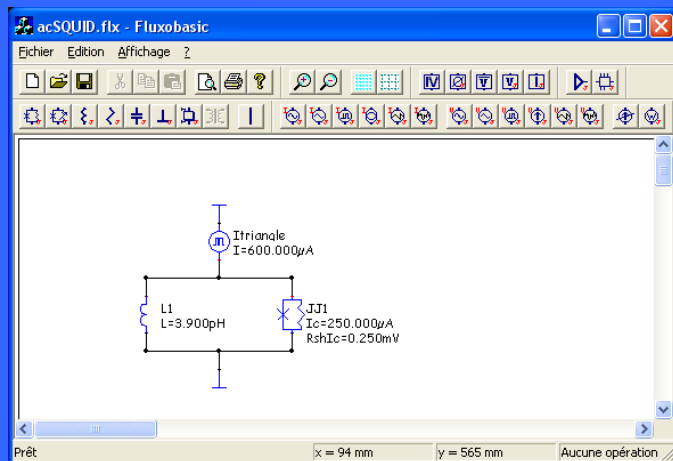
$$\frac{I_{ext}}{I_c}(\text{point B}) = \frac{I_{ext}}{I_c}(\text{point A}) + \frac{2\rho}{I}$$



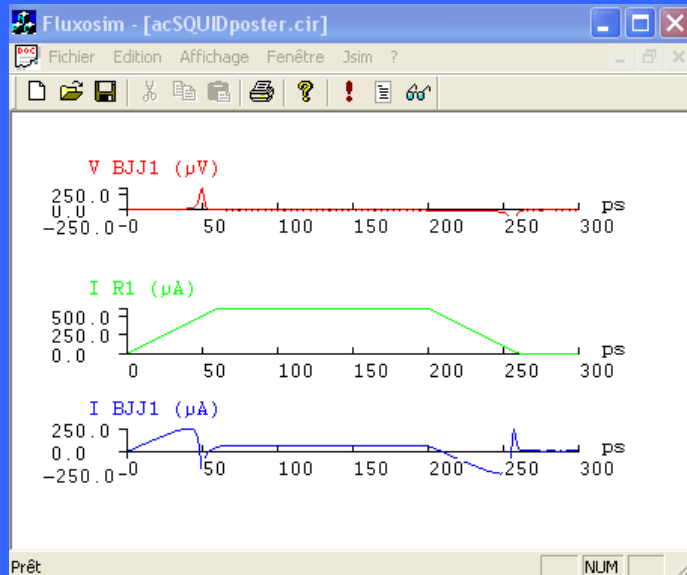
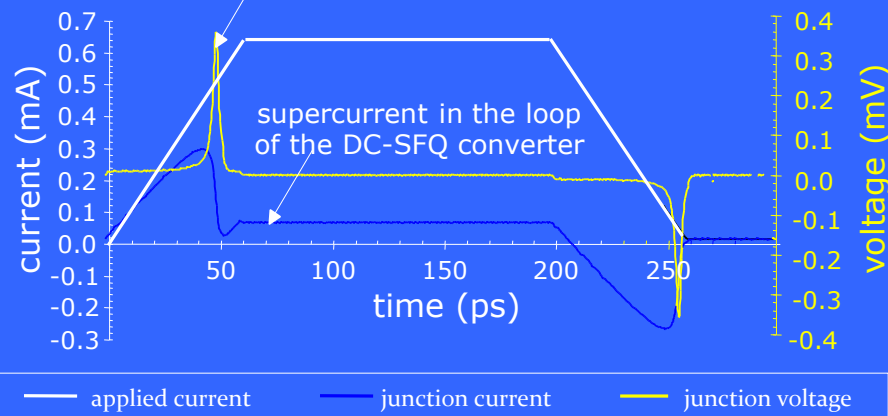
Picosecond pulse and magnetic flux quantum



Simulation of a pulse generator



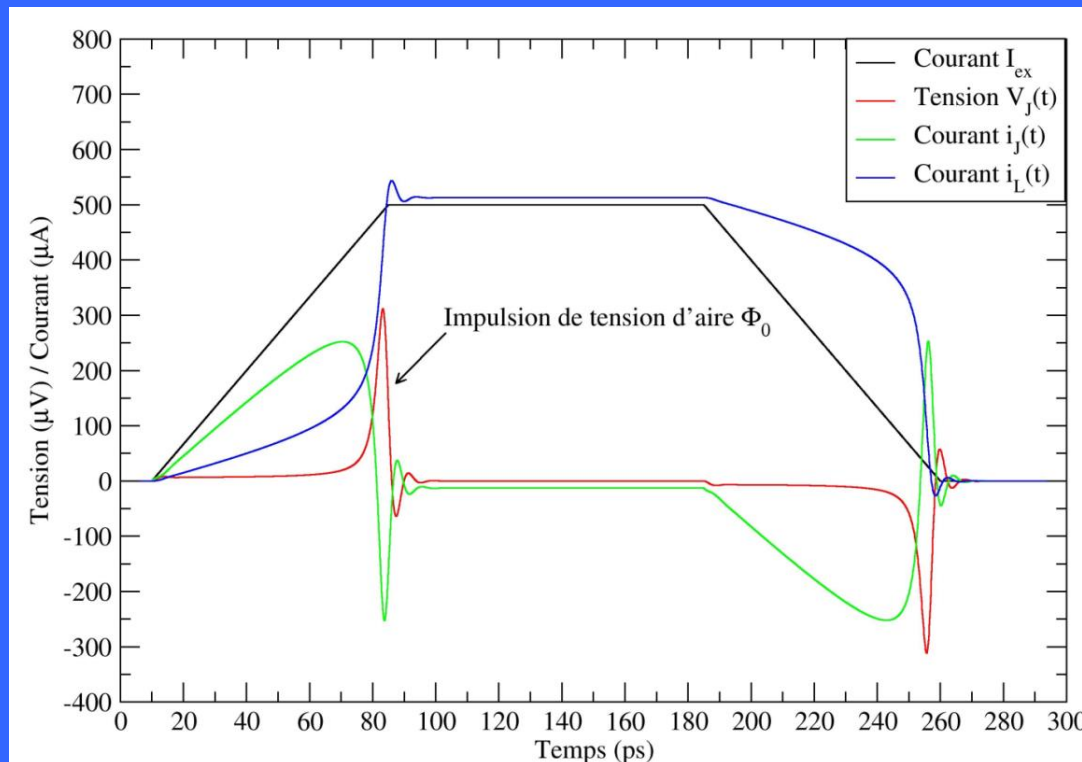
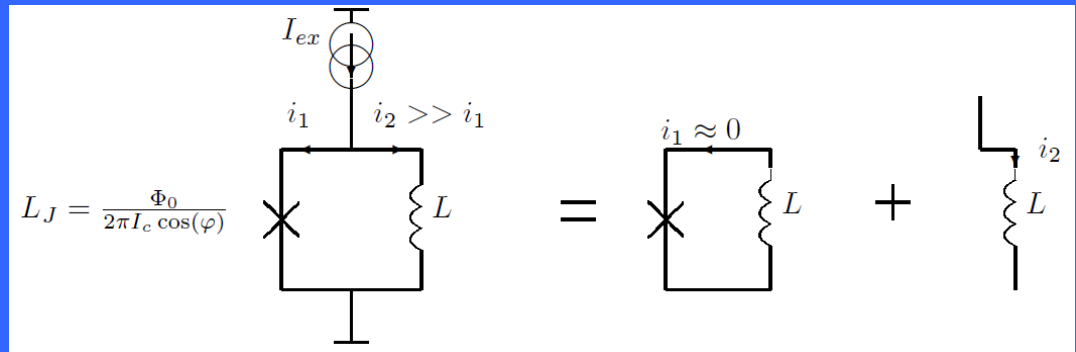
quantized area pulse =
 $2.07 \text{ mV.ps} = 2.07 \text{ mA.pH} = 2.07 \cdot 10^{-15} \text{ Wb}$



```
Netlist
* ..... Netlist du schéma acSQUIDposter.flx créé par Fluxbasic .....
BJJ1 22 0 JJRS1
RBJJ1 22 0 1.0000hm
L1 22 0 3.900pH
ITRIANGLE 0 36 PULSE(DMA 600.000uA 0.000ps 60.000ps 60.000ps 140.000ps 350.000ps)
R1 36 22 0.0010hm
.MODEL JJRS1 JJ(RTYPE=0, RN=10.0000hm, ICRT=250.000uA, CAP=0.000IF, VG=2)
.PRINT DEWV BJJ1
.PRINT DEVI R1
.PRINT DEVI BJJ1 JJTOTAL
.TRAN 1ps 300.000ps 0.000ps 1ps
.END
* ..... fin de la netlist du schéma acSQUIDposter.flx .....
OK
Cancel
```

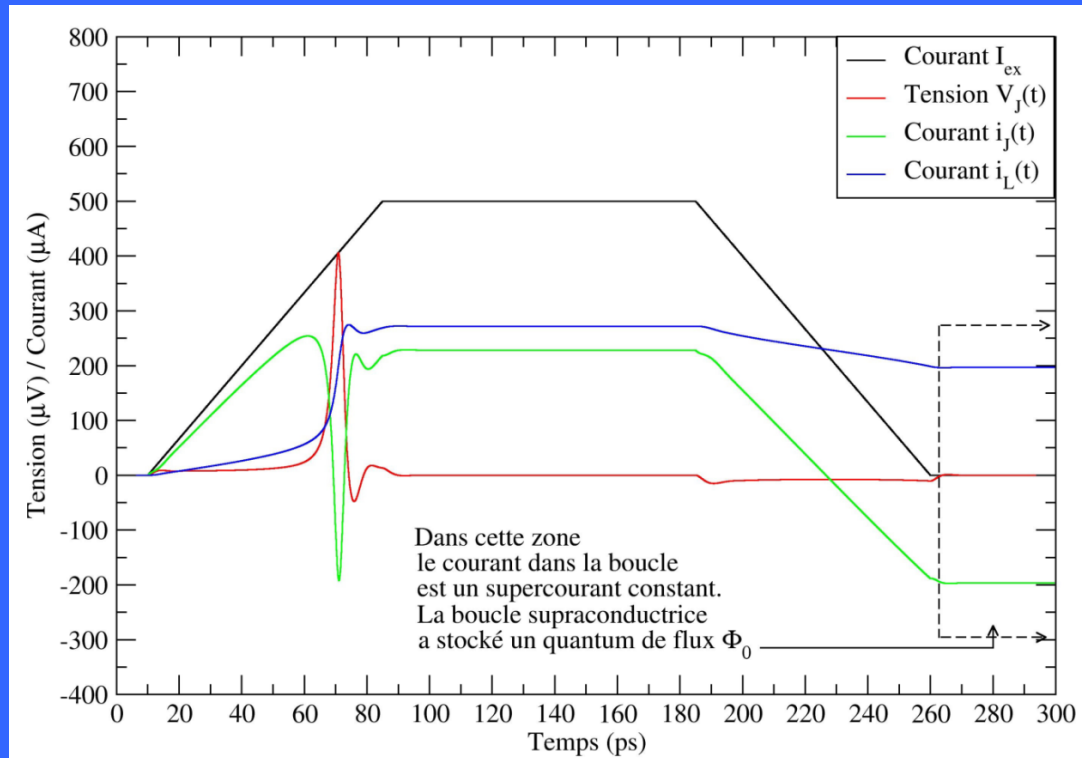
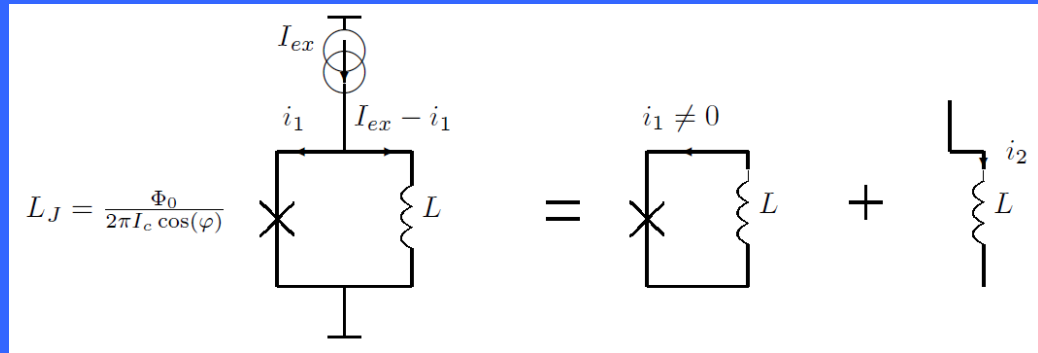
Pulse transmission

$$L \cdot I_c < \Phi_0$$

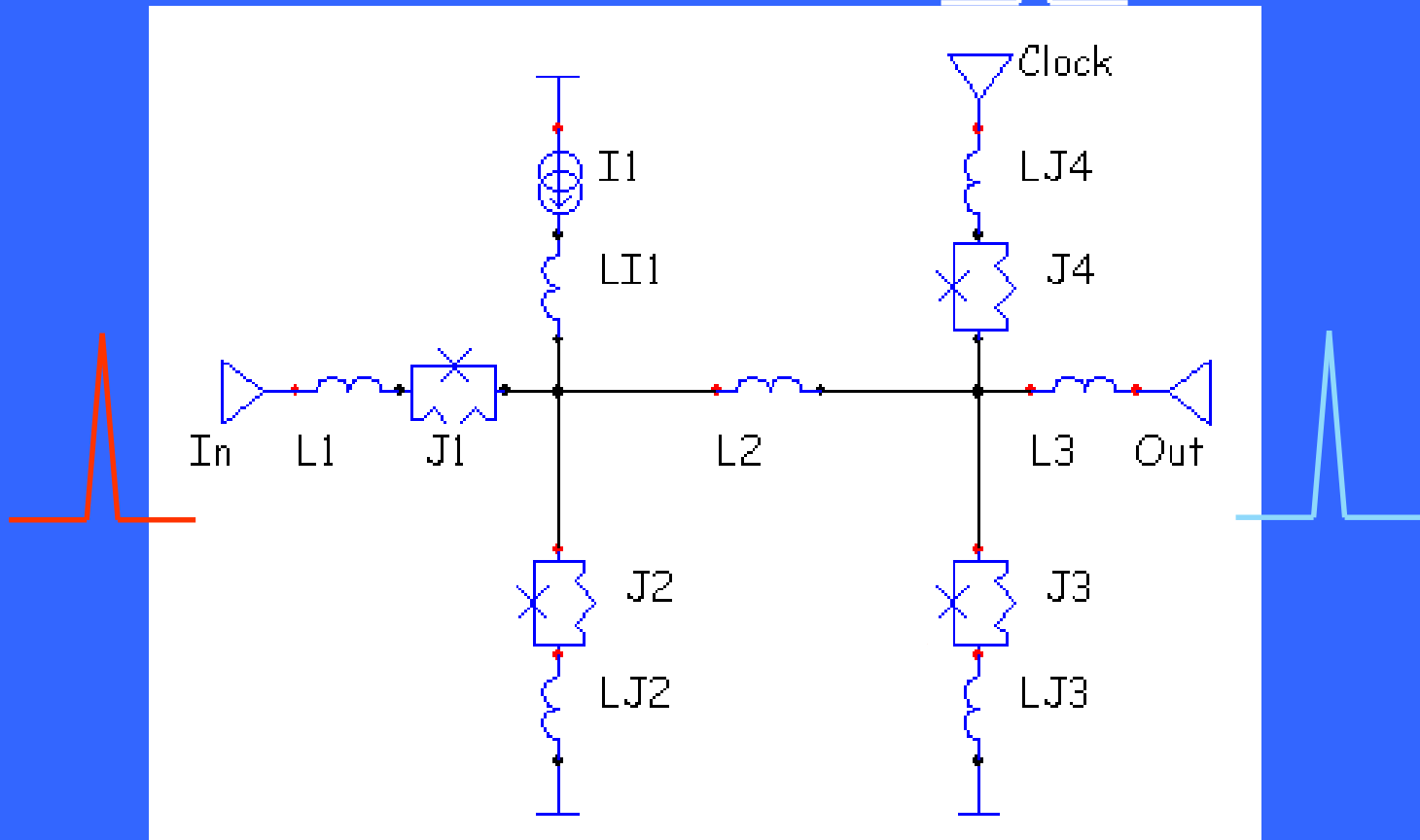


Pulse storage

$$L \cdot I_c > \Phi_0$$



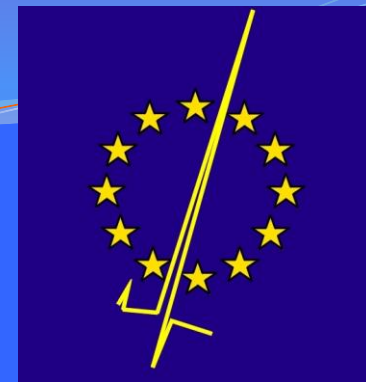
Example of SFQ gate: the Delay-Flip-Flop (DFF)



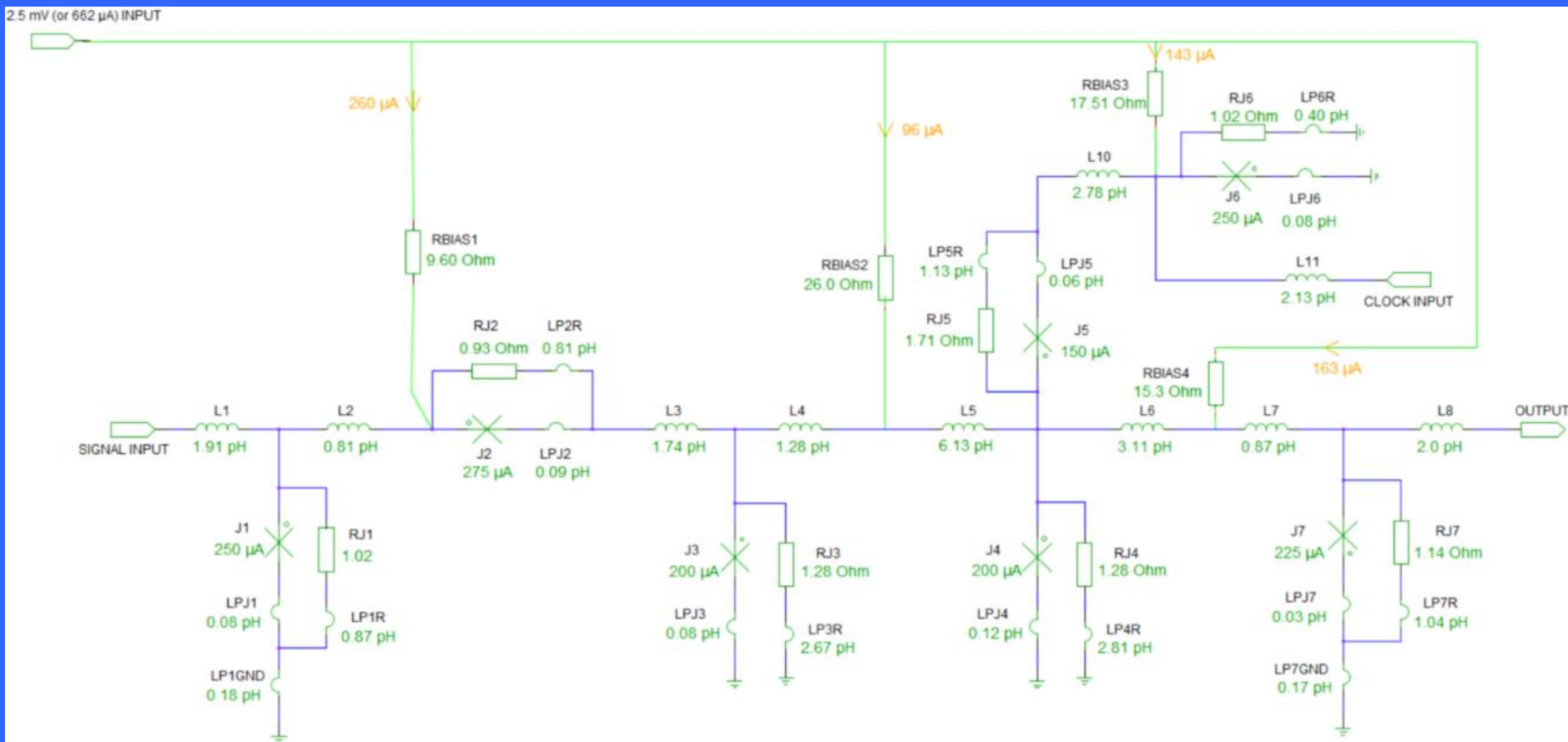
The digital signal is coded with 2 states, between two clock pulses :

- '0' : no pulse
- '1' : one quantized pulse (SFQ pulse)

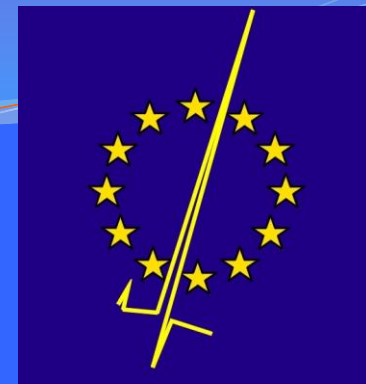
Schematics of the Delay-Flip-Flop cell FLUXONICS Cell Library



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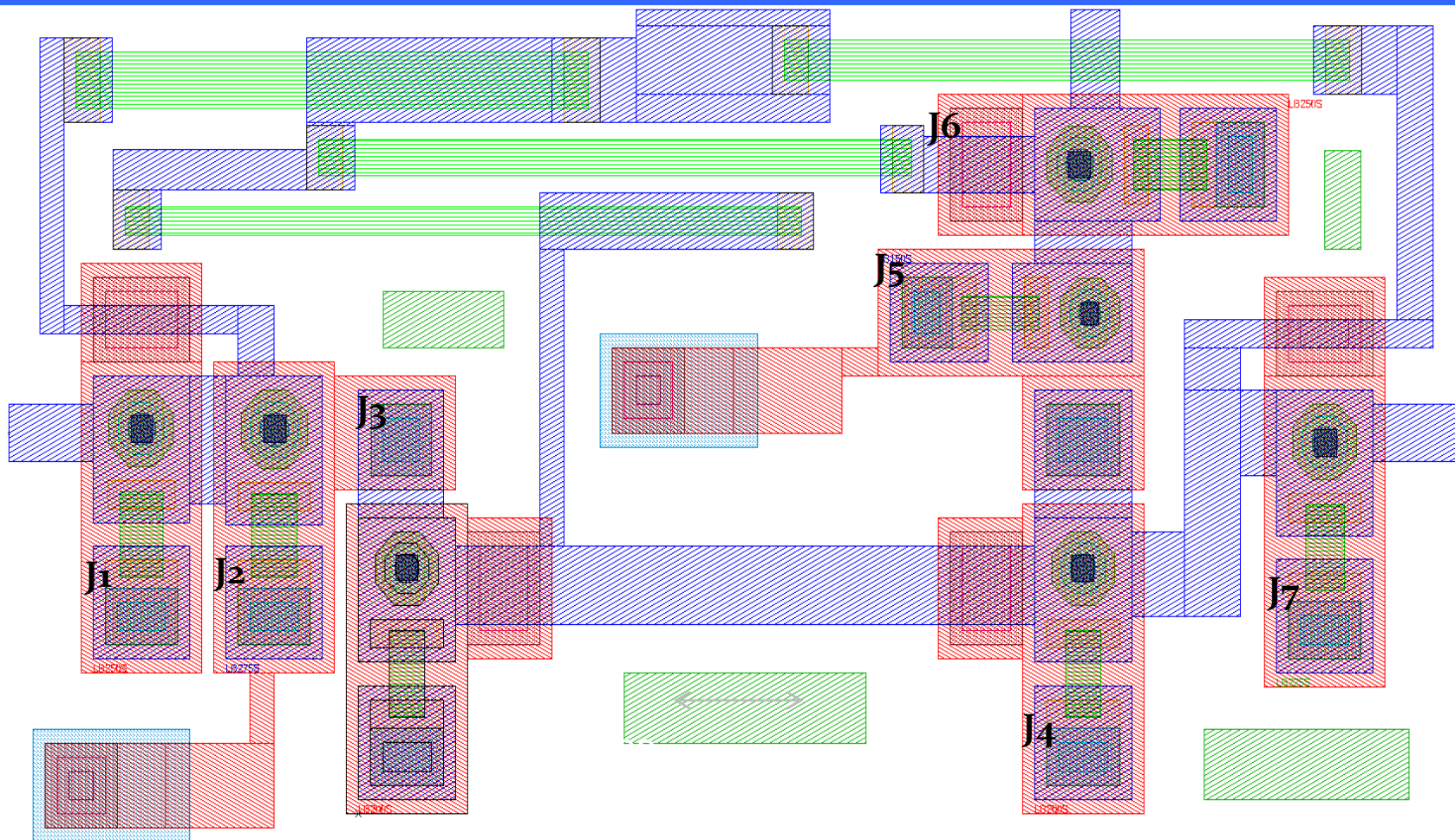


Layout of the Delay-Flip-Flop cell FLUXONICS Cell Library

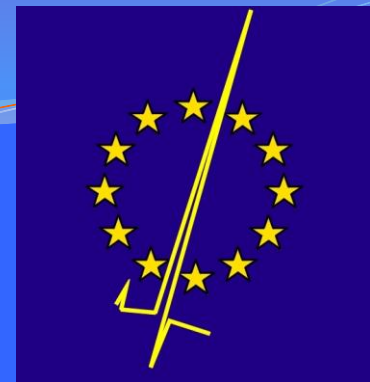


www.FLUXONICS.eu

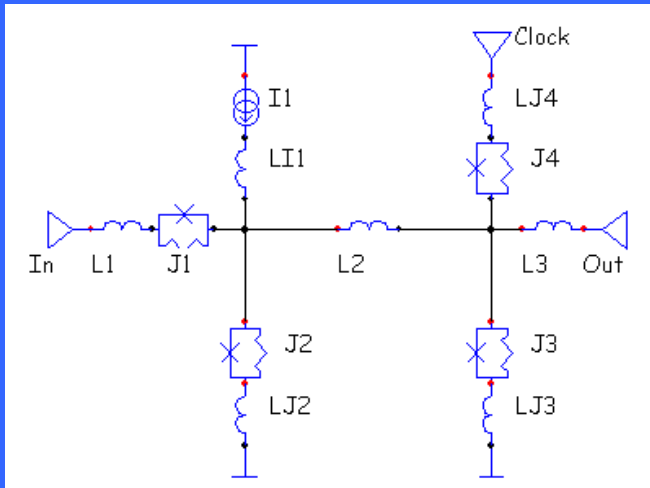
Layout for the Nb/Al-AlO_x/Nb technology – FLUXONICS Foundry – IPHT Jena - Germany



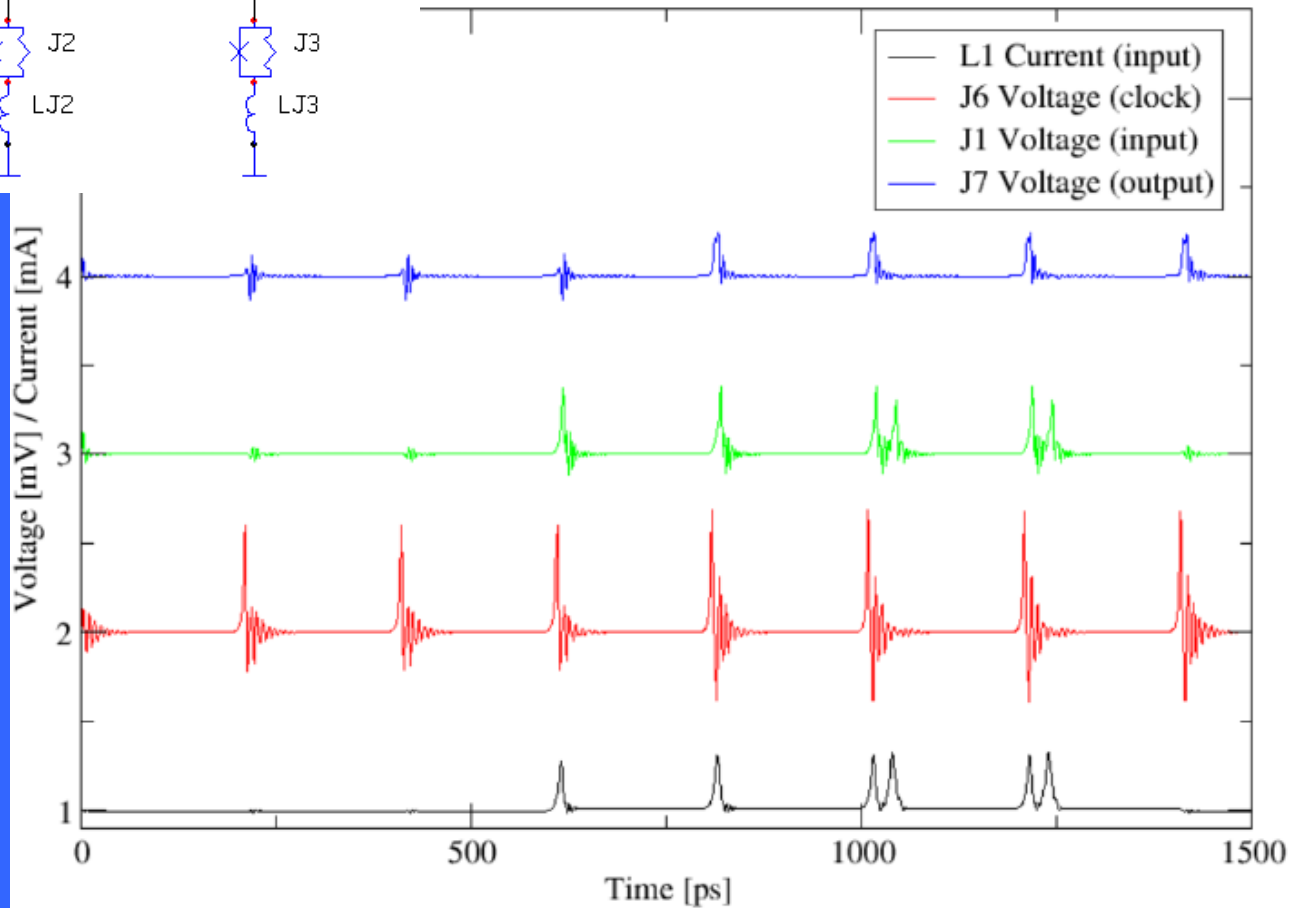
Simulation of the Delay-Flip-Flop cell FLUXONICS Cell Library



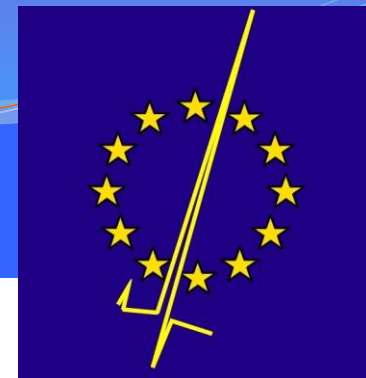
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$R_{N}I_C = 0,256 \text{ mV}$, $f = 5\text{GHz}$, $\beta_C = 1$

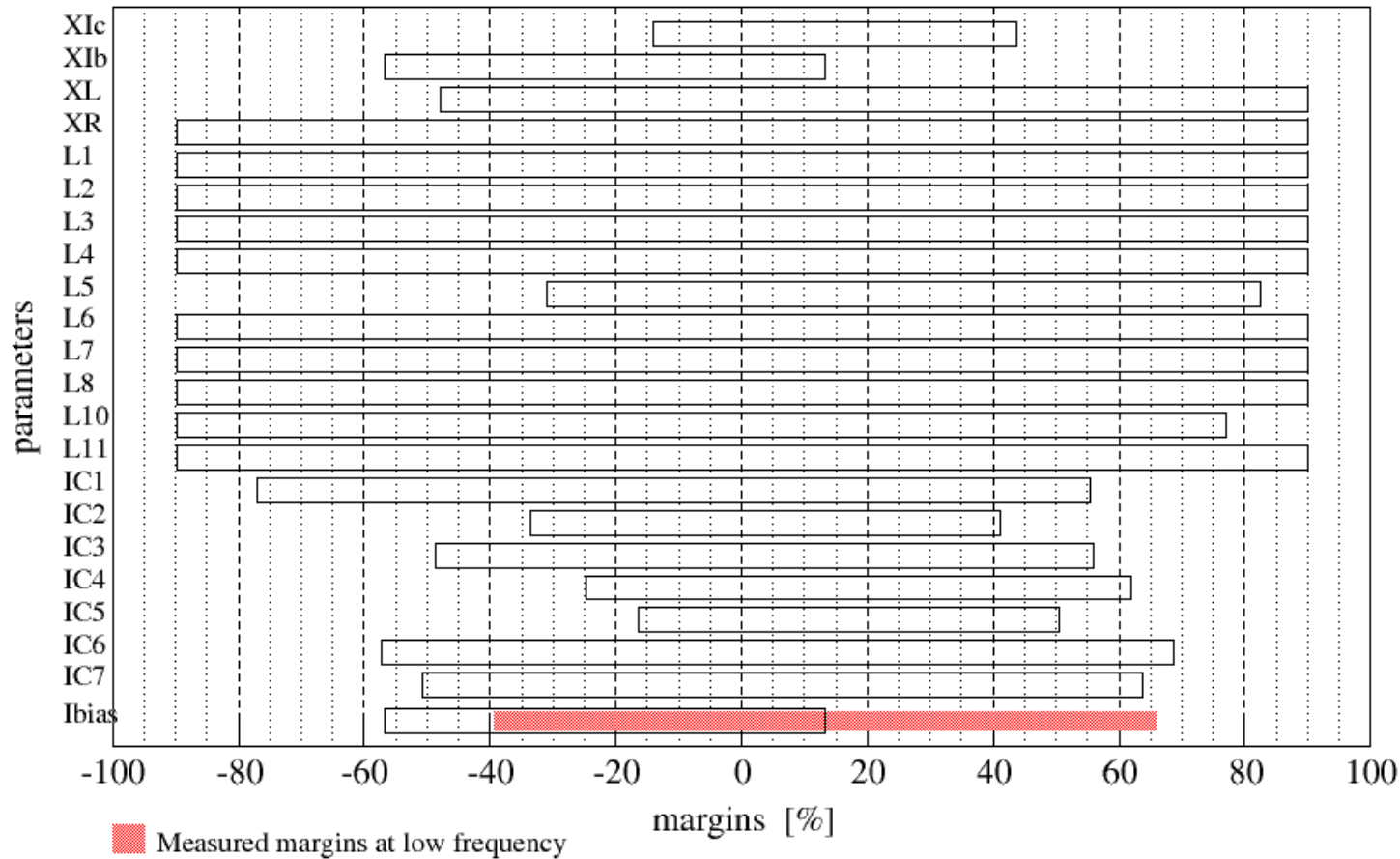


Margins of the Delay-Flip-Flop cell FLUXONICS Cell Library

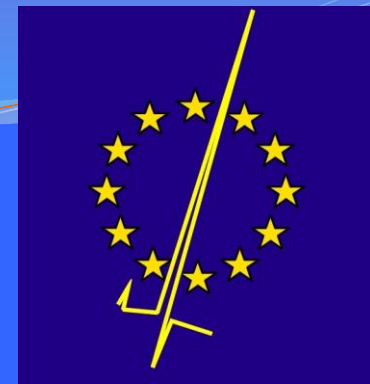


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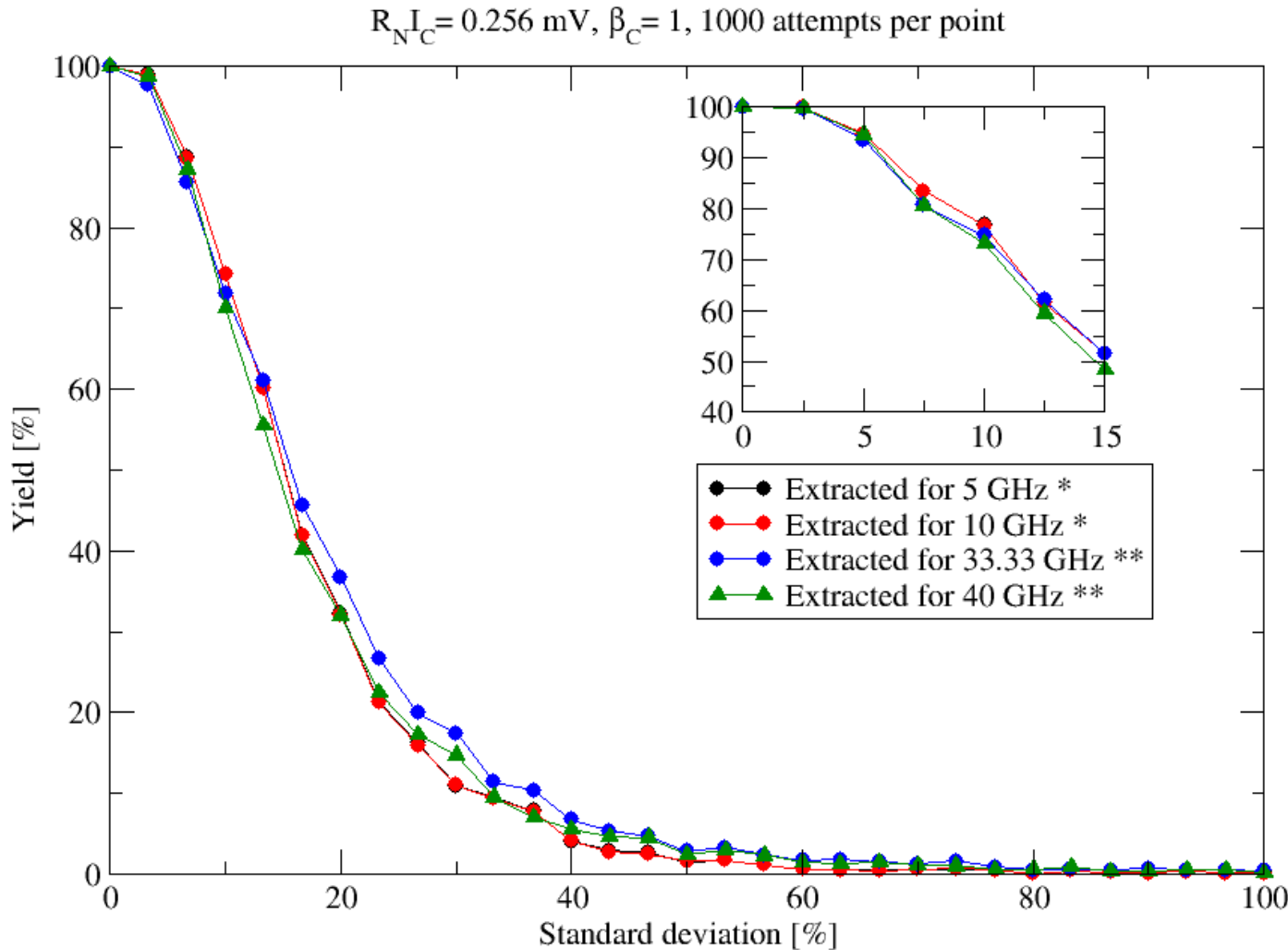
$R_{N^C} I_C = 0.256 \text{ mV}$, $f = 5 \text{ GHz}$, $\beta_C = 1$



Yield of the Delay-Flip-Flop cell FLUXONICS Cell Library



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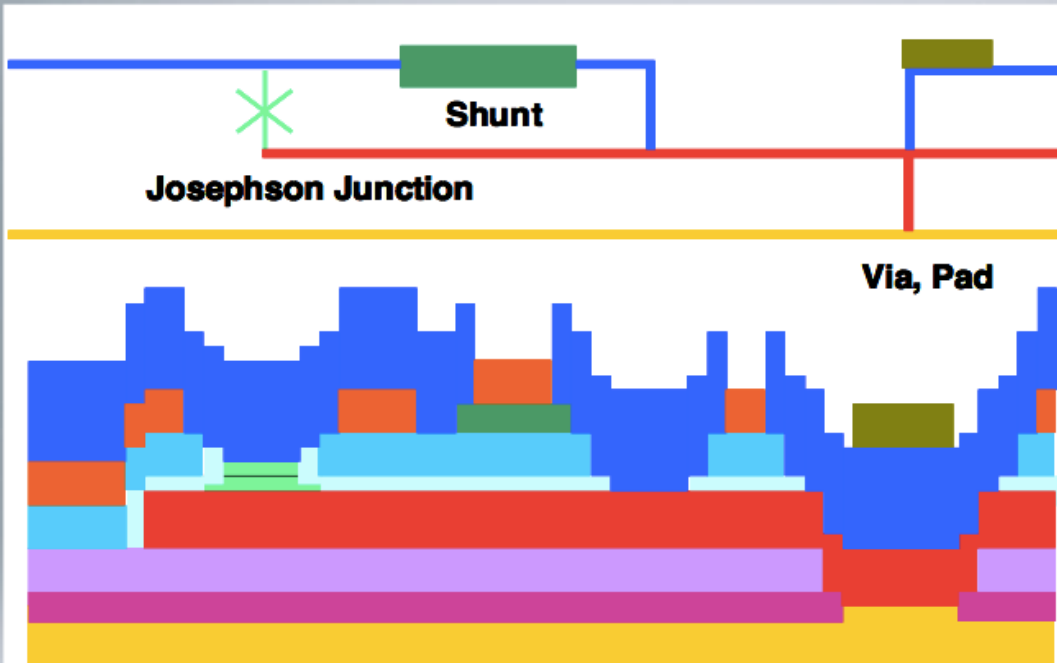
* Complex test sequence including double SFQ pulses

** Simplified test sequence without double SFQ pulses



RSFQ process cross-section FLUXONICS Foundry

RSFQ process – cross section



Layer	Thickness	Material
R2	50 nm	Au
M2	350 nm	Nb
I2	150 nm	SiO
R1	80 nm	Mo
I1B	150 nm	SiO
I1A	70 nm	Nb ₂ O ₅
T1	60 nm 12 nm 30 nm	Nb Al ₂ O ₃ Nb
M1	250 nm	Nb
I0B	200 nm	SiO
I0A	50 nm	Nb ₂ O ₅
M0	200 nm	Nb

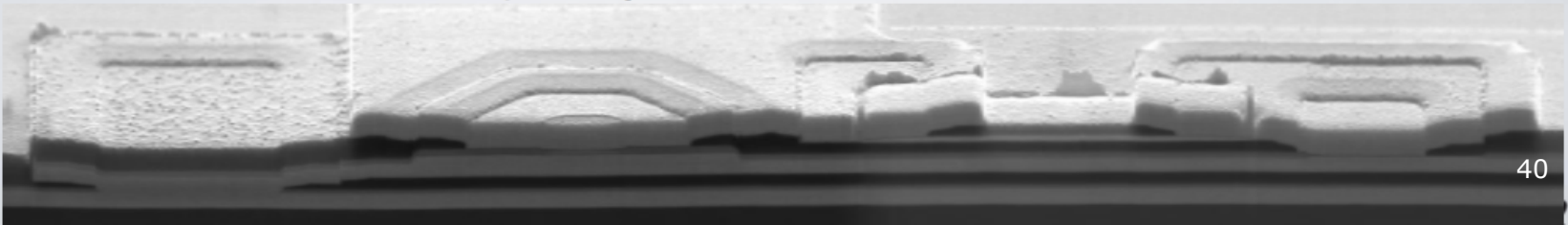
iphtjena

Via

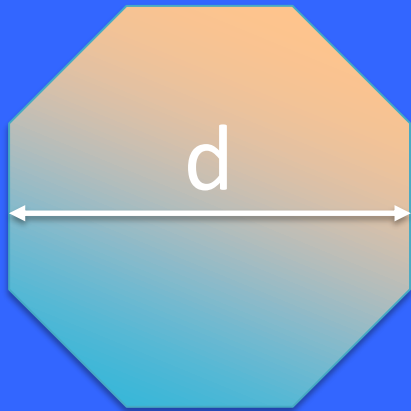
Josephson junction

Shunt

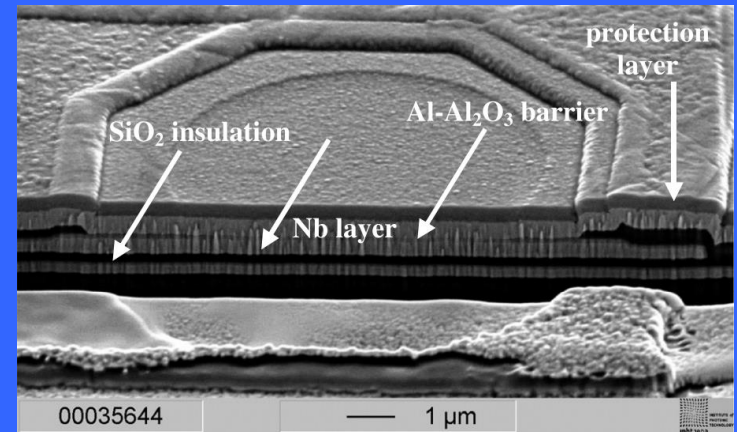
Via



RSFQ technology parameters and tolerances FLUXONICS Foundry



Josephson junction
specific capacitance :
 $50 \pm 2 \text{ fF}/\mu\text{m}^2$



FLUXONICS octagonal Josephson junctions

RSFQ technology parameters and tolerances

FLUXONICS Foundry

- ◆ Current density of 1 kA/cm² based on Nb/Al-AlO_x/Nb tri-layers
- ◆ 3 metal layers M0, M1 & M2 : 1st for ground plane and 2nd/3rd for wiring
- ◆ Characteristic voltage $V_c=256 \mu\text{V}$
- ◆ McCumber parameter $\beta_c = 1$
- ◆ 13 shunted octagonal Josephson junctions for digital operation

Junction	Lb100	Lb125	Lb150	Lb175	Lb200	Lb225	Lb250	Lb275	Lb300	Lb325	Lb350	Lb375	Lb400
I _c (μA)	100	125	150	175	200	225	250	275	300	325	350	375	400
area (μm ²)	9.94	12.44	15.11	17.59	20.09	22.54	25.13	27.59	29.99	32.47	35.03	37.42	40.18
d (μm)	3.4	3.8	4.3	4.7	4.9	5.2	5.5	5.9	6.1	6.3	6.5	6.8	7.0
R _{shunt} (Ω)	2.58	2.06	1.69	1.46	1.27	1.14	1.02	0.93	0.85	0.79	0.73	0.68	0.64

RSFQ technology parameters and tolerances FLUXONICS Foundry

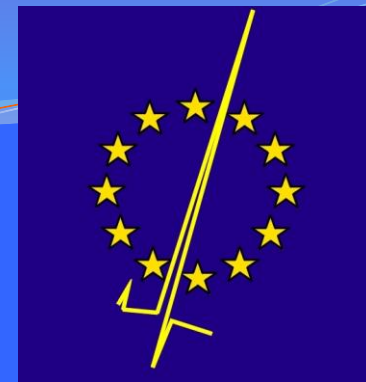


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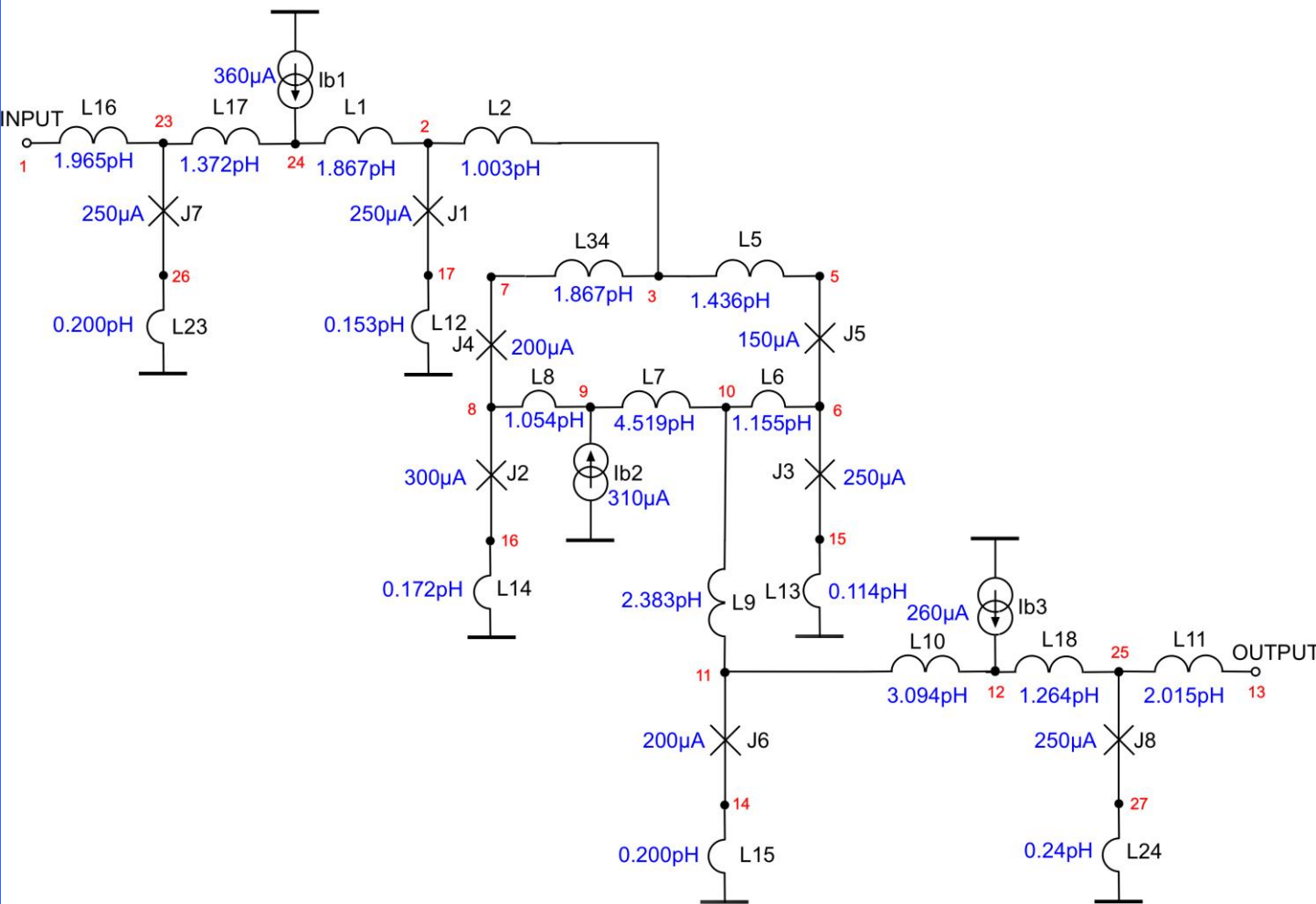
Parameter	Nominal Value	Inter Wafer tolerance	On wafer tolerance	On chip tolerance
Josephson current density J_C	1000 A/cm ²	± 20 %	± 15 %	± 5 %
Sheet Resistance R_{square}	1.0 Ω	± 20 %	± 10 %	± 5 %
Inductance L_{10} M1-M0	0.52 pH	± 10 %	± 5 %	± 2 %
Inductance L_{21} M2-M1	0.64 pH	± 10 %	± 5 %	± 2 %
Inductance L_{20} M2-M0	0.81 pH	± 10 %	± 6 %	± 2 %

The Toggle Flip-Flop cell



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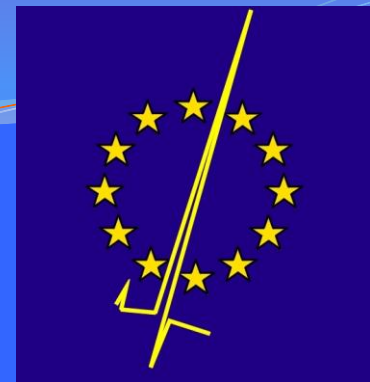
FLUXONICS FOUNDRY - 2012 - TFF with parasitics



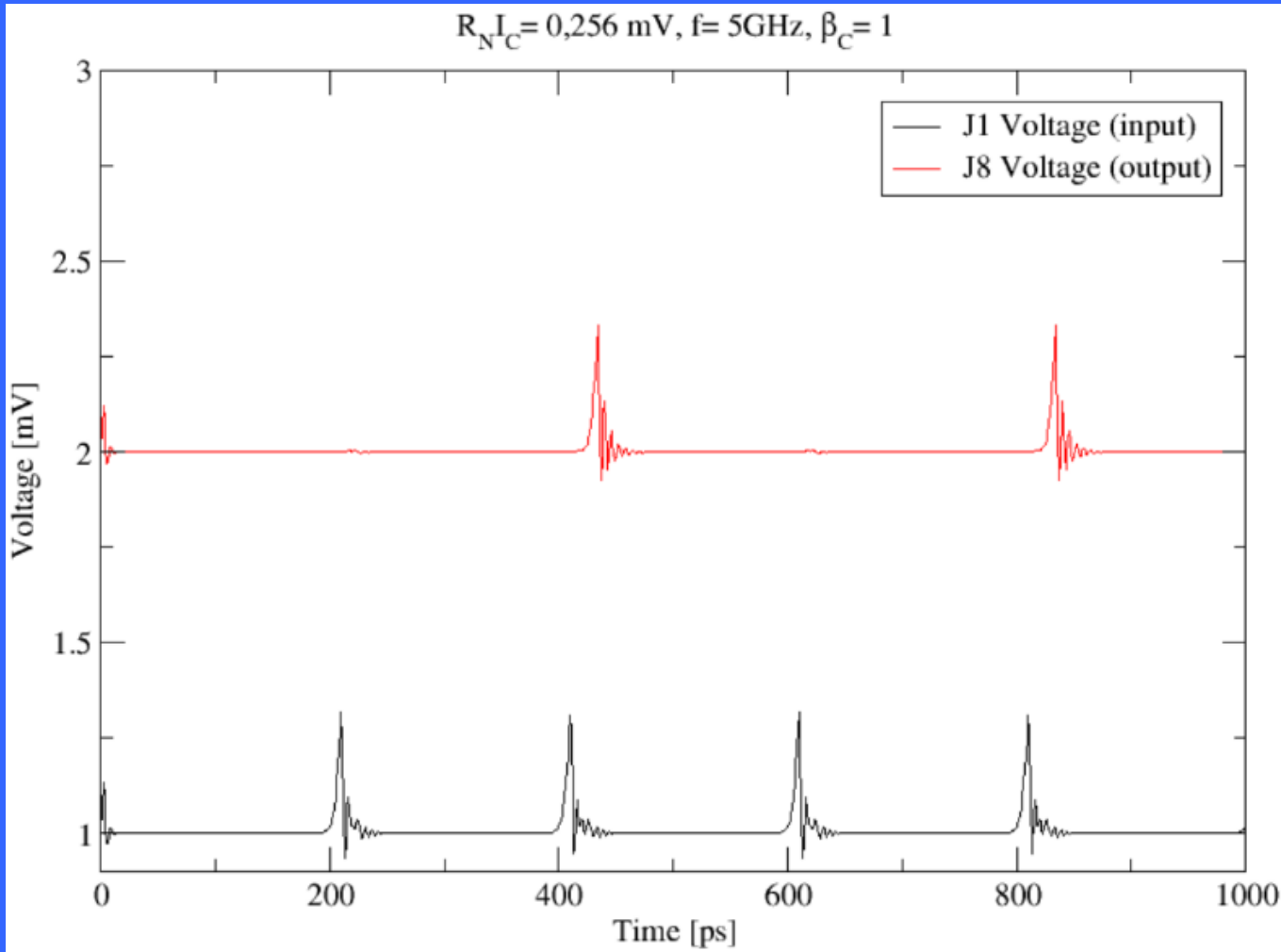
The Toggle Flip Flop (TFF) cell delivers an SFQ output pulse once every two SFQ pulses sent to its input.

For an SFQ clock signal at a given frequency, the output pulse train is an SFQ clock at half-frequency.

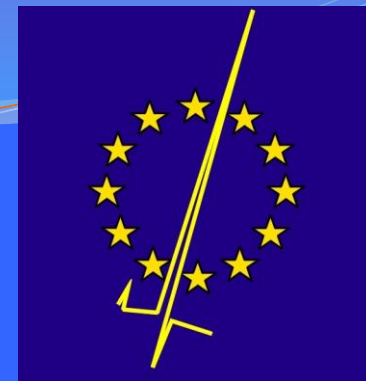
The Toggle Flip-Flop cell



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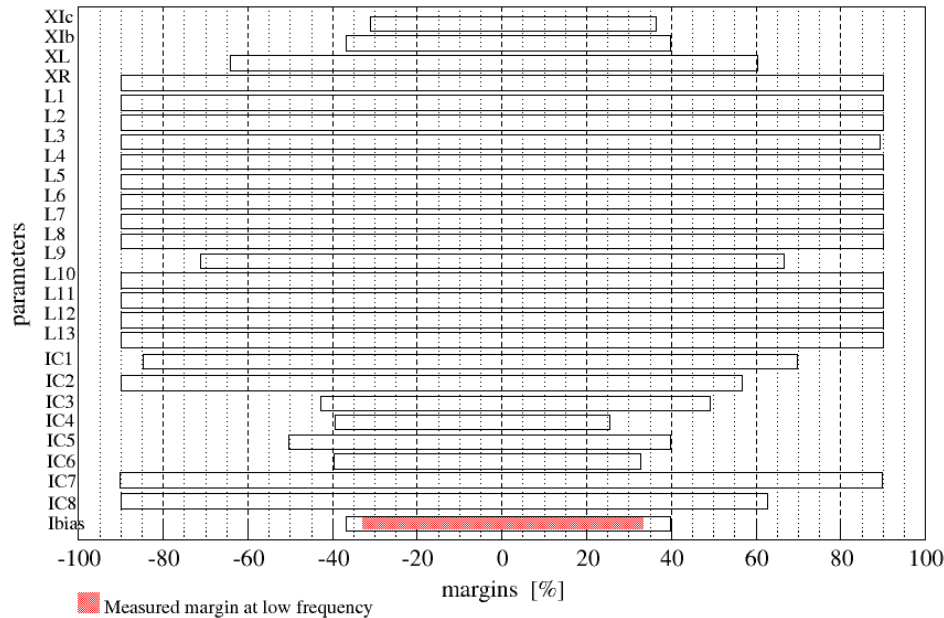


The FLUXONICS Toggle Flip-Flop cell margins and yield

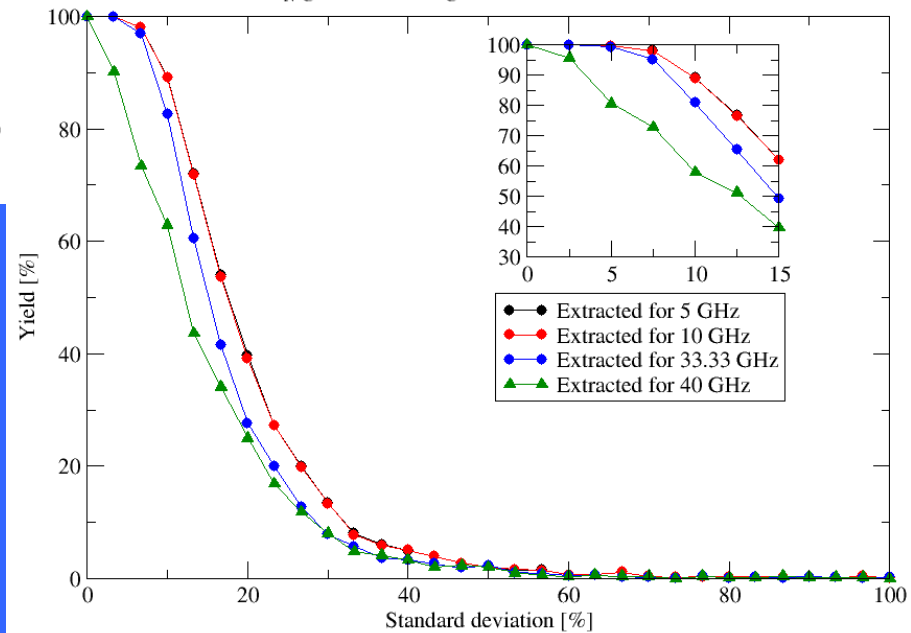


www.FLUXONICS.eu

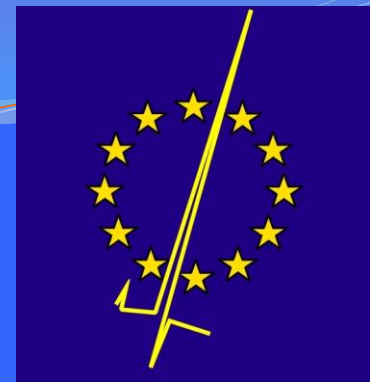
$R_N I_C = 0.256 \text{ mV}$, $f = 5 \text{ GHz}$, $\beta_C = 1$



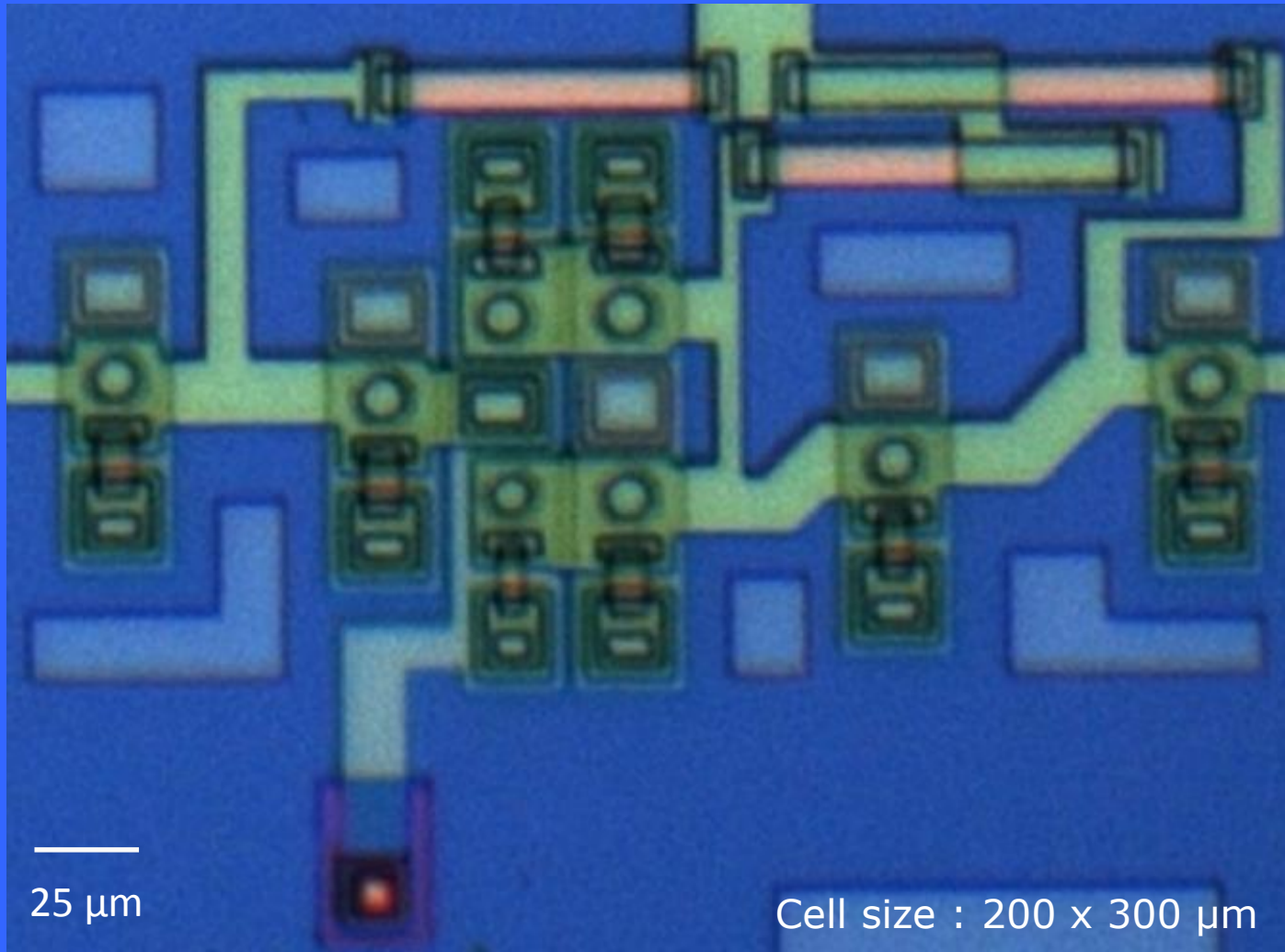
$R_N I_C = 0.256 \text{ mV}$, $\beta_C = 1$, 1000 attempts per point



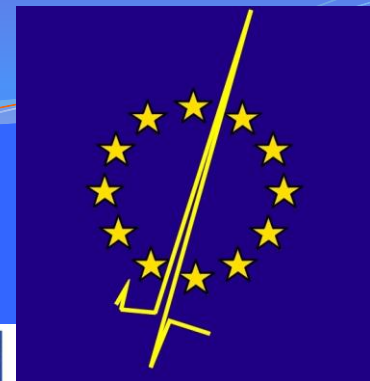
Picture of Toggle Flip-Flop cell



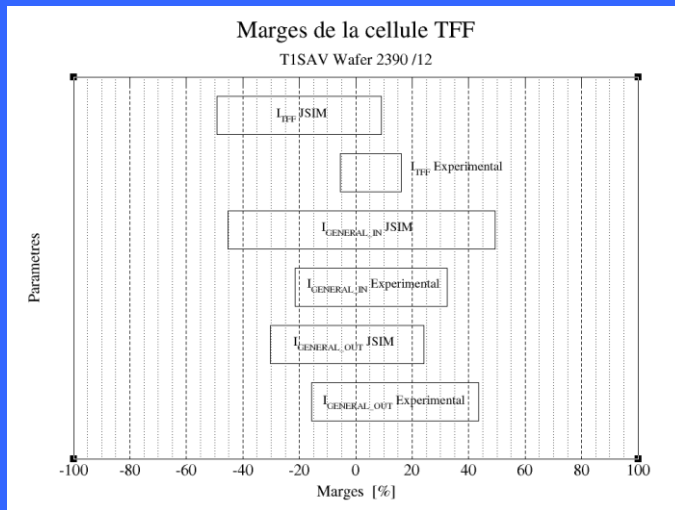
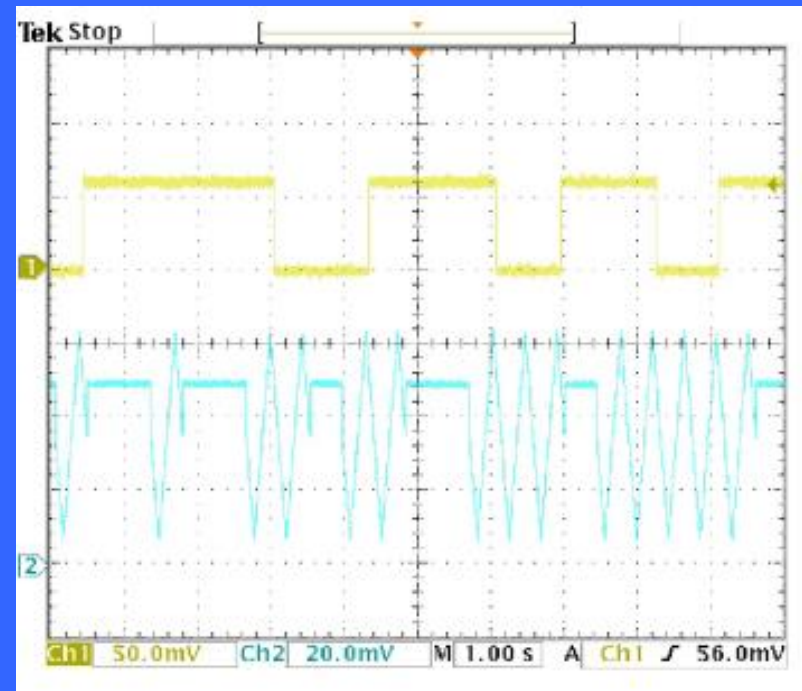
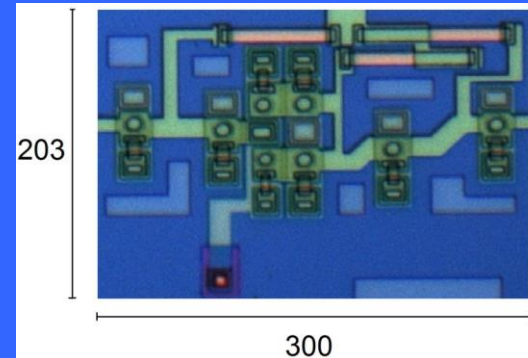
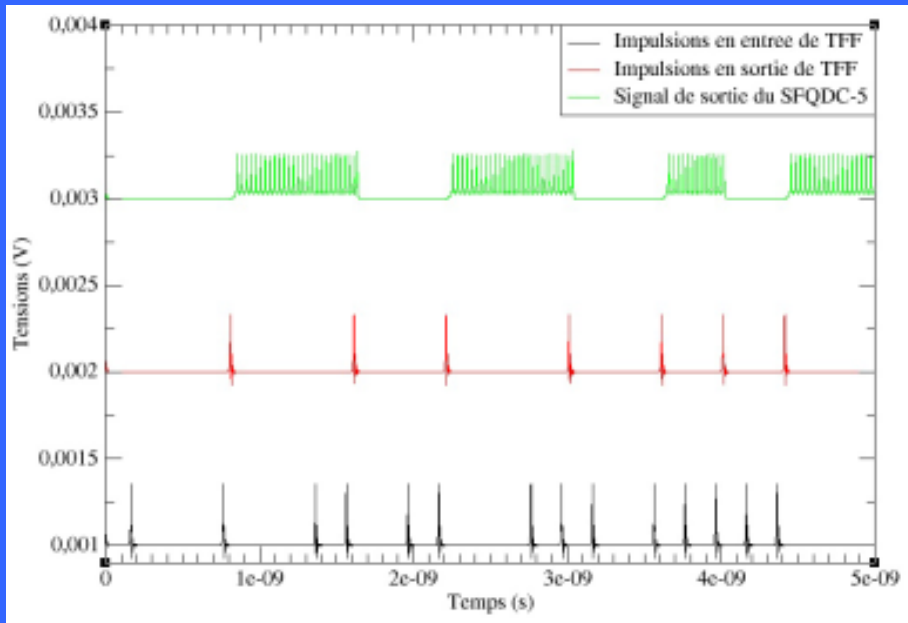
www.FLUXONICS.eu



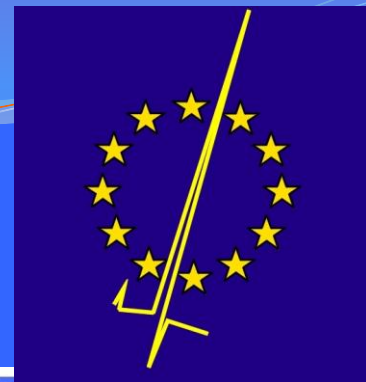
Toggle Flip-Flop experimental results



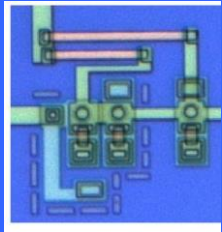
www.FLUXONICS.eu



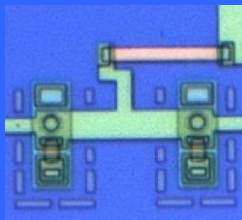
FLUXONICS cell library



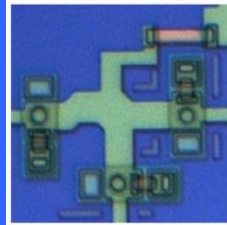
www.FLUXONICS.eu



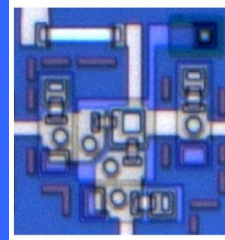
DCSFQ



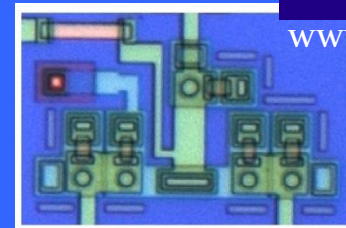
JTL



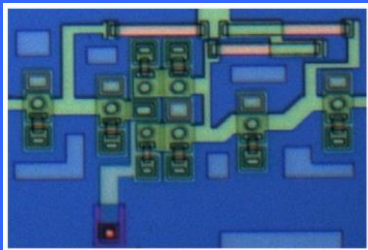
SPLITTER



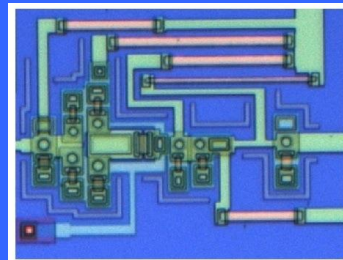
MERGER-1



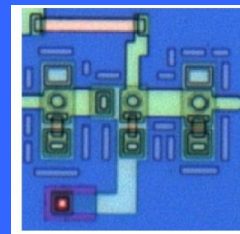
MERGER-2



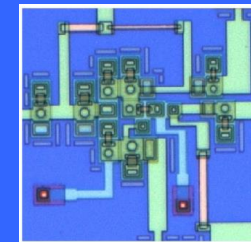
TFF



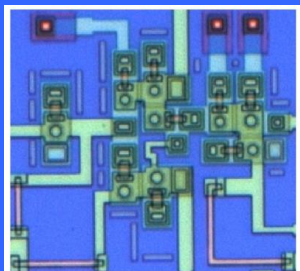
SFQDC



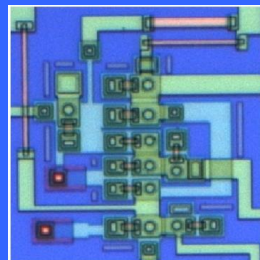
BUFFERJTL



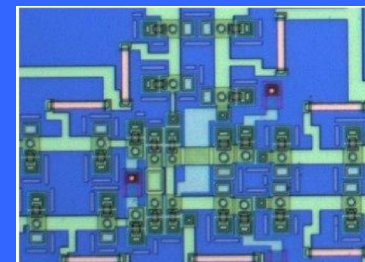
DFFC



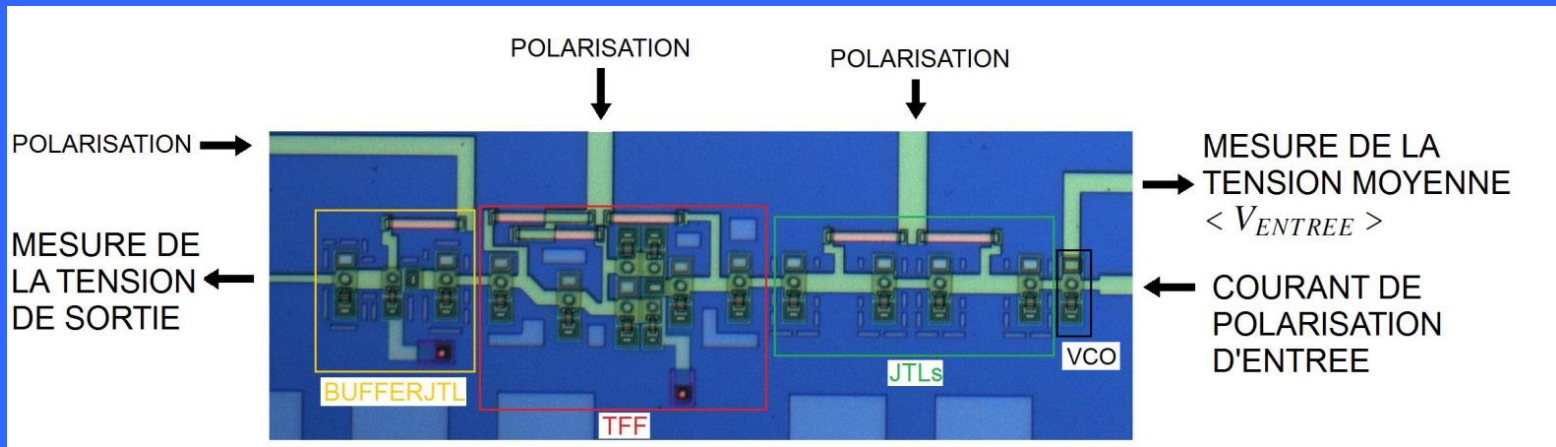
TFFC-A



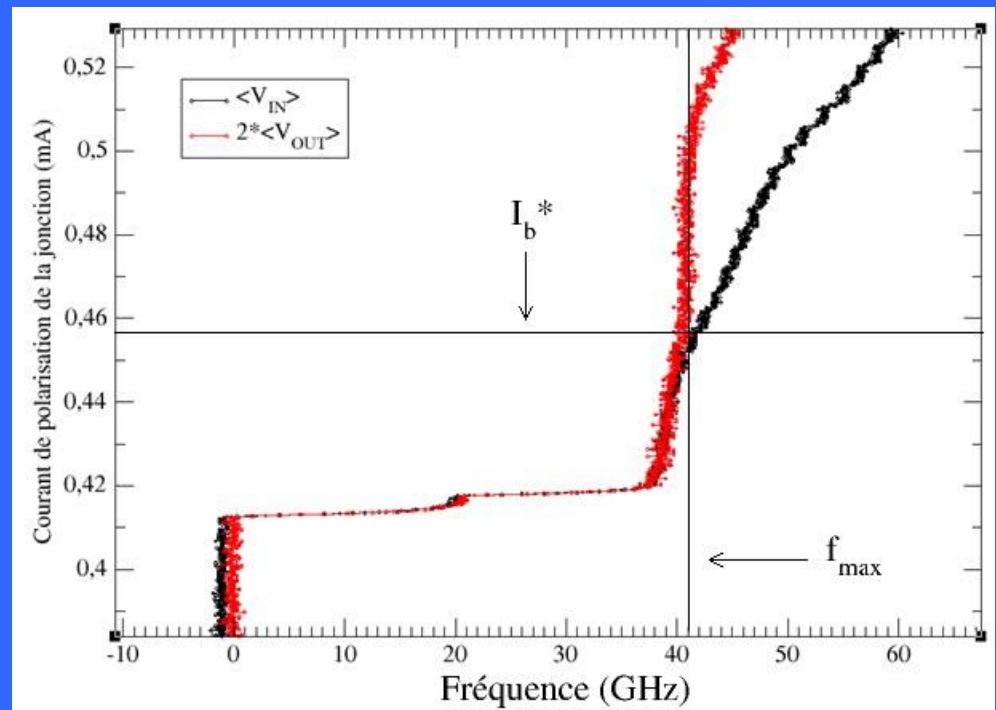
TFFC-B



NDRO



The physics of the Josephson junction gives easy access to the frequency of oscillations



Performances & applications of RSFQ logic

Performances:

- clock frequencies in the 30-110 GHz range (state-of-the-art)
- ultimate clock frequencies up to 770 GHz : demonstrated on simple circuit
- clock frequency objective for the next decade: 160-300 GHz
- very low consumption with new eSFQ and eRSFQ concepts

Applications:

Telecommunication domain:

- analog-to-digital converters
- routers
- base-station of mobile phones

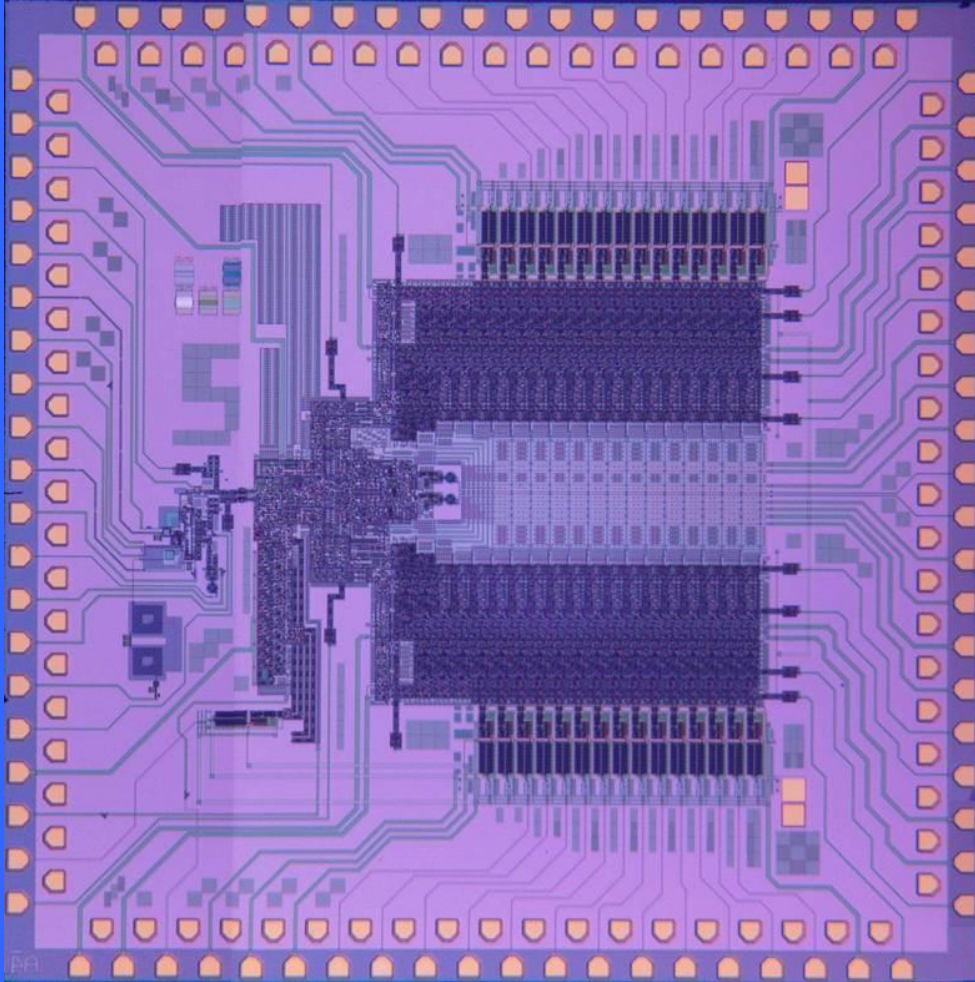
Security & intelligence:

- analog-to-digital converters
- super-computers
- software-defined radio - SDR

Science:

- super-computers
- astronomy: signal processing of imagers
- geophysics: study of Earthquakes, geophysical prospection
- (bio)-medical: encephalo- & cardio- magnetography
- archeology

Analog-to-Digital Converters



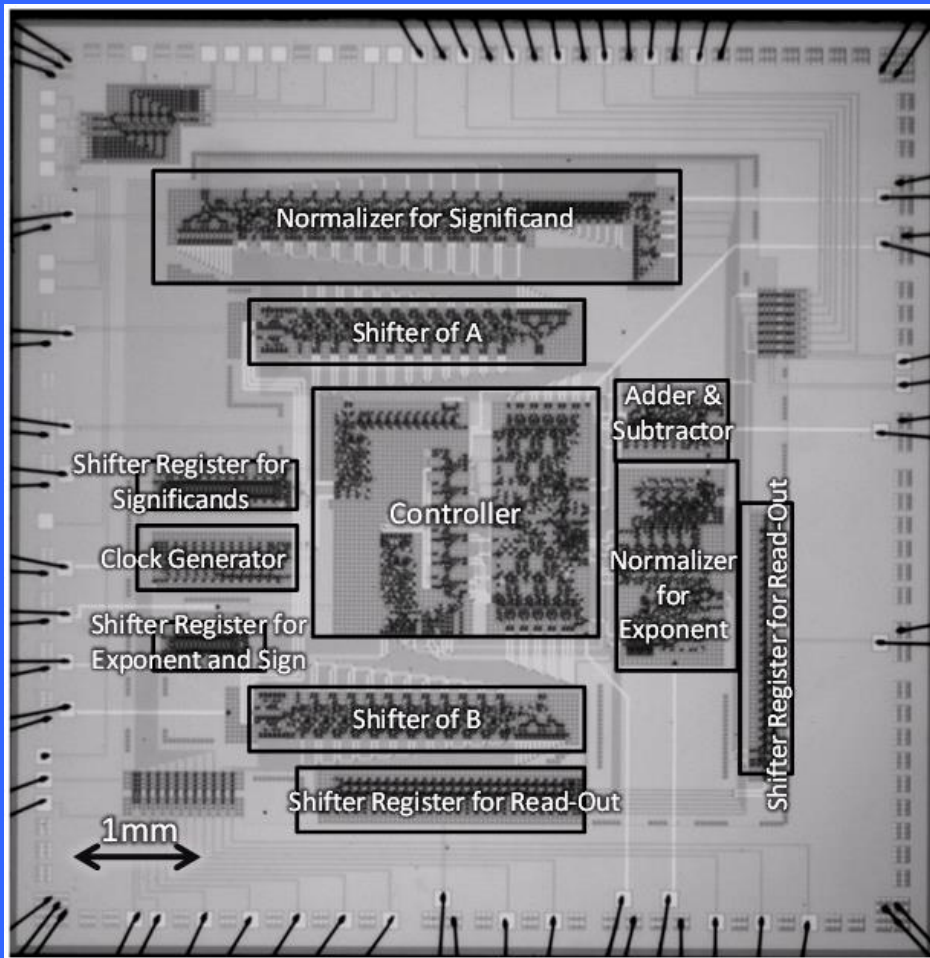
1 cm² chip, fabricated with HYPRES' standard Nb process with $J_c = 4.5 \text{ kA/cm}^2$.

It contains :

- a bandpass delta-sigma ADC,
- a digital channelizer,
- output drivers.

5000 - 10 000 Josephson junctions.

Floating-point units (Japan)



RSFQ half-precision floating-point adder (FPA) successfully demonstrated at 20 GHz.

Circuit size is 5.9 mm × 5.7 mm.

10224 Josephson junctions.

Performance is 1.67 GFLOPS.

Total power consumption is 3.5 mW.

Superconducting digital electronics integrated systems



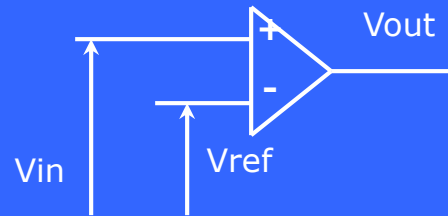
Complete cryocooled digital-RF receiver system prototype, assembled in a standard 1.8-meter tall 0.5-meter wide equipment rack.

Using the modular packaging approach, the system can currently host variety of chips.

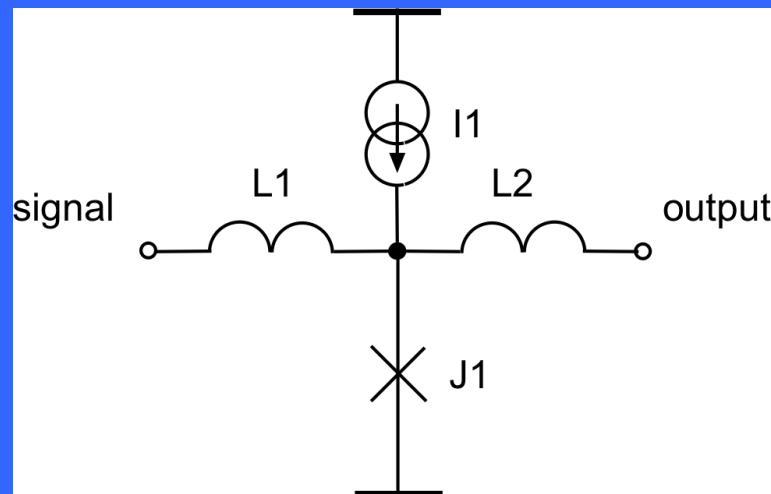
The system includes a two-stage 4-K Gifford-McMahon cryocooler manufactured by Sumitomo, two sets of interface amplifiers for connecting chip outputs to an FPGA board (placed behind the vacuum enclosure, on the metal tray) for further digital processing and computer interface. The system also includes a current source and a temperature controller.

An introduction to comparators

- **Semiconductor technology:** comparators based on operational amps have specifications that depend weakly on environment

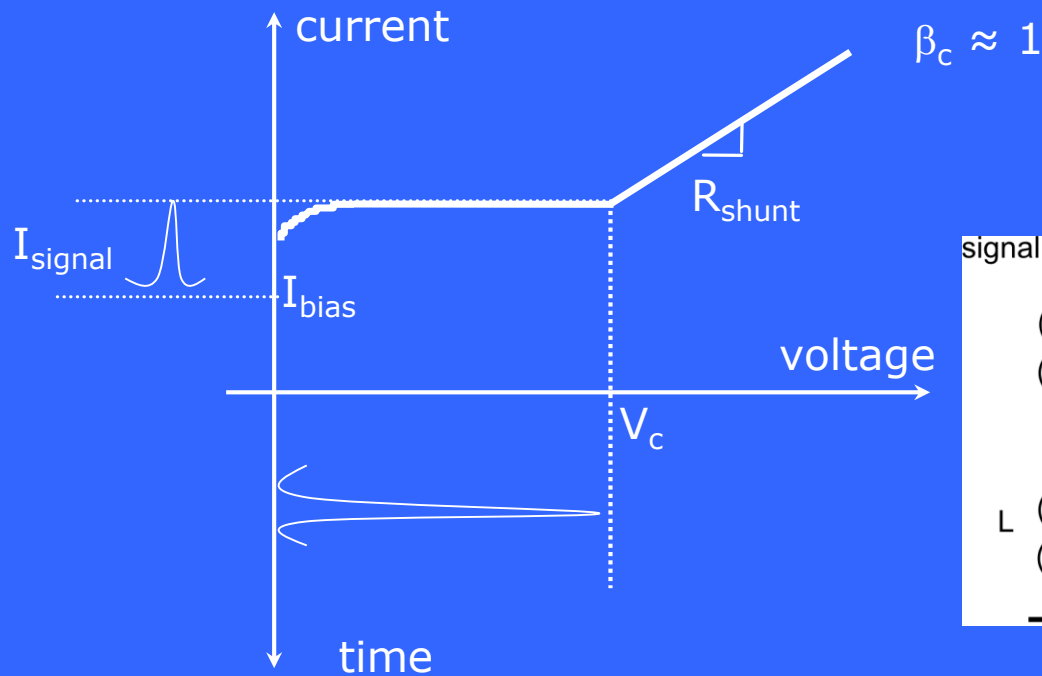


- **Superconductor technology:** comparators are based on Josephson junctions whose high non-linearity involves a design that is fully environment-dependent



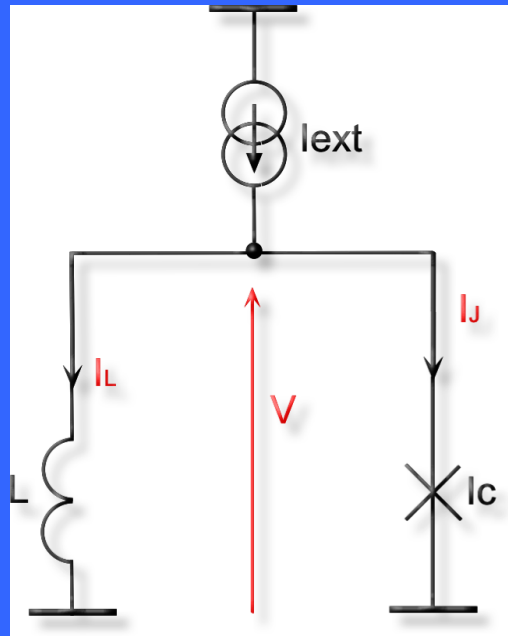
Analog-to-digital conversion with Josephson junctions

When Josephson junctions are shunted to be non-hysteretic and faster, digital information is stored in the magnetic flux quantum and requires a superconducting loop to be generated.



- Digital signal is based on two states, for a given time interval:
 - '0' : no pulse
 - '1' : one SFQ pulse
- Much faster than switching logic if shunt resistance is correctly chosen

The DC-to-SFQ interface used as a comparator

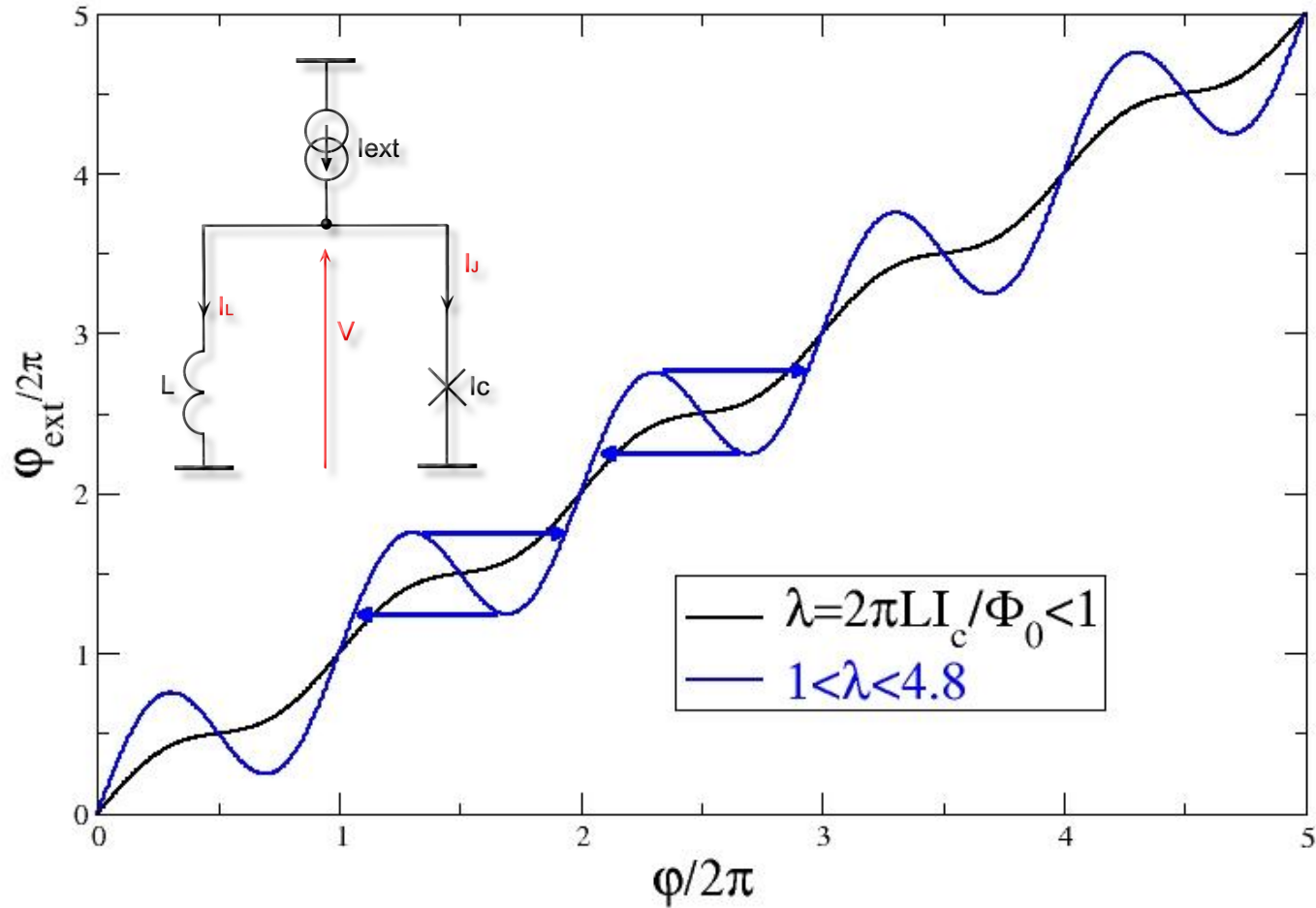


- The Josephson junction switches for specific values of I_{ext} ;
- It can be used to know I_{ext} at the switching instants;
- If the temporal form of I_{ext} is complex, the pulses are not equally spaced in time and the post-processing of digital data is complex.

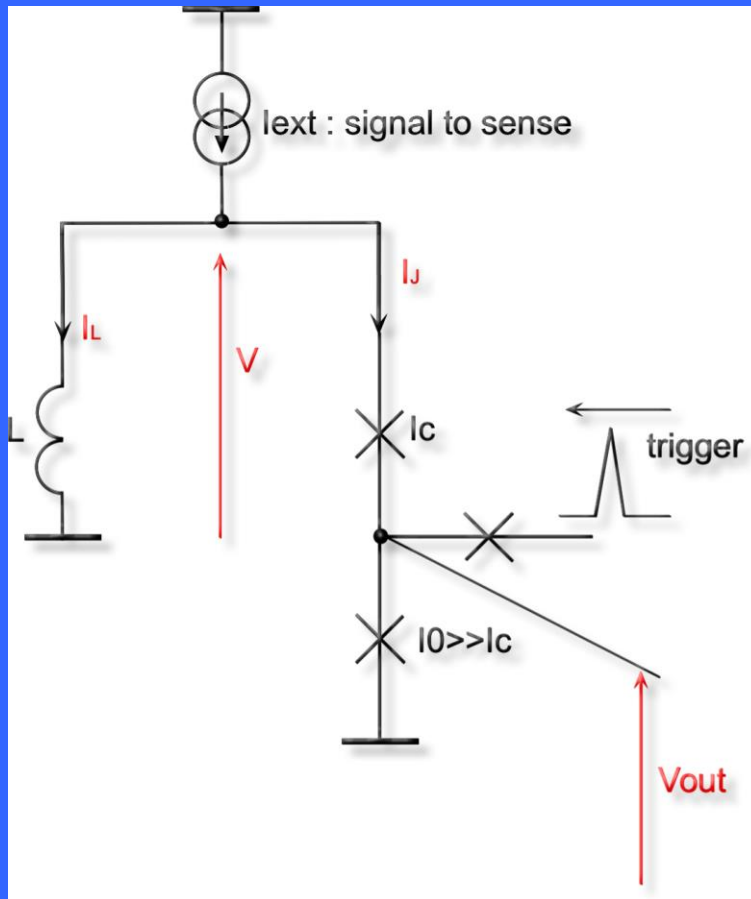
- A pulse added to the signal to sense, and chosen to force triggering of the Josephson junction at a regular rate, transforms the DC-to-SFQ converter into a comparator.
- Then the generated pulse needs to be measured and processed.

The DC-to-SFQ interface used as a comparator

Driving a DC-to-SFQ converter

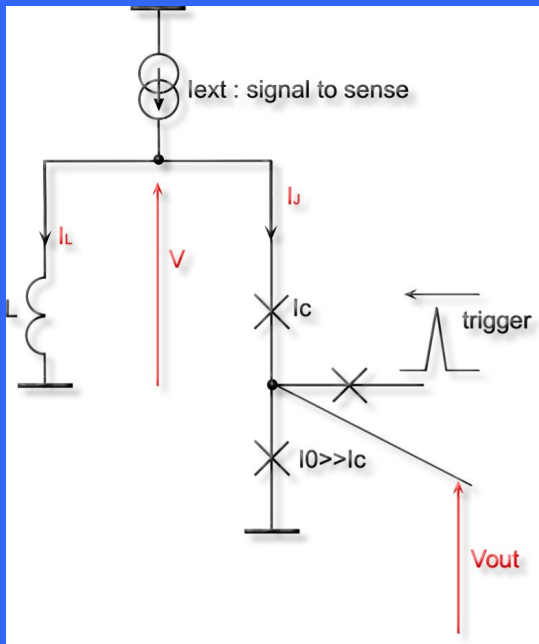


The DC-to-SFQ interface used as a QOJ comparator

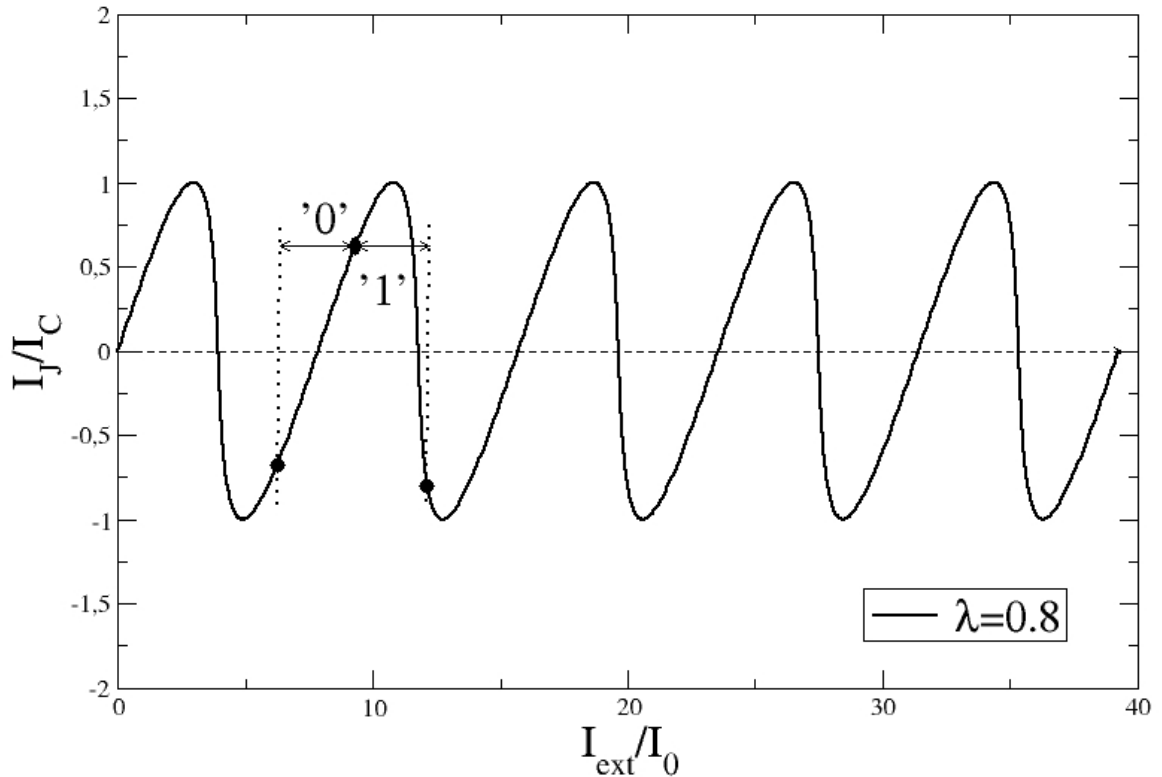


- The second junction is chosen to have a critical current much higher than the one of the comparator junction
 - The device is a **quasi-one-junction SQUID (QOJS)**: Ko & Van Duzer, 1988
 - It is biased so that $P(\text{switching}) = 50\%$ in absence of signal
 - Ko & Van Duzer, 1988
 - Networks of such QOJS made for flash ADCs
-
- 6-bit ADC demonstrated (4 bits at 5 GHz and 3 bits at 10 GHz) : Bradley (1993)

The DC-to-SFQ interface used as a QOJ comparator

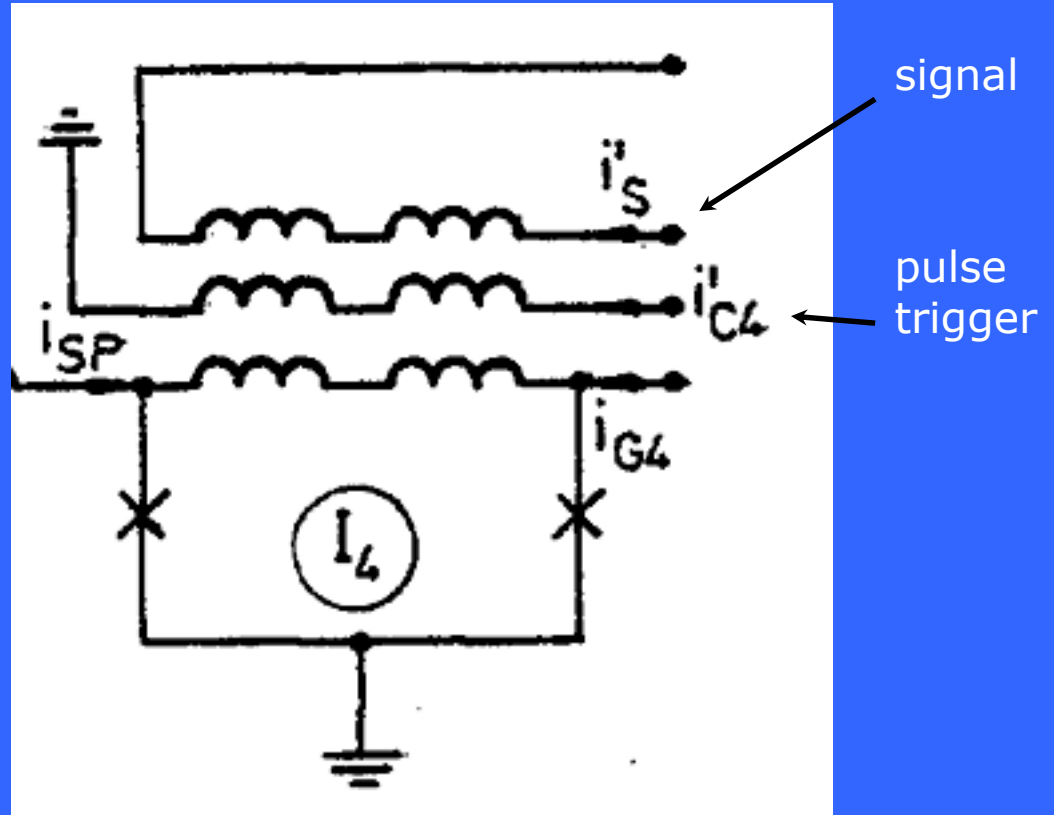
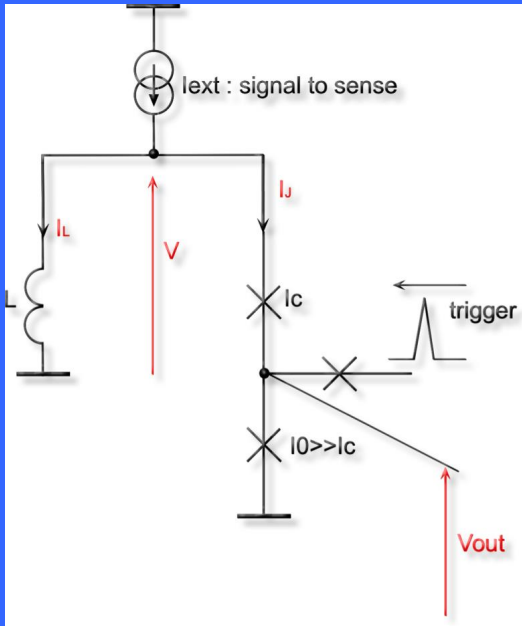


The quasi-one-junction SQUID



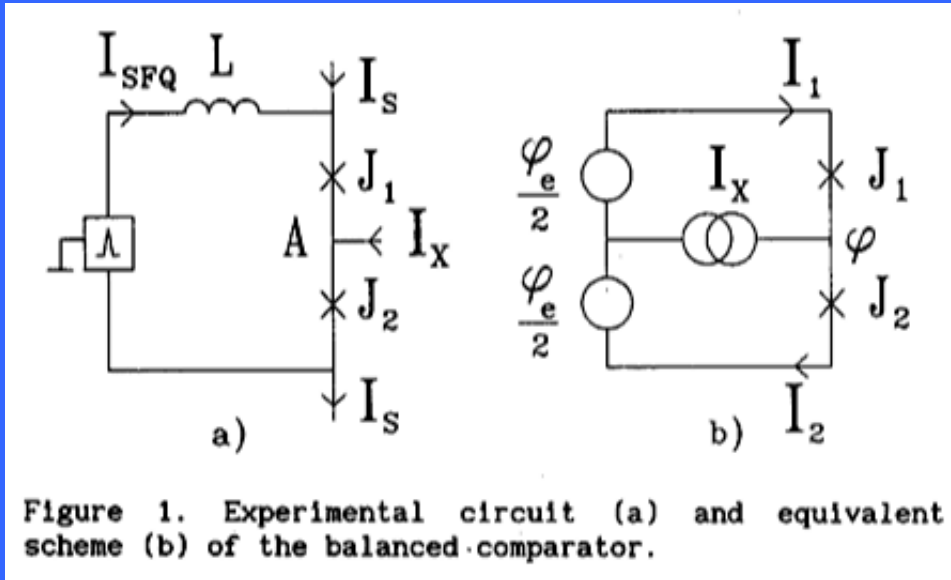
- 6-bit ADC demonstrated (4 bits at 5 GHz and 3 bits at 10 GHz) : Bradley (1993)

The SQUID comparator

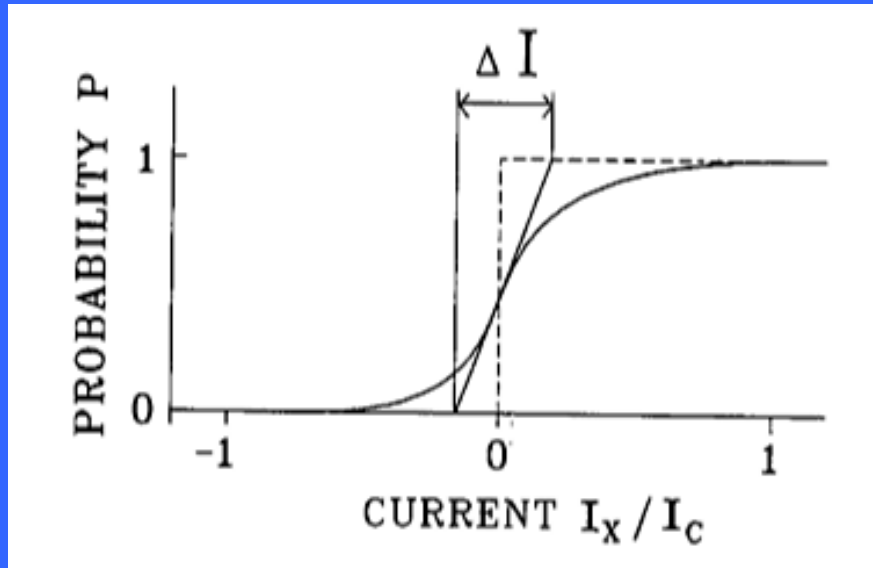
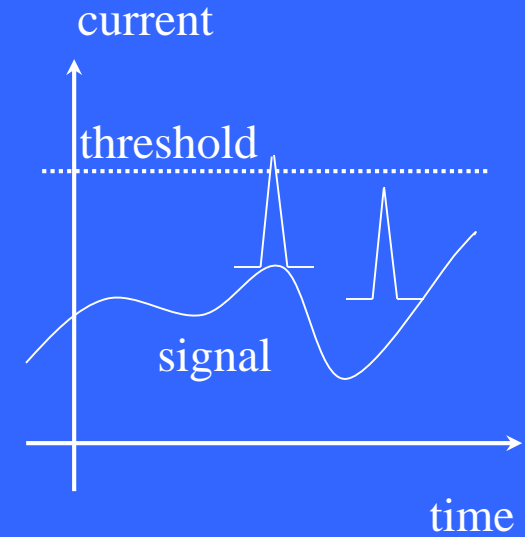


Kratz & Jutzi, 1985

The balanced comparator



Filippov & Kornev, 1991



$$DI = \left| \frac{\partial P}{\partial I} \right|_{I=0}^{-1}$$

Parameters influencing the comparator resolution

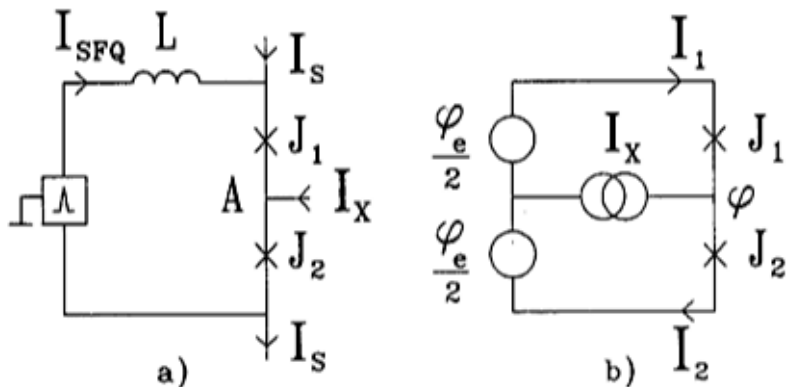
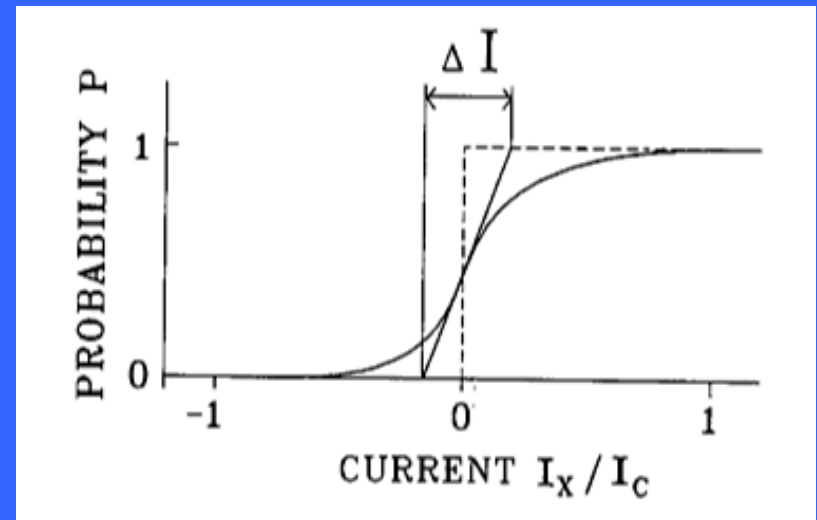


Figure 1. Experimental circuit (a) and equivalent scheme (b) of the balanced comparator.



ΔI depends on:

- noise in the system (<-- temperature)
- triggering pulse shape: time rise,...(<-- frequency of operation)
- JJ parameters (capacitance, McCumber parameter)
- loop inductances (and stray inductances)
- bias current
- environment impedance in a wide frequency range

The balanced comparator resolution

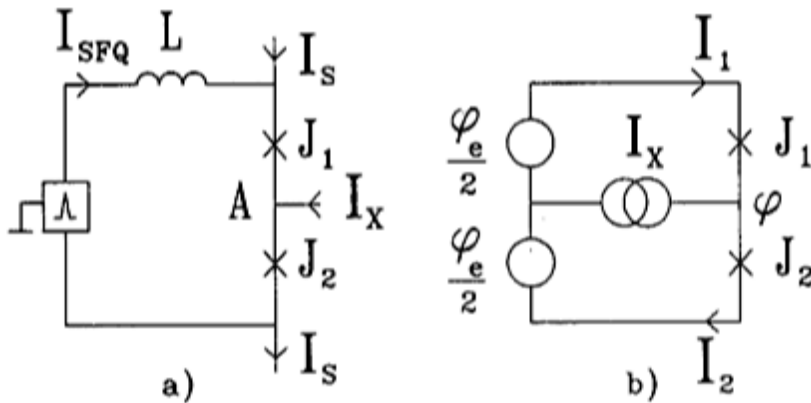
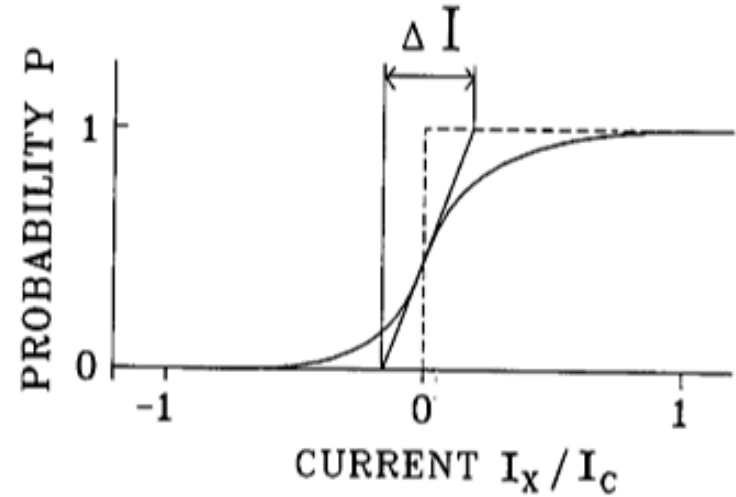


Figure 1. Experimental circuit (a) and equivalent scheme (b) of the balanced comparator.



$$DI \propto I_c^{1/3} I_T^{2/3} \ln \left(a \frac{R_N I_c T}{a} \right)^{-1/3}$$

α is the switching rate

$$I_T = \frac{2ek_B T}{\hbar} = 0.04 \mu A / K$$

The balanced comparator resolution

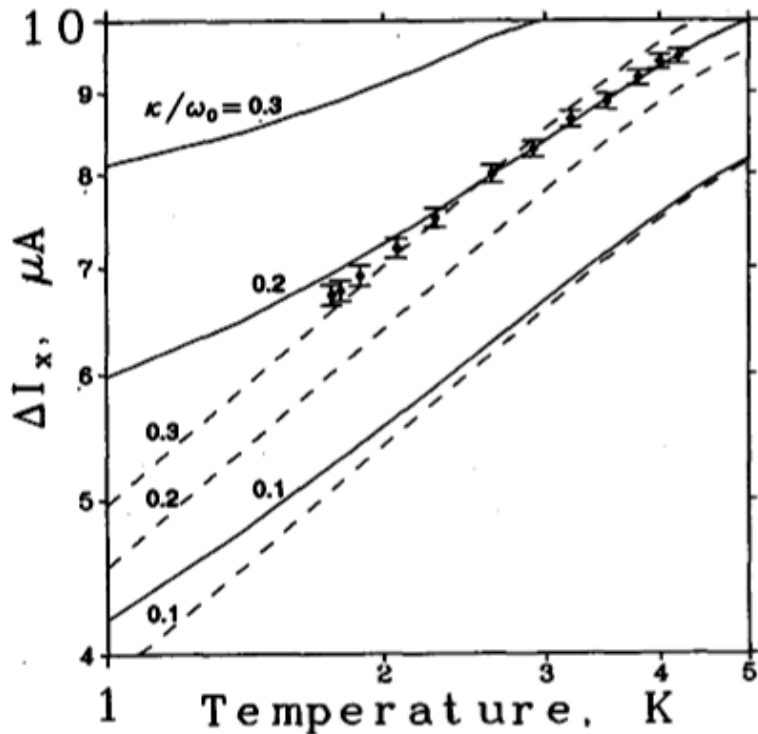


Fig. 4. Width of the switching probability distribution as a function of temperature. Points: experiment for chip# USB99, wafer 2440H, $I_c(4.2K) \approx 145 \mu A$. Solid lines: theory for various values of the ratio κ/ω_0 . Dashed lines: the same for purely thermal fluctuations ($\hbar\omega_0 \ll k_B T$).

Filippov et al, 1995

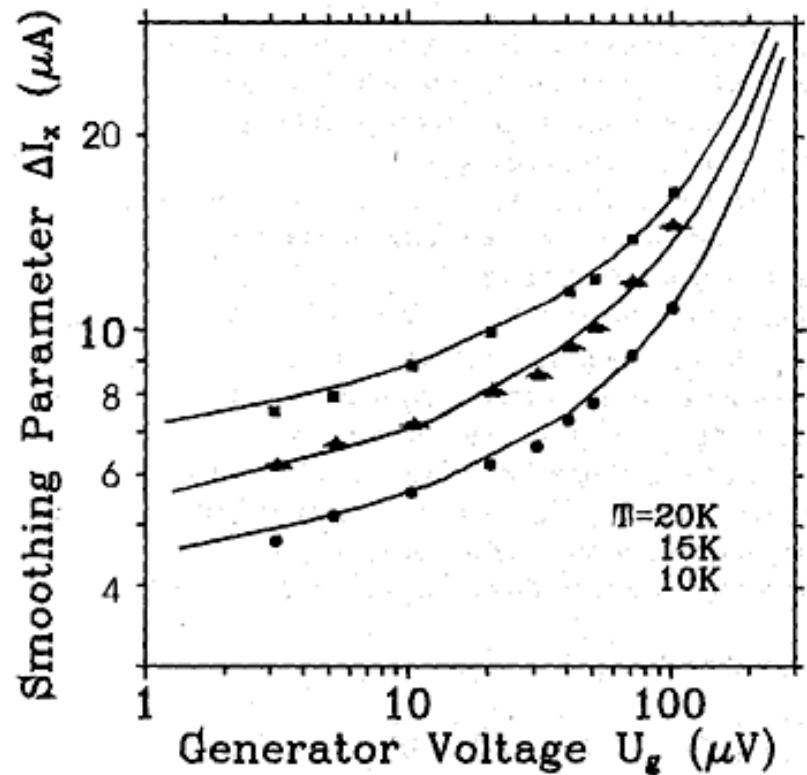


Fig. 5. Dependence of the smoothing parameter ΔI_x on the generator voltage U_g . For each temperature, I_b was adjusted in order to keep the comparator in the WP.

Oelze et al, 1997

The balanced comparator resolution

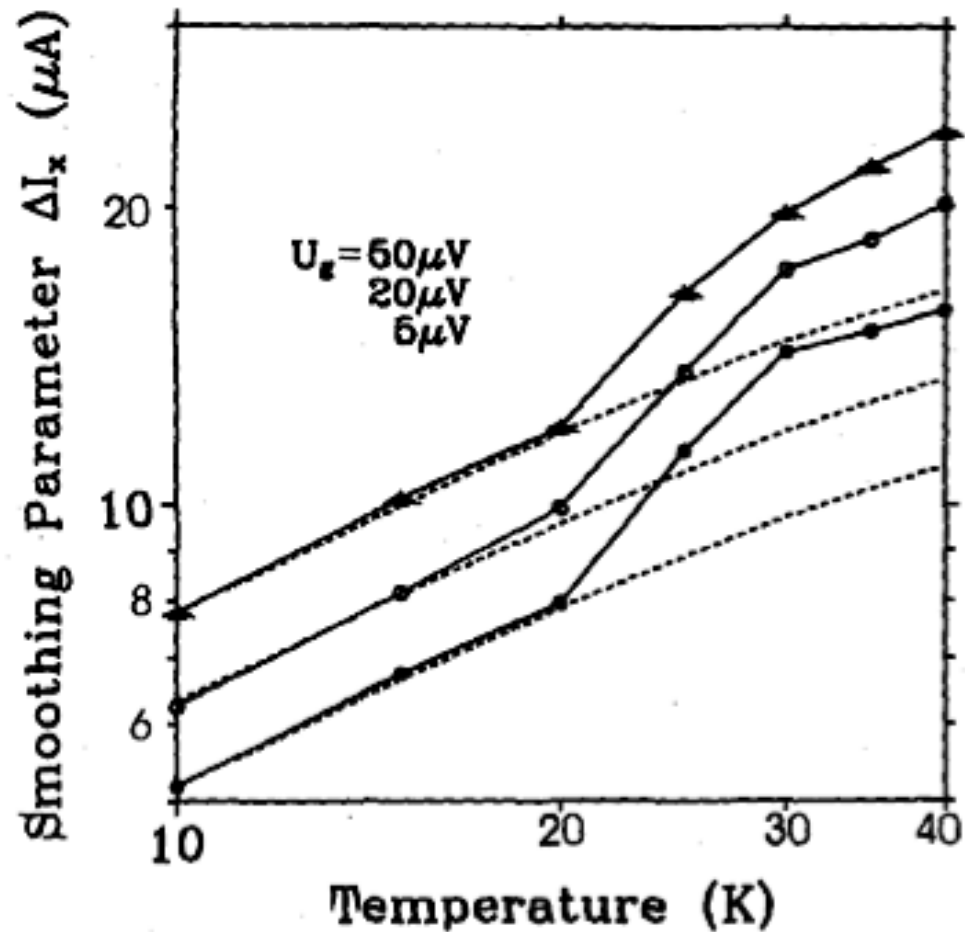


Fig. 6. Temperature dependence of the smoothing parameter; experimental data (solid lines, points) and theoretical results (dashed lines).

The current knowledge on balanced comparators

- The influence of noise, shape of triggering pulse and speed is fully understood, even versus the input signal inductance
- The jitter of the device can be derived from this analysis
- Experiments and theory are in very good agreement regarding noise considerations (no extra noise needs to be added)
- The influence of the sensing impedance (in particular inductance) and of other parasitic elements in the sensing loop is still not totally sorted out (Gordeeva & Pankratov, JAP2008)

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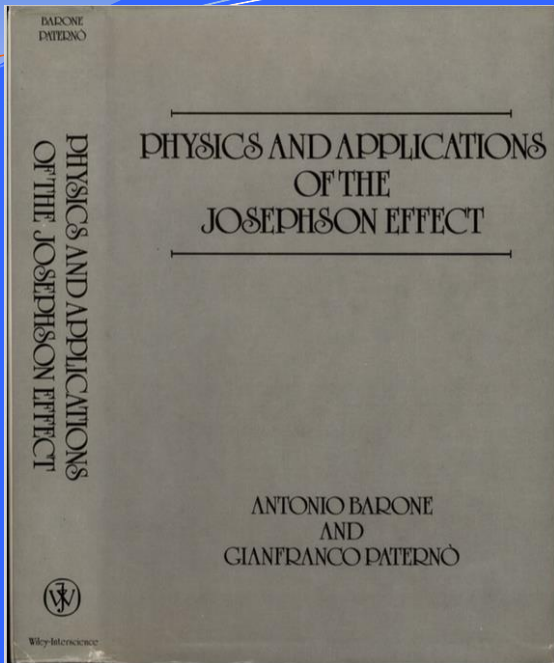
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KONSTANTIN K. LIKHAREV

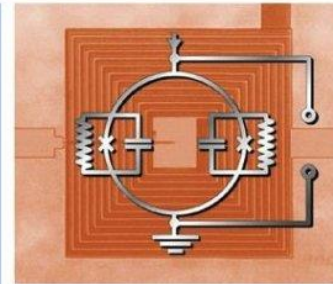
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The SQUID Handbook

Vol. I Fundamentals and Technology of SQUIDS
and SQUID Systems

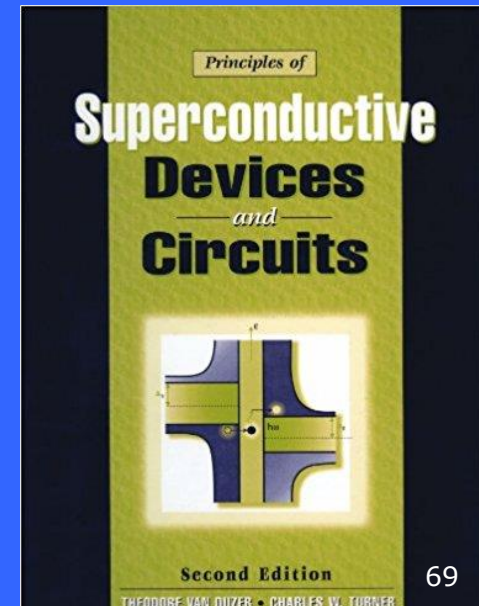
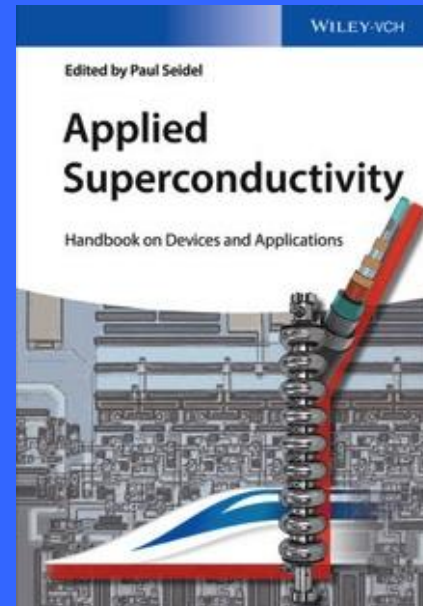
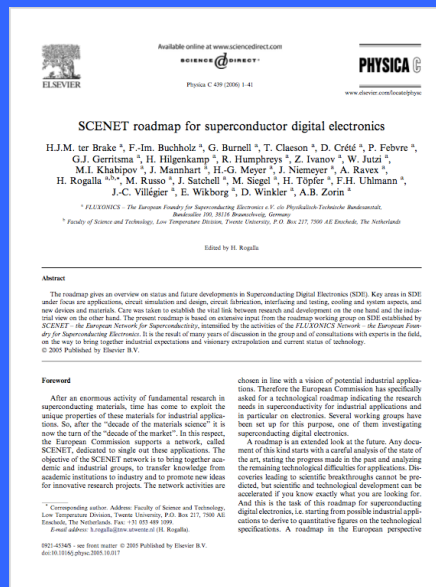
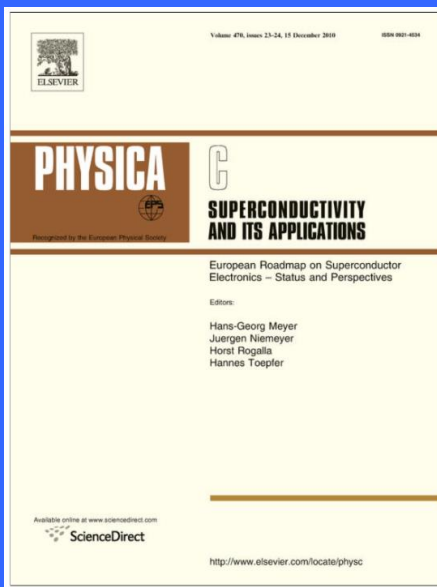
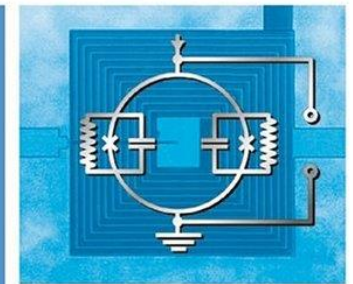


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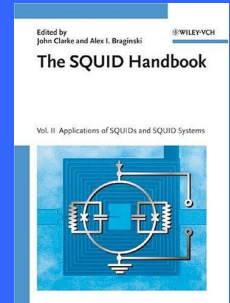
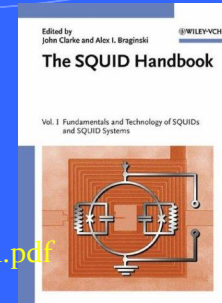
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Thank you for your attention !

phase

Flux jump



Cooper pair

x

Fontaine de Vaucluse - France - March 9, 2013

time