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LHCb vertex locator upgrade: front-end electronics and firmware.

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The LHCb Experiment will be upgraded to a trigger-less system reading out the full detector at 40 MHz event rate with all selection algorithms executed in a CPU farm. The upgraded Vertex Locator (VELO) will be a hybrid pixel detector read out by the "VeloPix" ASIC with on-chip zero-suppression. The upgrade of the LHCb experiment will be installed during the shut-down LS2 of LHC in 2019-2020. It will transform the experiment into a trigger-less system reading out the full detector at 40 MHz event rate. The VELO surrounding the interaction region is used to reconstruct primary and secondary decay vertices and measure the flight distance of long-lived particles. The highest occupancy ASICs will have pixel-hit rates above 900 Mhit/s and produce an output data rate of over 15 Gbit/s, adding up to 1.6 Tbit/s of data for the 41M pixels of the whole VELO.

This poster will present the architecture and design of the VELO on-detector electronics, describing each component and its relation to the LHCb common frame. The main components are: the VeloPix ASIC at 5 mm from the beam in a secondary vacuum tank and exposed to an extremely high inhomogeneous radiation environment, the Opto- and Power Board (OPB) outside of the vacuum, but still in a high radiation environment, the LHCb readout (TELL40) and front-end control (SOL40) boards, placed in a radiation free environment. The whole system is currently being integrated, validated and tested. The results and experience gained from these test will be presented.

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