The VeloPix ASIC test results

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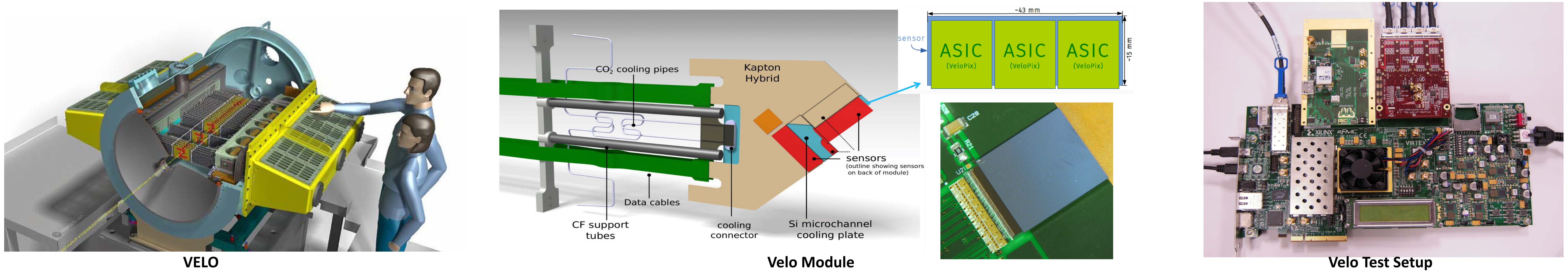
LHCb and VELO

LHCb is a dedicated experiment searching for new physics by studying CP violation and rare decays of b and c quarks. The LHCb silicon vertex detector (VELO) is a crucial component of the experiment. The detector provides precision space points close to the interaction point and thus used to reconstruct b decay vertices, in both the trigger and offline track reconstruction as well as being an important part of the tracking system. In order to match the upgraded LHCb readout system, which aims at a trigger-free read-out of the entire detector at the bunch-crossing rate of 40 MHz, all silicon modules and electronics must be replaced. The upgraded VELO will be a hybrid pixel detector (55x55 um pitch), read out by the VeloPix ASIC derived from the Timepix3. The sensors and ASICs will approach the interaction point to within 5.1 mm and be exposed to a radiation dose of up to 370 Mrad. The hottest ASICs must sustain pixel hit rates of more than 900 Mhits/s and produce an output data rate of over 15 Gbit/s, adding up to 1.6 Tbit/s of data for the whole VELO.



VELO — Velo Module — Velo Test Setup

VeloPix Asic Tests:

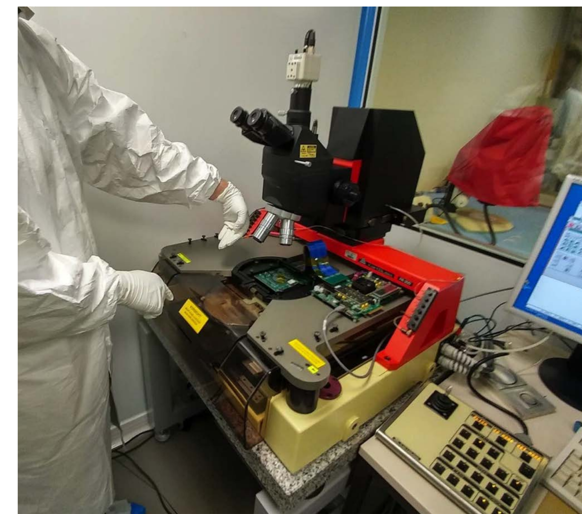
- All digital and analogue functionality has been validated and conforms to specifications.
- Low temperature (-40ºC) operation verified.
- Test with wafer probe card successful.
- TID Test:
  - Test done with X-ray machine at Glasgow university in Dec 2016.
  - Irradiated up to 400 Mrad.
  - No change in digital power consumption.
  - No drift in analogue parameters: Pixel thresholds, noise and global DACs remain stable.
- Beam Test:
  - Done in Fermilab.
  - 5 Plane VeloPix telescope.
  - Rates up to 300 Mtracks/s.
- Timewalk studies.
- SEE Test:
  - 4 sesions at HIF in Louvain-Le-Neuve.
  - Aims was to determine cross-section for single event upsets (bit-flips).
  - Shoot heavy ions of various type / angles.
  - Found some issues:
    - Single Event Latch-up (SEL):
      - It is a (local) short circuit on the power lines. 30 mA current rise per SEL.
      - Recovery is only possible by power cycling the chip.
      - Occurs only in pixel matrix (use of custom high density library). Not in the periphery (use of standard cell library). it prevents read back of data from the internal shift register (e.g. read of config settings)
      - Temperature dependant. Not occurring below -10ºC.
      - SEL is due to high n-well and p-substrate resistance.
      - SEL confirmed by injection of laser light at Montpellier facility.

      Solution: n-well and substrate contacts need to be placed closer to P+ and N+ implants of CMOS.
    - Large cross-section for the SLVS receivers:
      - Covered matrix to get rid of SEL. Then we observed frequent resets of the chip.
      - Note, the distribution and logic of the reset signals is triplicate.
      - But there is only one line receiver, and this happens to have a quite large cross section -> gives single event transients.

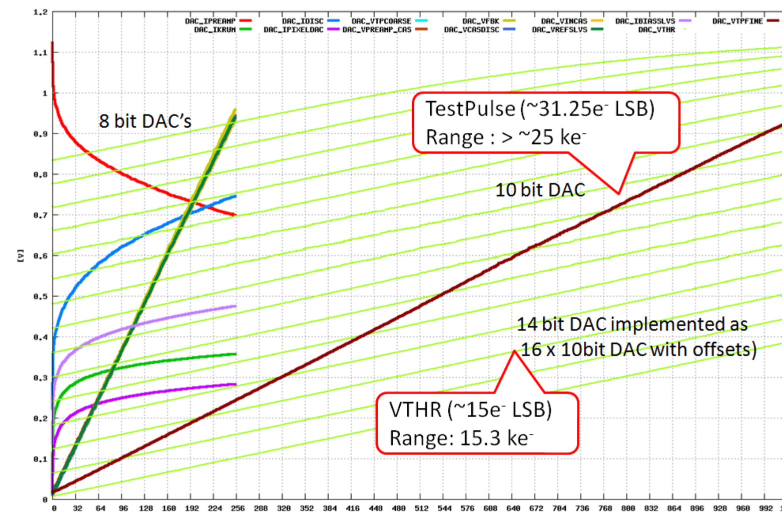
      Solution: Triplicate the SLVS reset receiver and on other ECS / TFC signals.
    - Few small design flaws.
- High Speed Test:
  - Excessive jitter on GWT due to the too much cycle-to-cycle period variation of the internal 320MHz.
  - Rate can be lowered (to almost zero) by tuning an internal clock phase.
  - Origin understood as Vcc & GND bouncing

  Solutions:
  - ***Add extra on-chip decoupling.***
  - ***Splitting of internal supplies in ePLL***
  - ***Shorter bond wires and add external decoupling***
  - ***Smaller, slower, clock buffers***
    - ***Smaller current peaks, and spread in time***
    - ***Small penalty in clock skew, hence timewalk)***

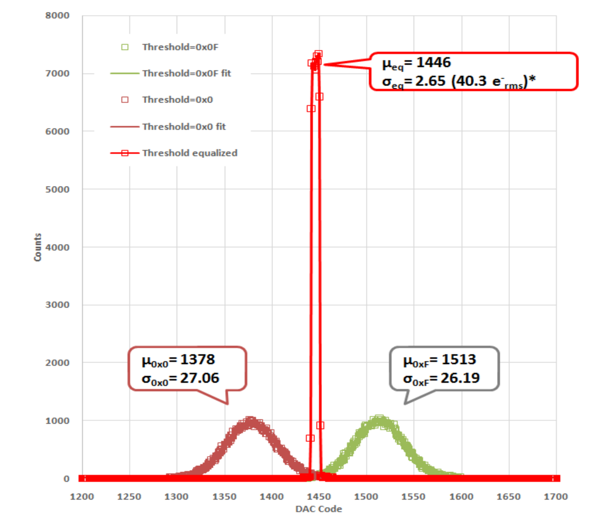
Wafer Probe



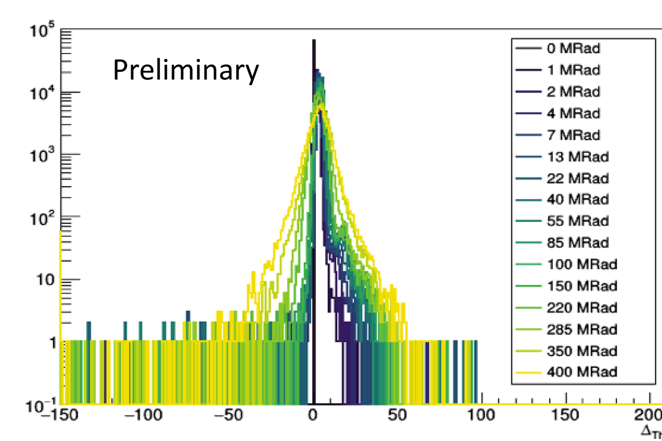
DAC´s



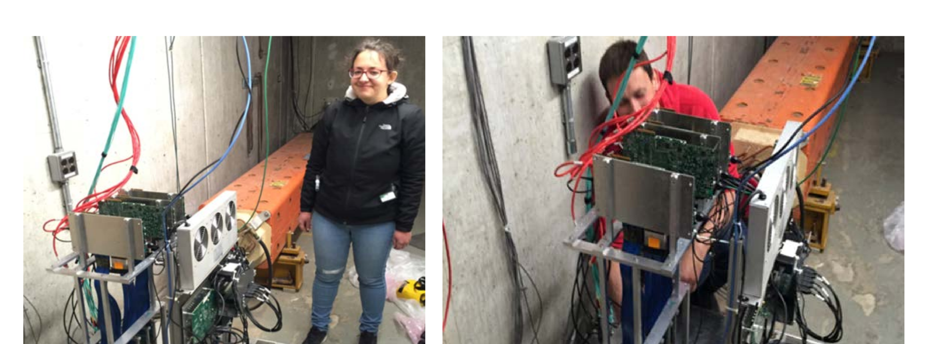
Equalization

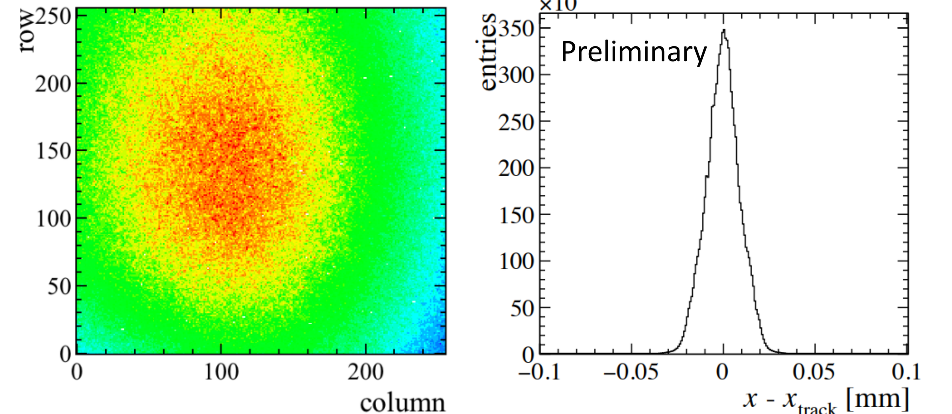


TID Test

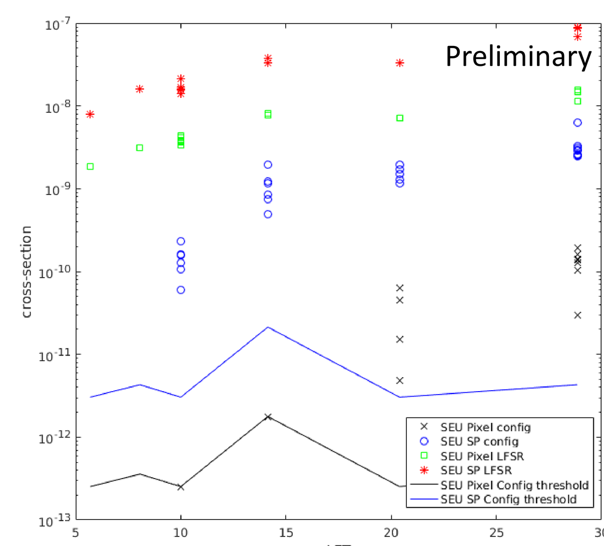


Beam Test

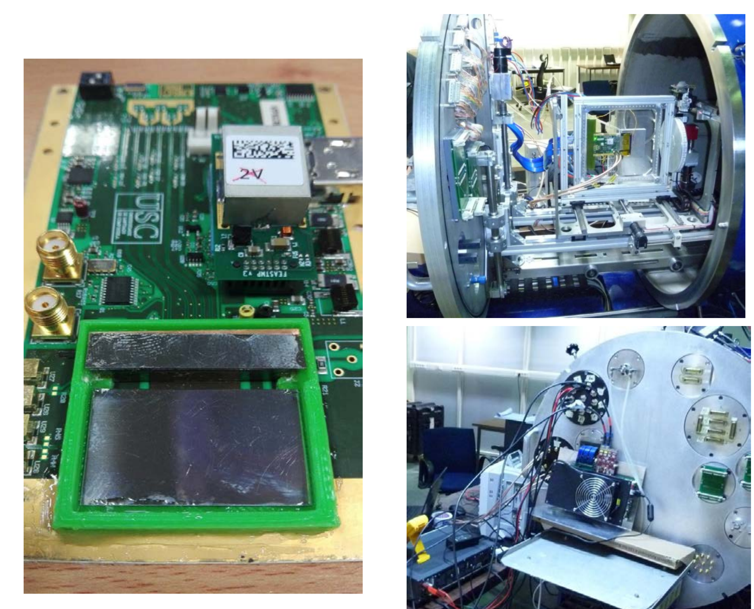


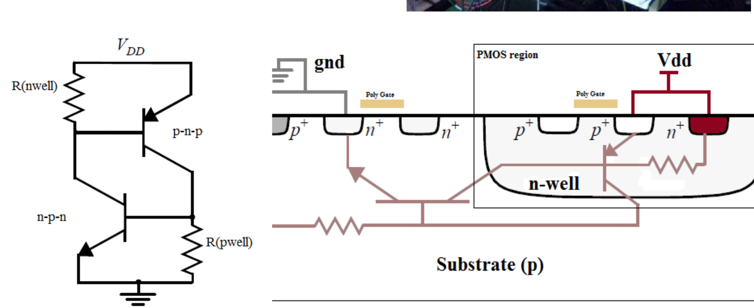


SEU Cross-section

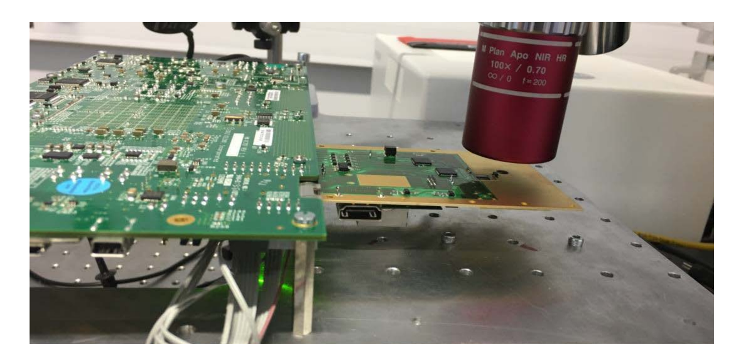


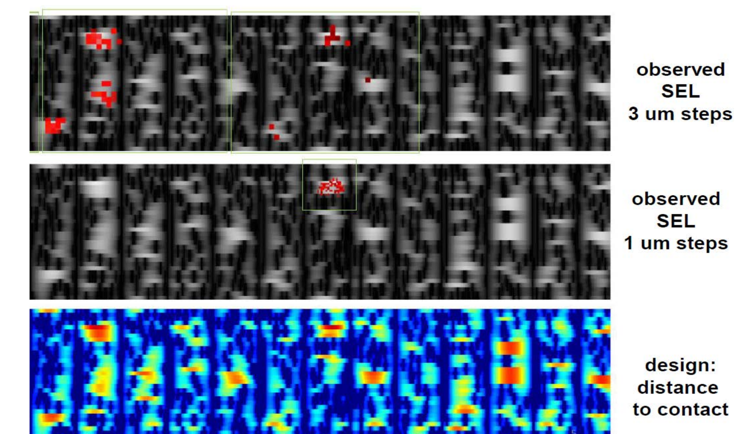
SEE Louvain-Le-Neuve

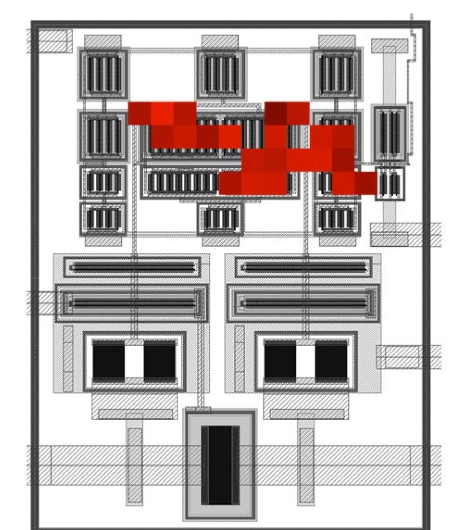




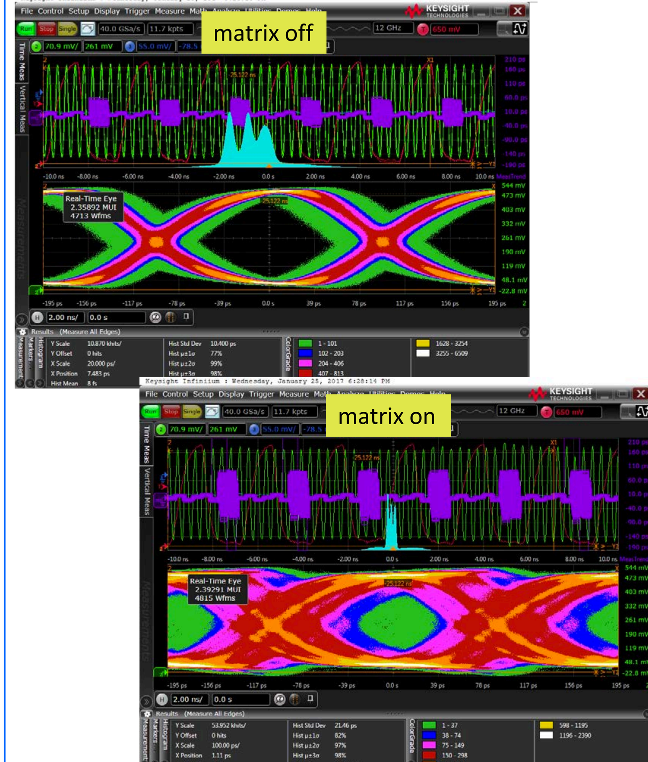
Montpellier laser facility







High Speed Test



VERTEX/2017

GOBIERNO DE ESPAÑA — MINISTERIO DE ECONOMÍA Y COMPETITIVIDAD

Research proyect: “DESAFIOS PRESENTES Y FUTUROS DEL EXPERIMENTO LHCB DEL CERN”. FPA2014-57896-C4-1-R.