VERTEX/2017

THE NA62 GIGATRACKER

FROM SILICON MICROCHANNEL COOLING PLATES TO TRACKING DETECTORS

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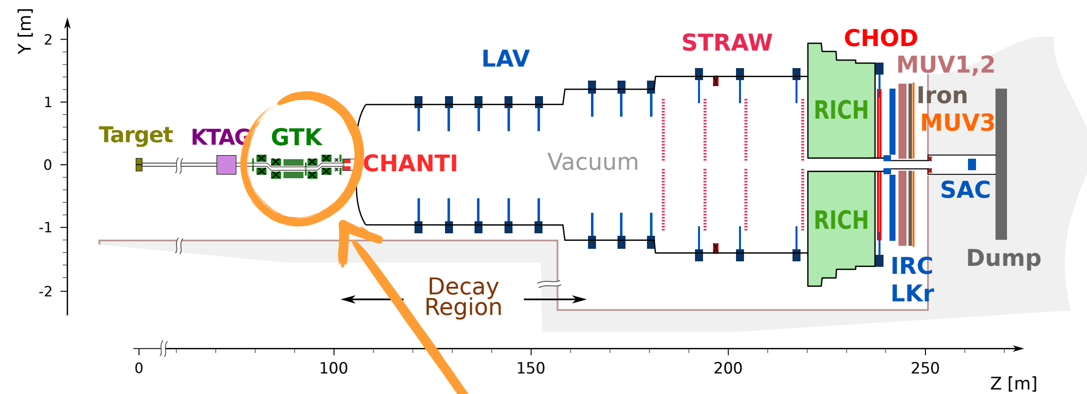
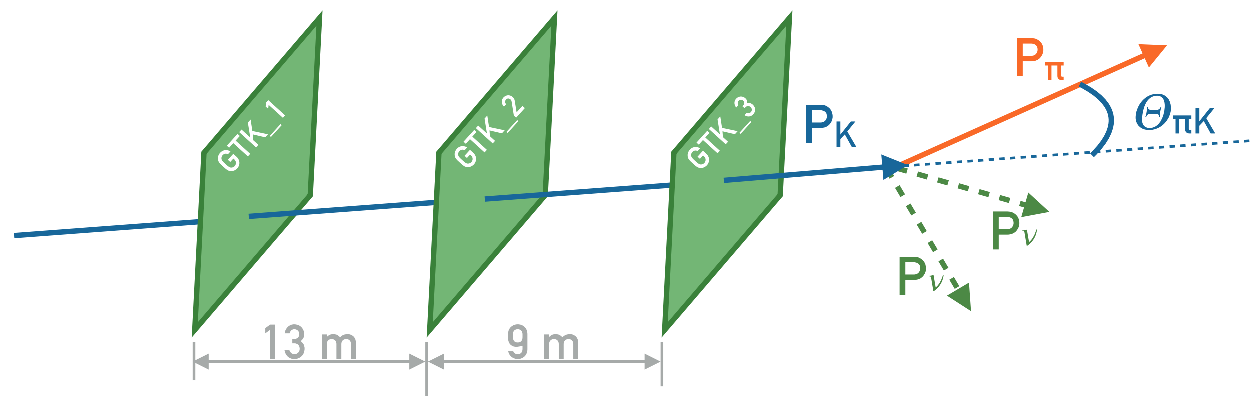
CERN

The NA62 GigaTracKer





- NA62 aims at investigating an extremely rare kaon decay $K^{+} \longrightarrow \pi^{+}\nu\bar{\nu}$ in the North Area of the CERN SPS.
- The GTK is located inside the vacuum pipe right before the K decay region.
- It determines the momentum and the direction of the K entering the NA62 experiment with a time resolution of ~100 ps.

Talk by Ernesto Migliore on Thursday morning.

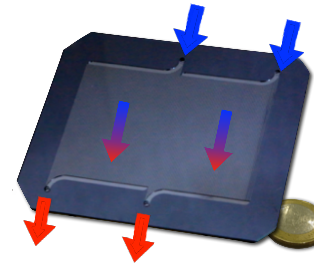
Insertion and extraction in the beam vacuum line

- At nominal beam intensity the detectors are exposed to a fluence corresponding to 4×10^{14} n_{eq} /cm^2 in one year (200 days) of data taking.
- In order to minimise radiation-induced damages, the detectors are operated at approximately -15ºC in vacuum (~10^{-6} mbar).
- Detectors have to be replaced every 100 days.
- The detector mechanics has been designed such that detectors can be replaced rapidly during one of the regular short accelerator stops (<0.5 day intervention).

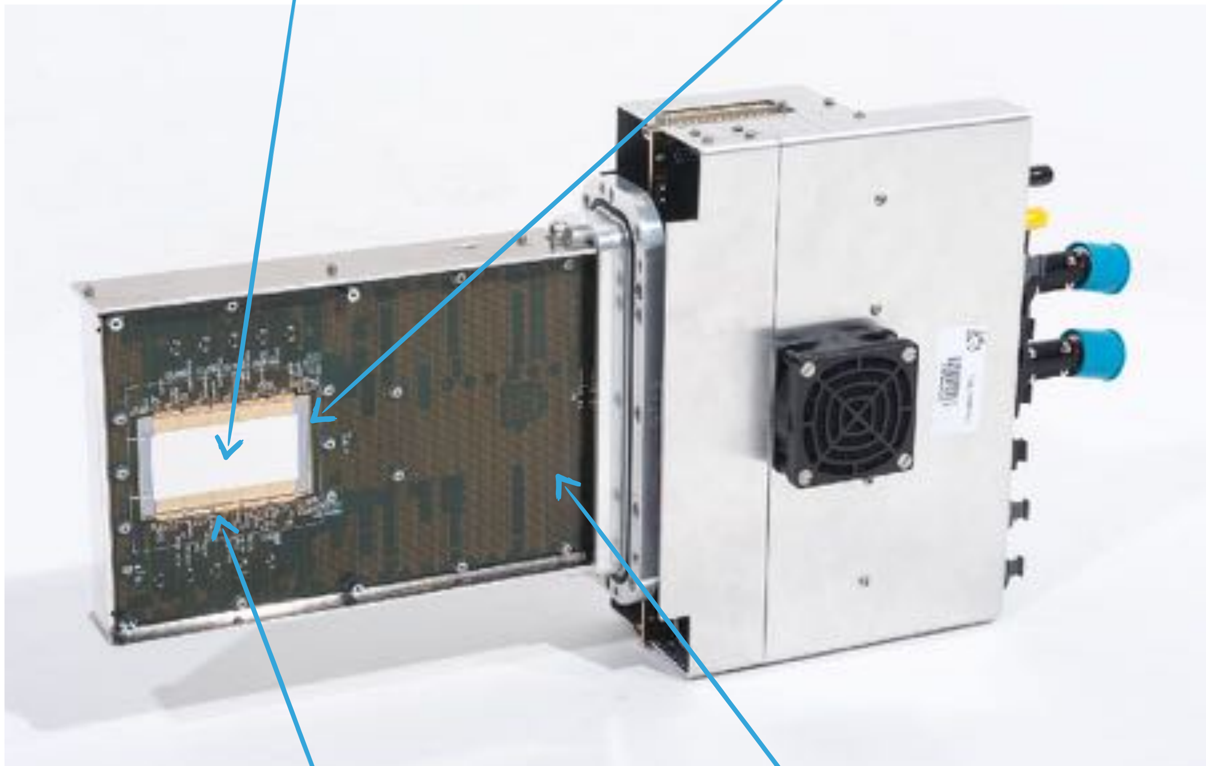
The GTK module

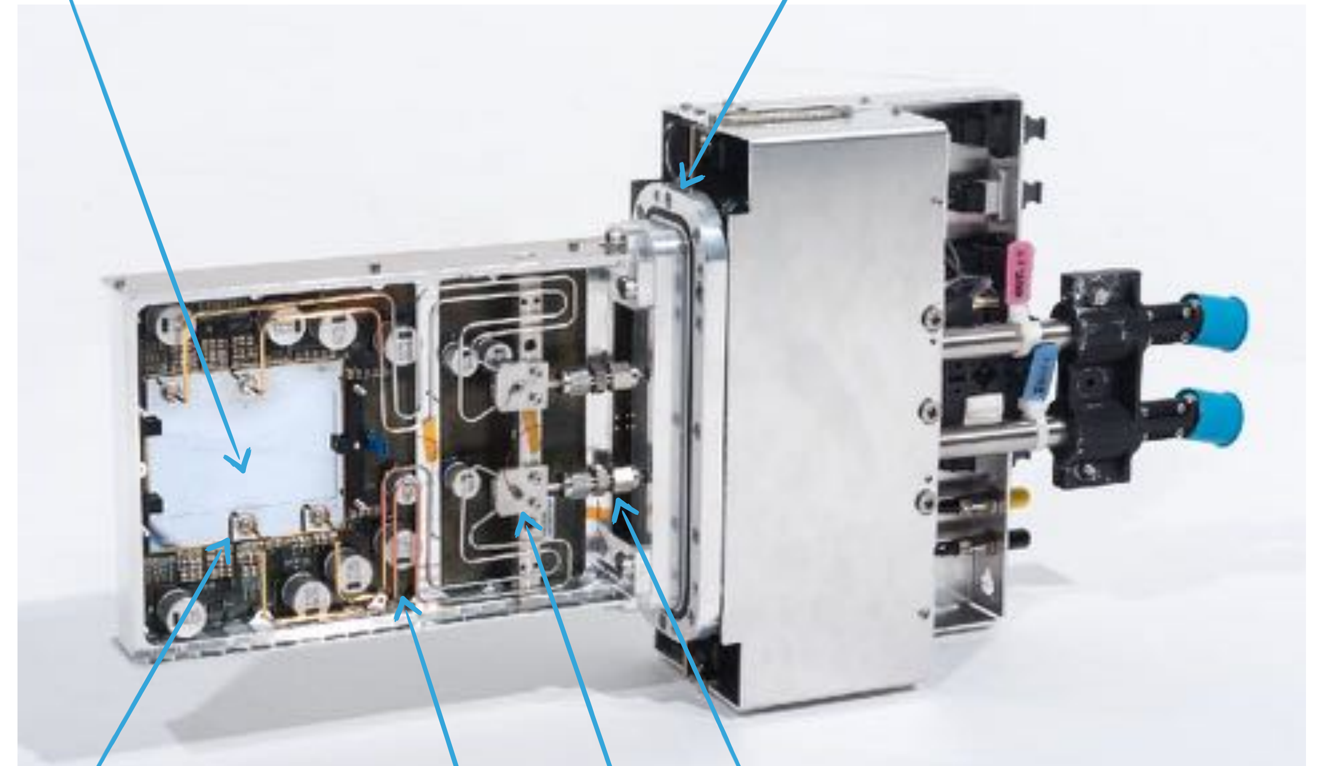
Sensor
- 200 µm thick Si (≥ 3kΩcm)
- Surface: 60.8 x 27.0 mm^2
- planar matrix of 18000 n-in-p 300 x 300 µm^2 pixel diodes

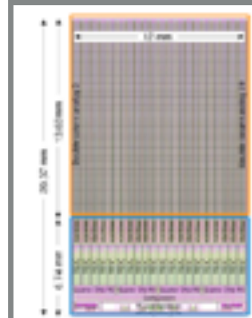
Cooling and support plate
- silicon microchannel cooling plate
- 2 networks of 75 microchannels (200 x 70 µm^2)
- Hybrid glued on cooling plate
- Cooling plate clamped to PCB



Vacuum flange
- ensures leak tightness
- position of GTK in the beam







TDCPix
- 100 µm thick
- ~15 µm high SnAg bumps
- Large chip: ~19 mm x 12 mm
- Power consumption: 3.5 W per chip
- Analog circuitry: 0.4 W/cm^2
- Digital circuitry: 3.2 W/cm^2

GTK_Carrier
- 14 metal layers PCB
- Electrical signals vacuum feed-through
- 40 differential 3.2 Gb/s signals over 30cm

KOVAR Connectors
- FeNiCo alloy
- CTE ~5x10^{-6} K^{-1}

1/8" SS capillaries
- Fluidic feed-through

Manifolds
- INLET: 1 x 1/8" to 2 x 1/16"
- OUTLET: 2 x 1/16" to 1 x 1/8"

1/16" SS capillaries

Silicon microchannels to cool the hybrid

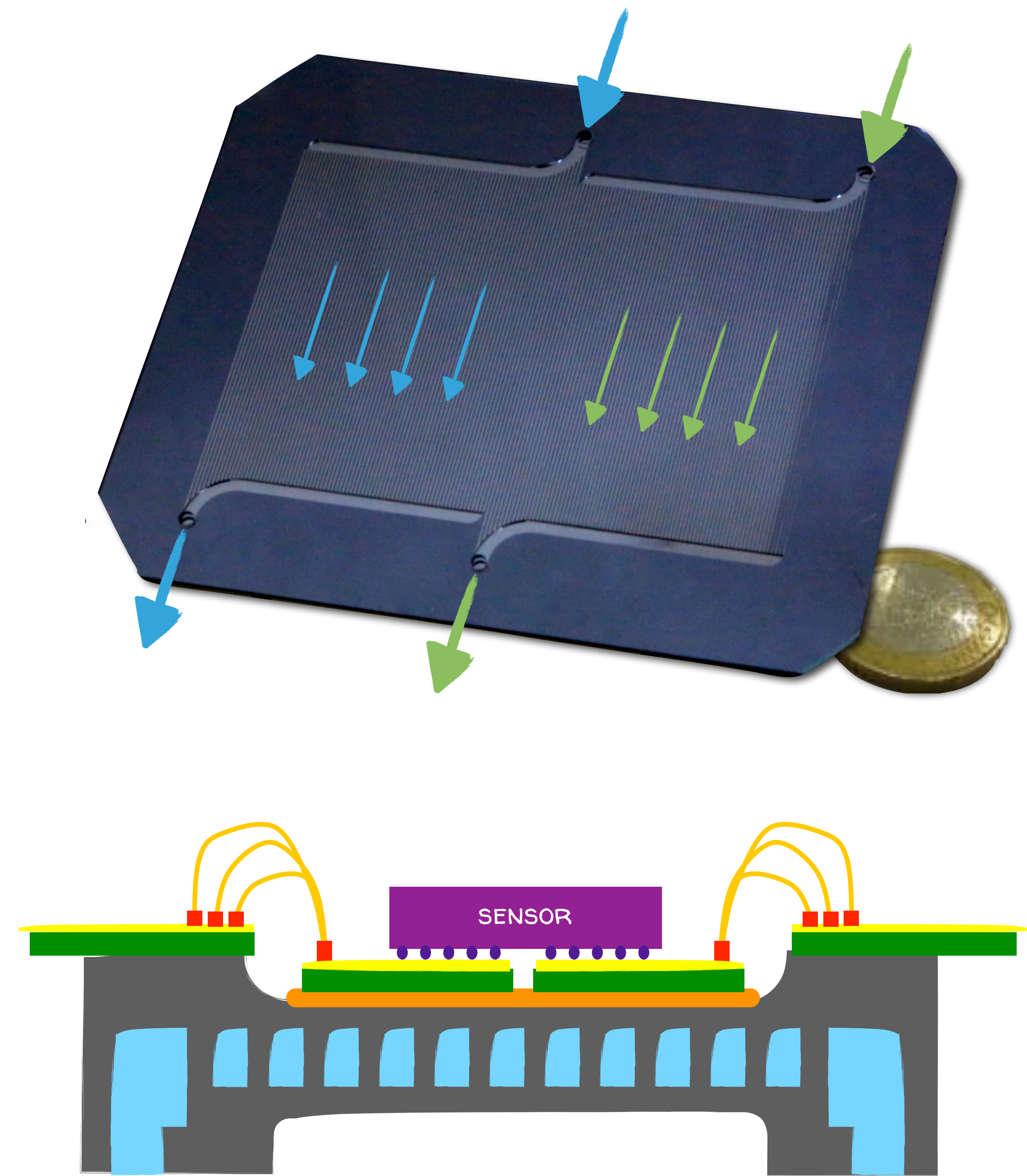
150 microchannels
liquid C_6F_{14}
T -15°C
flow ~3 g/s

sensor
max ΔT 5°C

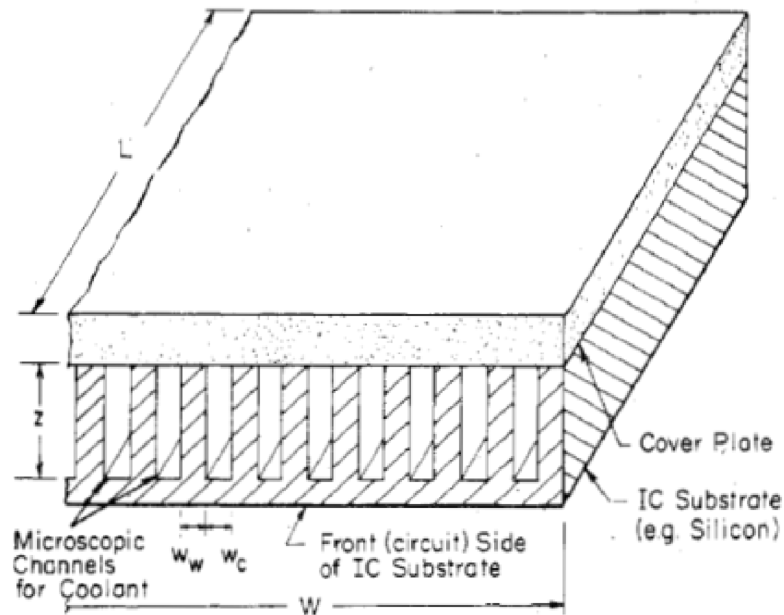
3.2 W/cm²
0.4 W/cm²
3.2 W/cm²

60 mm
100μm
200μm
27 mm
6.7 mm

2 independent networks of 75 microchannels



Why microfluidic on-detector cooling systems ?



D.B. Tuckerman and R.F.W. Pease, IEEE Elec. Dev. Letters, Vol. 2, 5, 1981

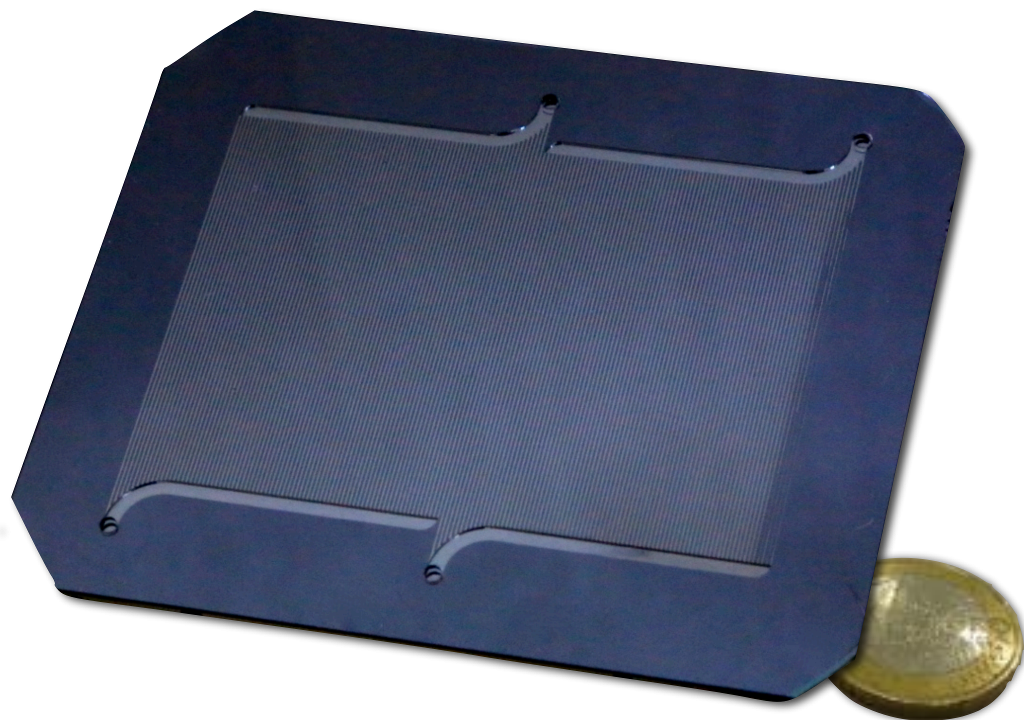
- No CTE mismatch
- Low material budget
- Active/distributed cooling
- Radiation resistance
- Great integration potential
- Thermal Figure of Merit (TFM)

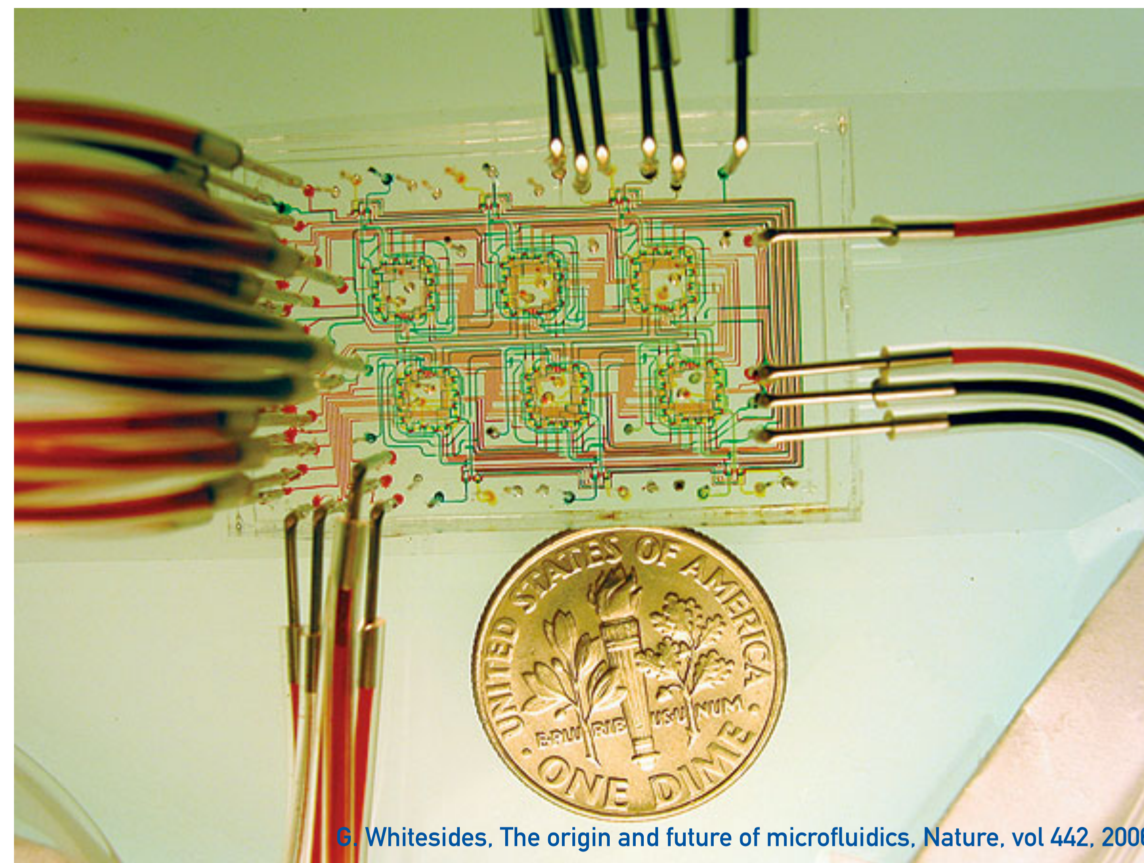
approach	TFM	
conventional Thermal conductive ledge Critical thermal contact! (ΔCTE, surface of contact...) (CFRP) Mechanical support	20	
integrated CARBON FOAM PIPE	12	
microchannels	5-8 liquid	***NA62*** ***C_6F_{14}***
	3 bi-phase	LHCb ***CO_2***

next talk by Oscar

$$TFM = \frac{(\Delta T \text{ fluid-sensor})}{(\text{power density})}$$

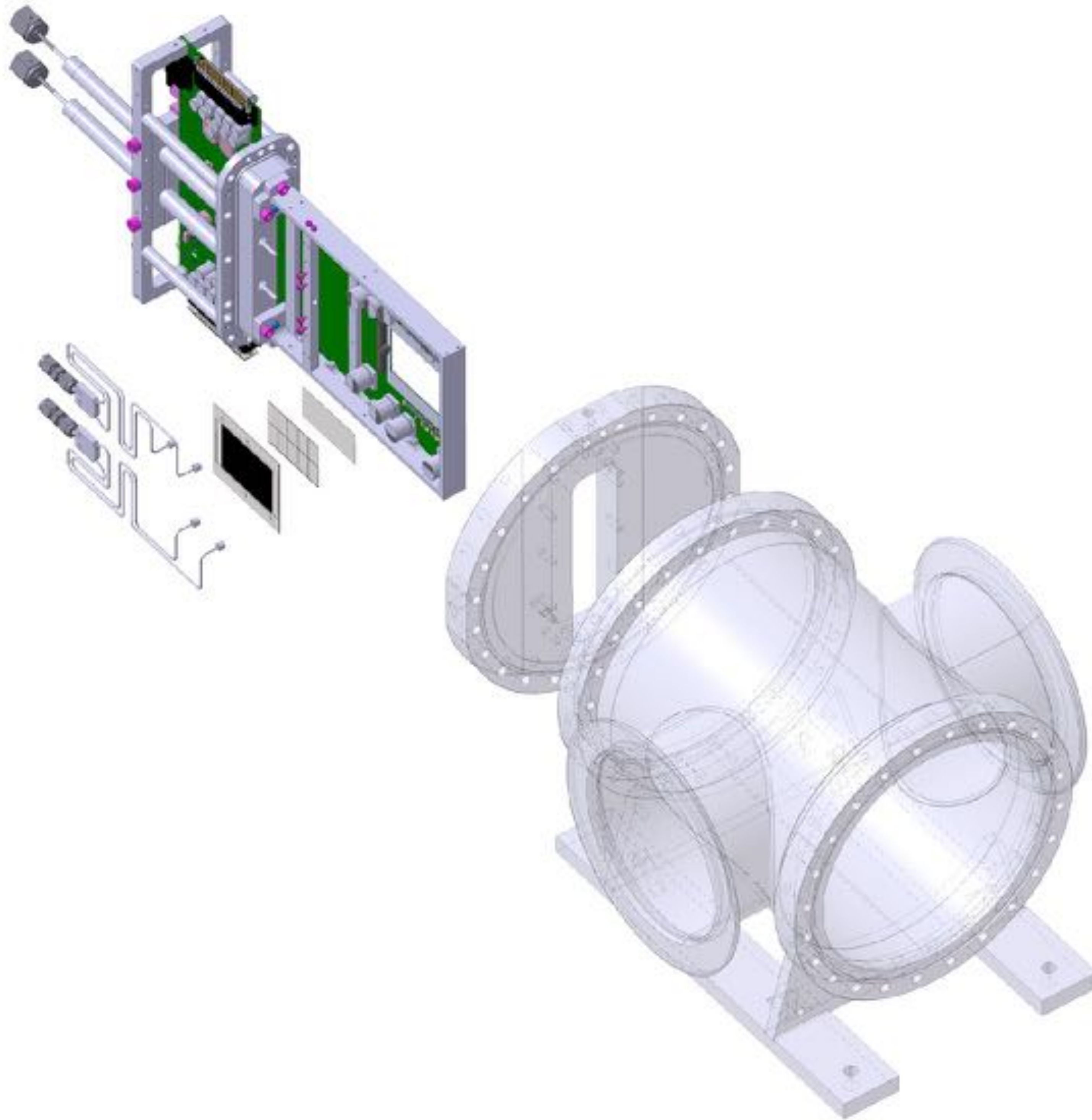
Microfluidics for the GTK


NA62 GTK silicon cooling plate


G. Whitesides, The origin and future of microfluidics, Nature, vol 442, 2006

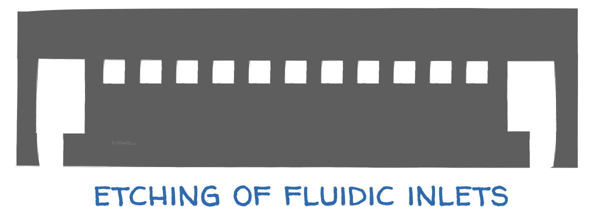
- The GTK cooling plates look simple with respect to other microfluidic devices.
  - Straight parallel microchannels
  - 4 fluidic connections
- Challenging microfabrication process and system integration.
  - The size of the device is much bigger than usual (cm^2 wrt mm^2).
  - Full silicon process (Deep etching, Direct Wafer Bonding).
  - Reliable (leak-tight) operation in vacuum.

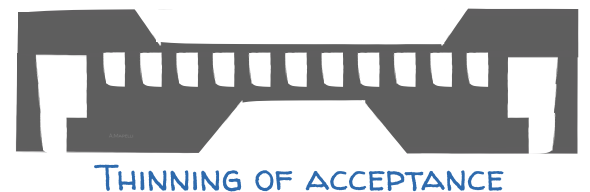
fabrication and assembly of GTK modules

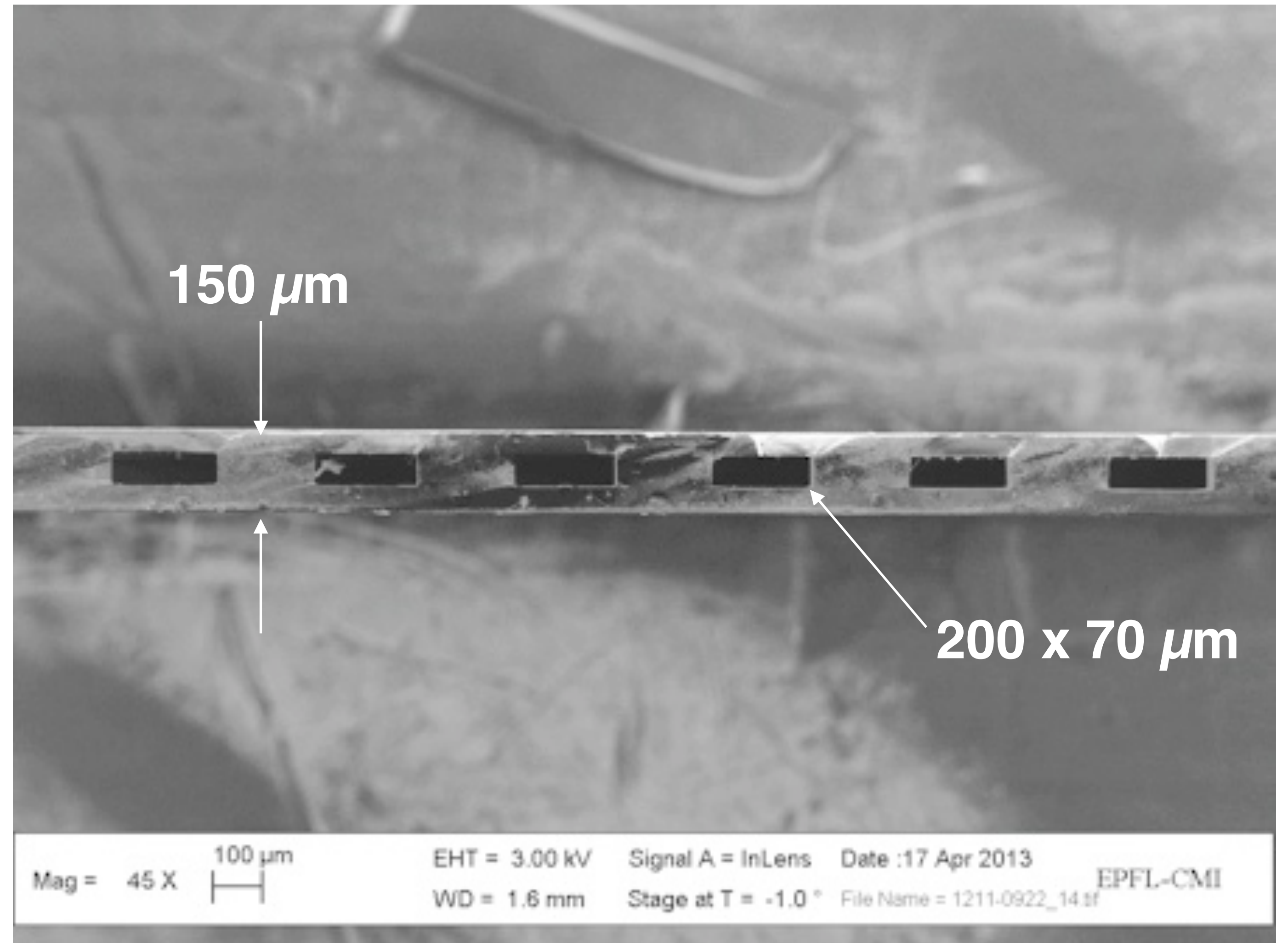


- microfabrication of cooling plates
- bending of capillaries and soldering to cooling plate
- glueing of hybrid on cooling plate
- preparation of GTK_carrier
- positioning of hybrid in GTK_Carrier
- wire-bonding

Microfabrication of the cooling plates

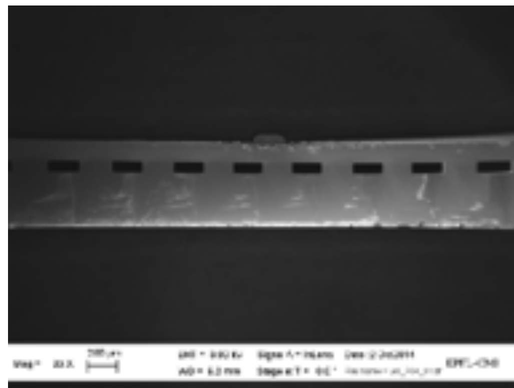


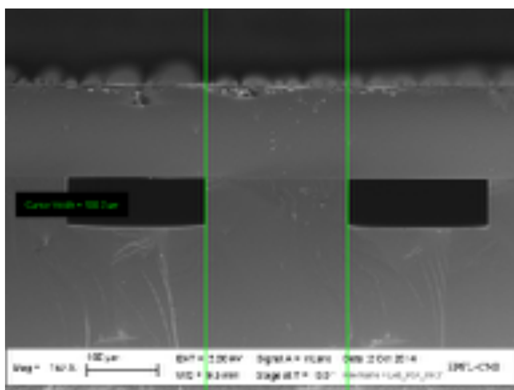


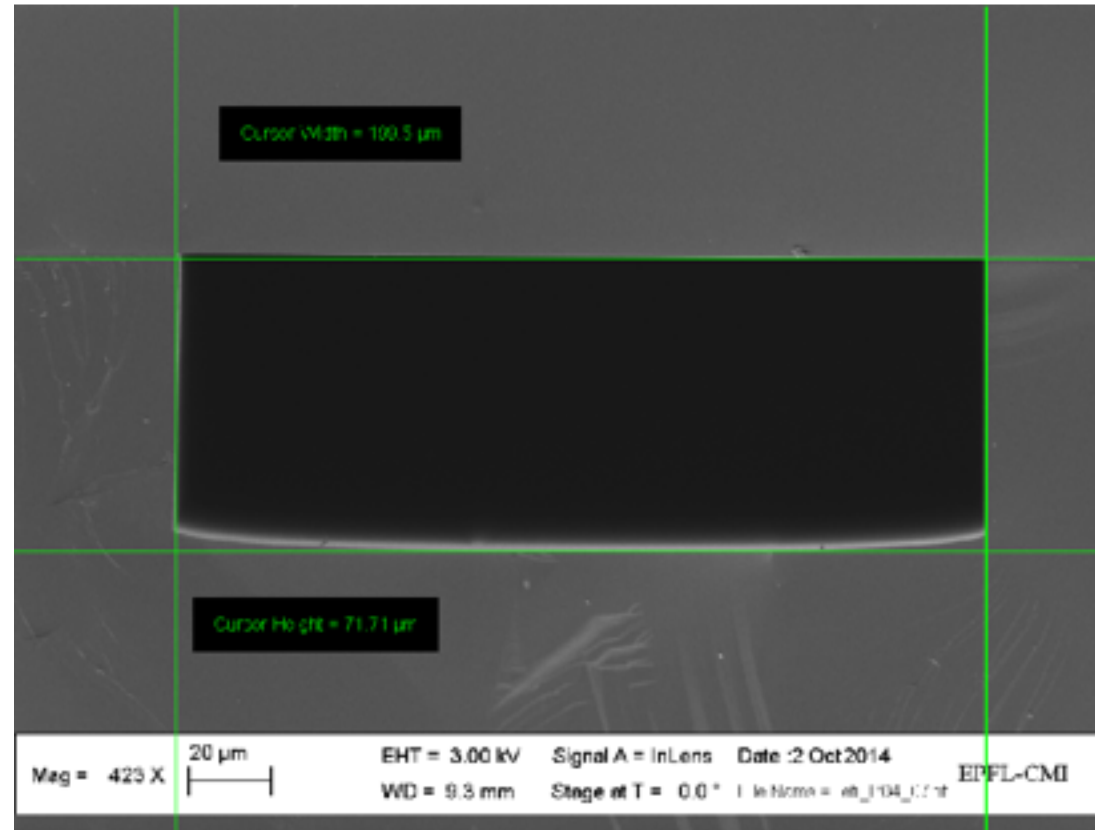


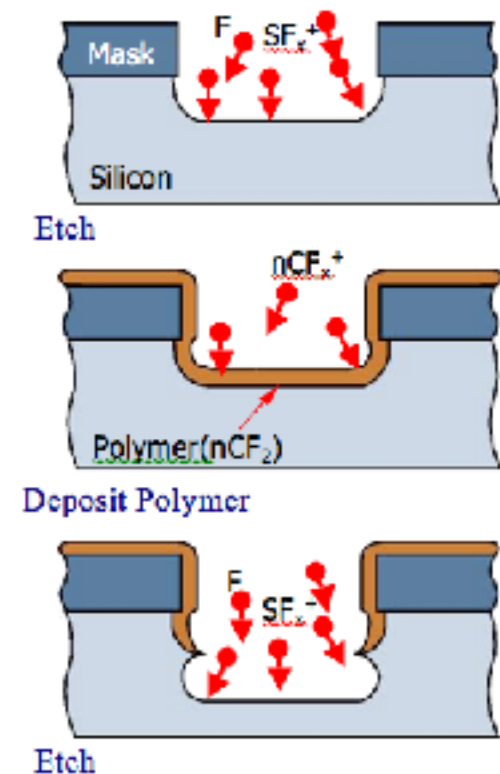
- Collaborative effort between experiments (**ALICE, LHCb and NA62**), CERN support groups (**DT and ESE**), and external partners (**CSEM and EPFL**).
- Design by CERN EP-DT
- Prototypes fabricated by EP-DT at EPFL-CMi on 4" wafers
- Pre-production series by IceMOS on 6" wafers
- Two batches fabricated at CEA-Leti on 8" wafers
- Third batch under production, delivery expected at the end of the year.

Etching of the microchannels

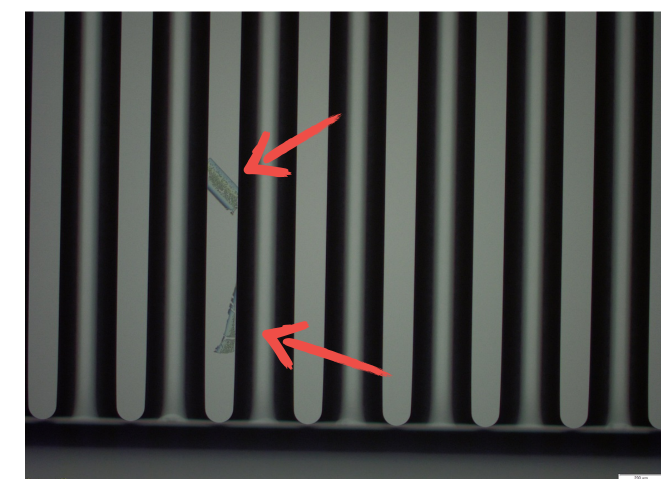








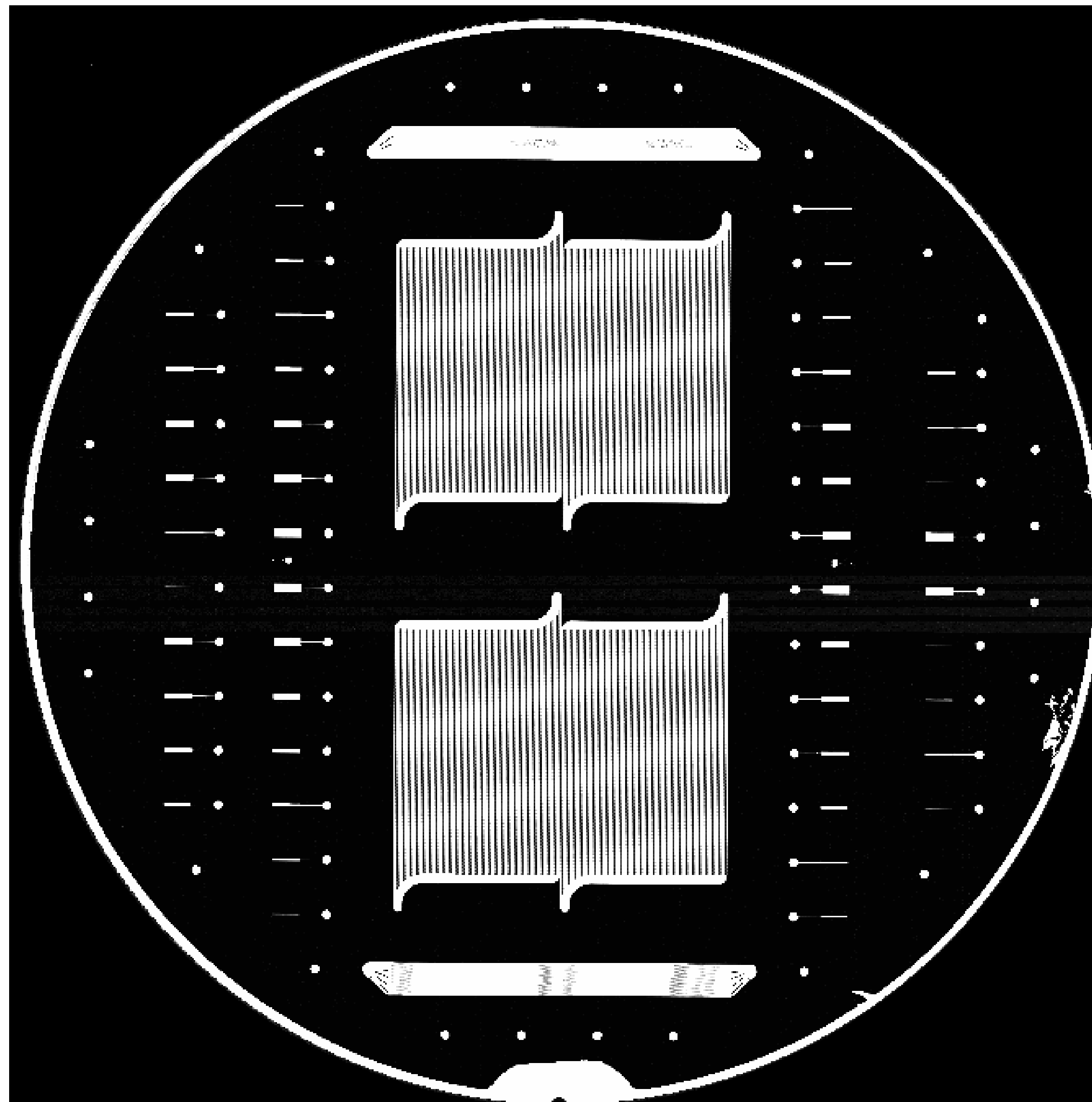
- Deep Reactive Ion Etching (DRIE)
  - depth: 70 µm
  - width: 200 µm
  - pitch:400 µm
- Passivation polymers can lead to issues during wafer bonding.
- During cleaning they can detach form the sidewalls of the channels and re-deposit on the surface to be bonded.
- Additional decontamination and cleaning steps are required.

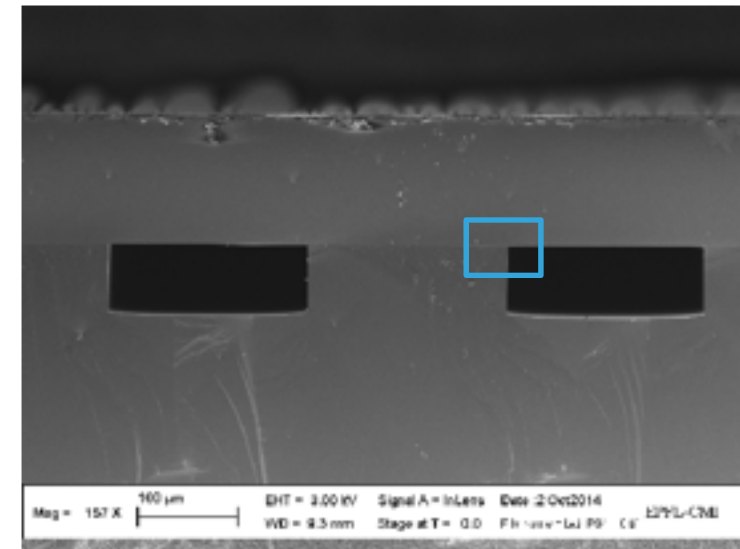


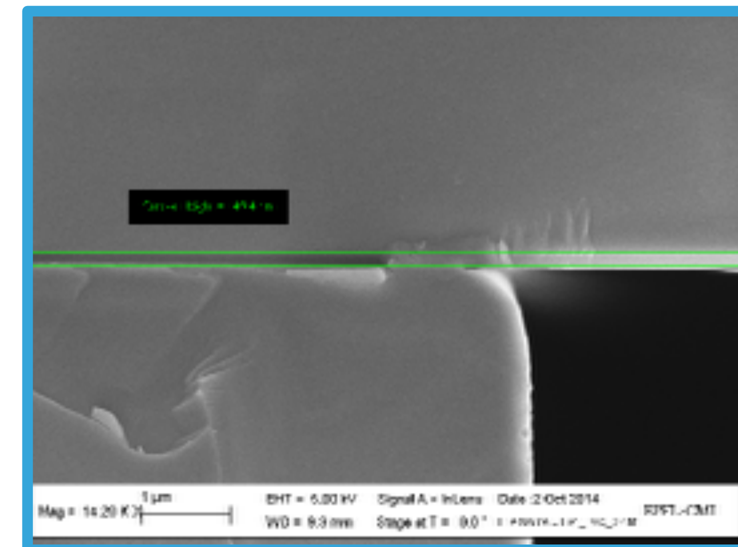
Passivation polymers detaching from sidewalls.

Wafer bonding - surface preparation

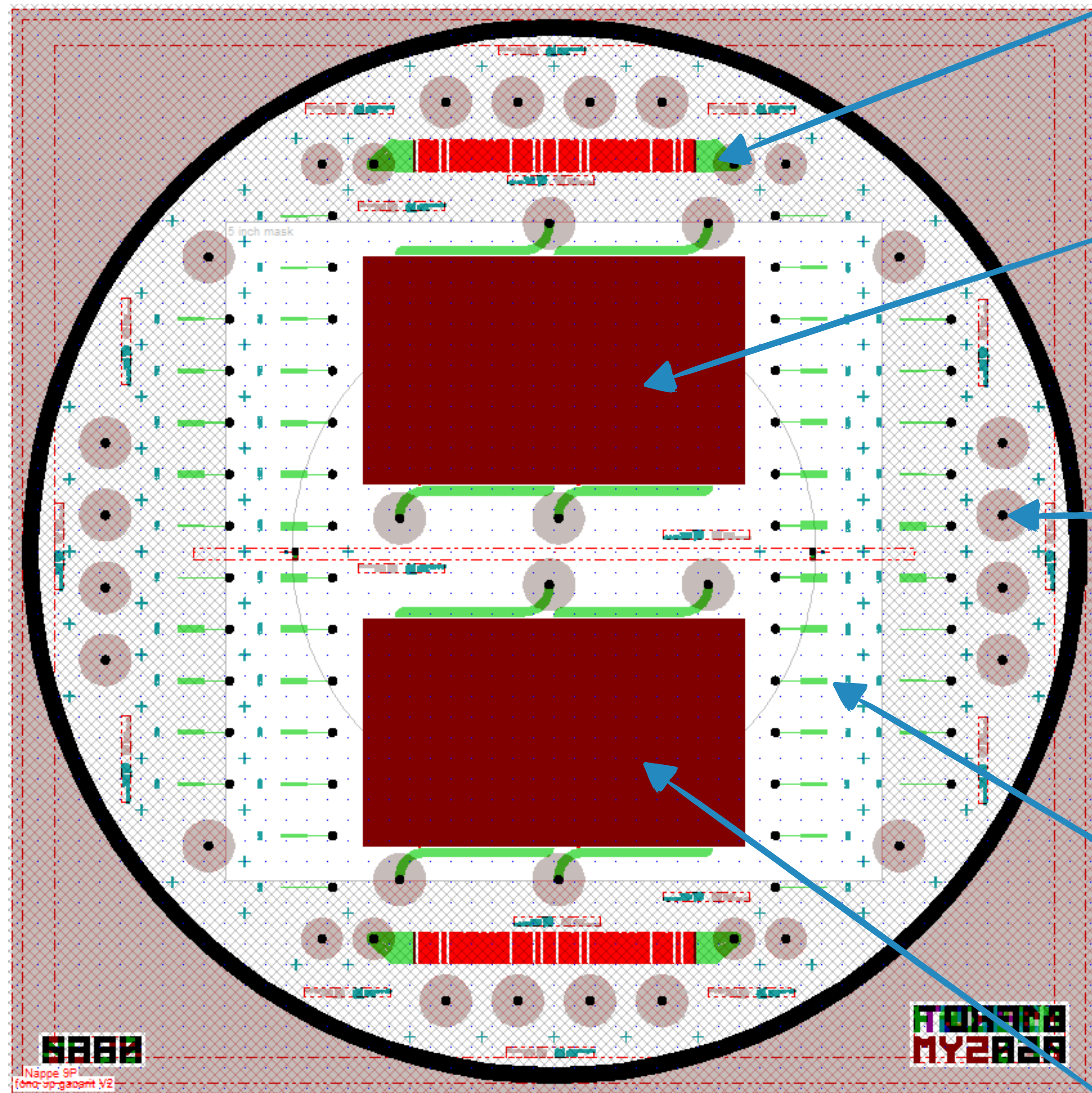
- Silicon direct bonding extremely sensitive to surface roughness and cleanliness.
- Dedicated wafers processed at CEA-Leti to study the surface preparation. The size of the microfluidic circuits is much bigger than standard MEMS and required additional efforts.
- Scanning Acoustic Microscopy to visualise interface defects.







Layout of wafers fabricated at CEA-Leti



2x branches to fabricate cooling frames (alternative solution)

Cooling plate TOP

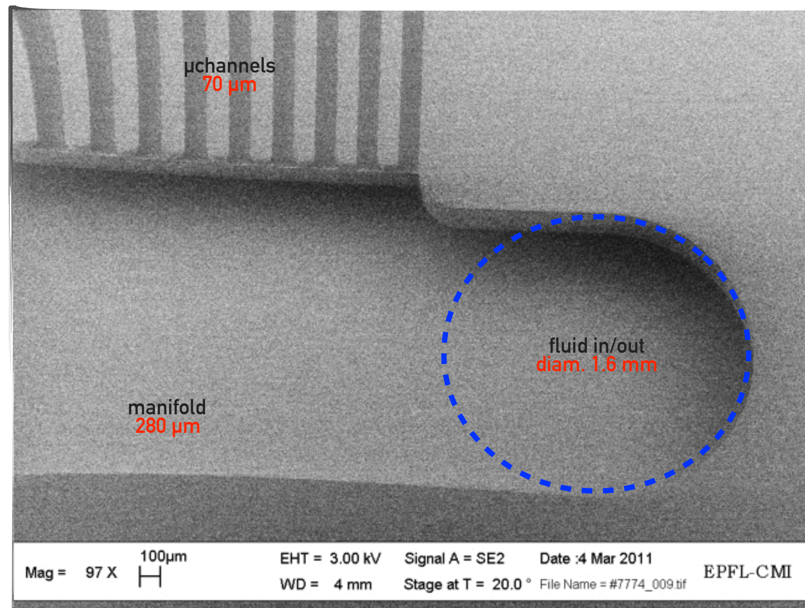
24 x Soldering test samples - QA/QC (common study with LHCb)

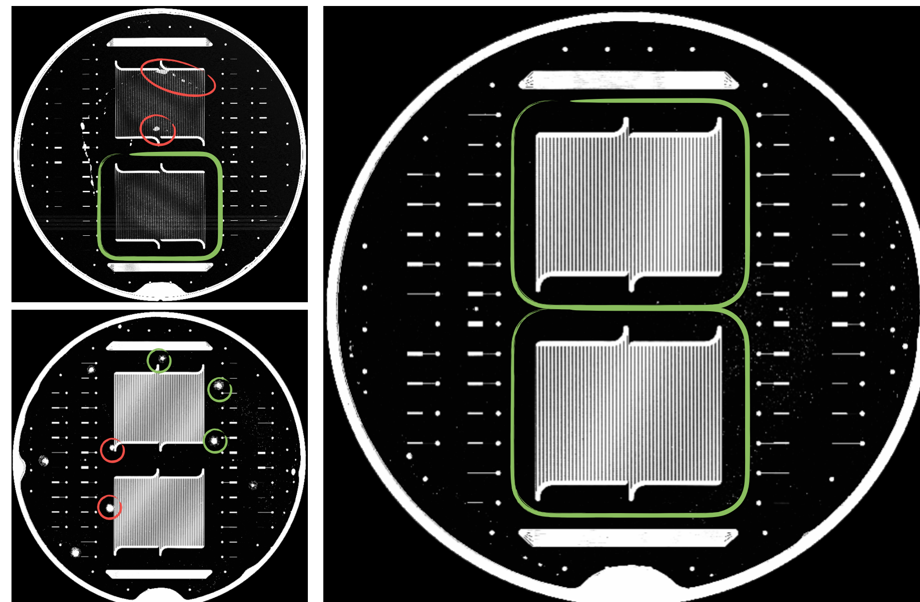
48 x Pressure test samples - QA/QC

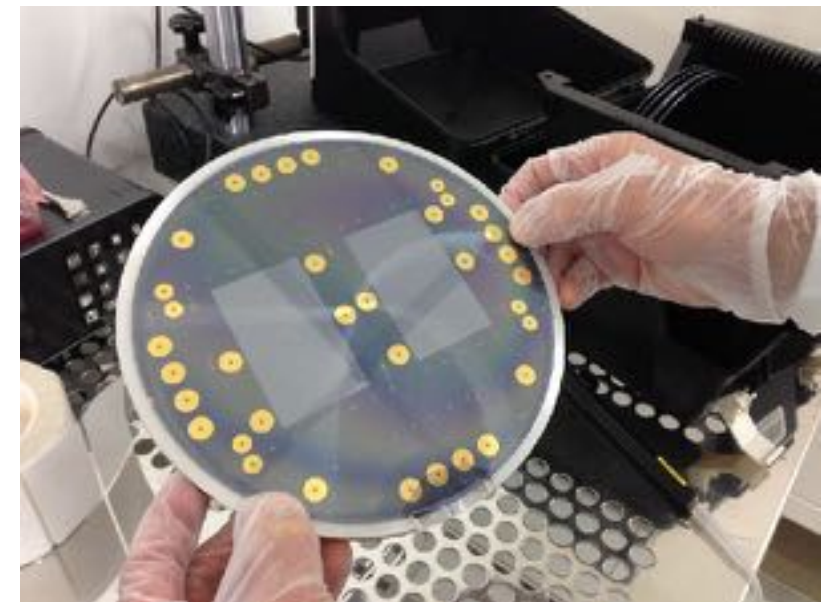
Cooling plate BOT

Acceptance of cooling plates 1/2

- 1. Etching profiles of the microchannels.
- 2. Scanning Acoustic Microscopy of bonded wafers.
- 3. Visual inspection during tape-out.

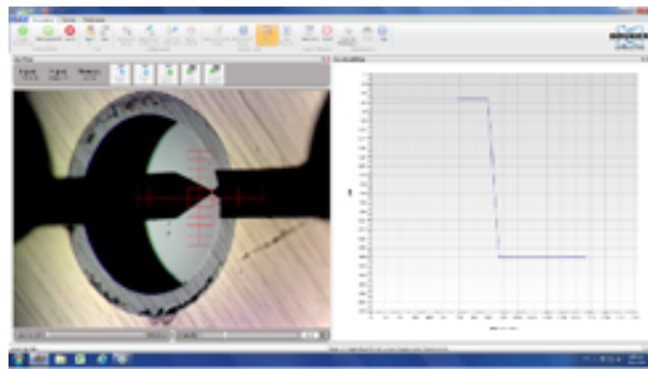
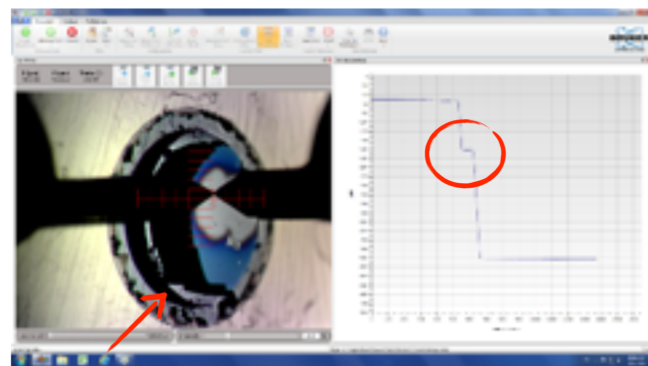




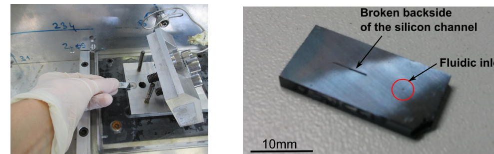


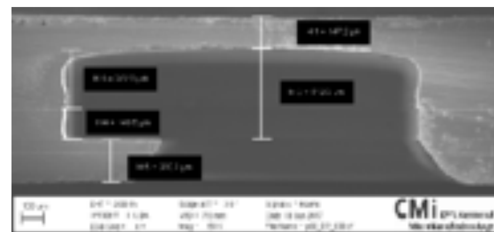
Acceptance of cooling plates 2/2

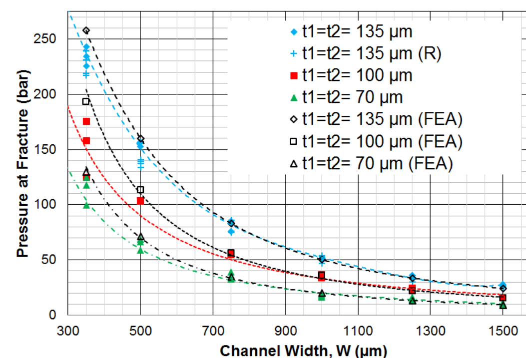
- 3. Metrology of cooling plates (Inlets and pools).
- 4. Pressure tests on dedicated samples.
  - 1500 μm wide cavities (manifolds) > 25 bars
  - 200 μm wide cavities (microchannels) > 200 bars
  - Soldering pads > 200 bars
- 5. Pressure and temperature cycles on each soldered cooling plate.

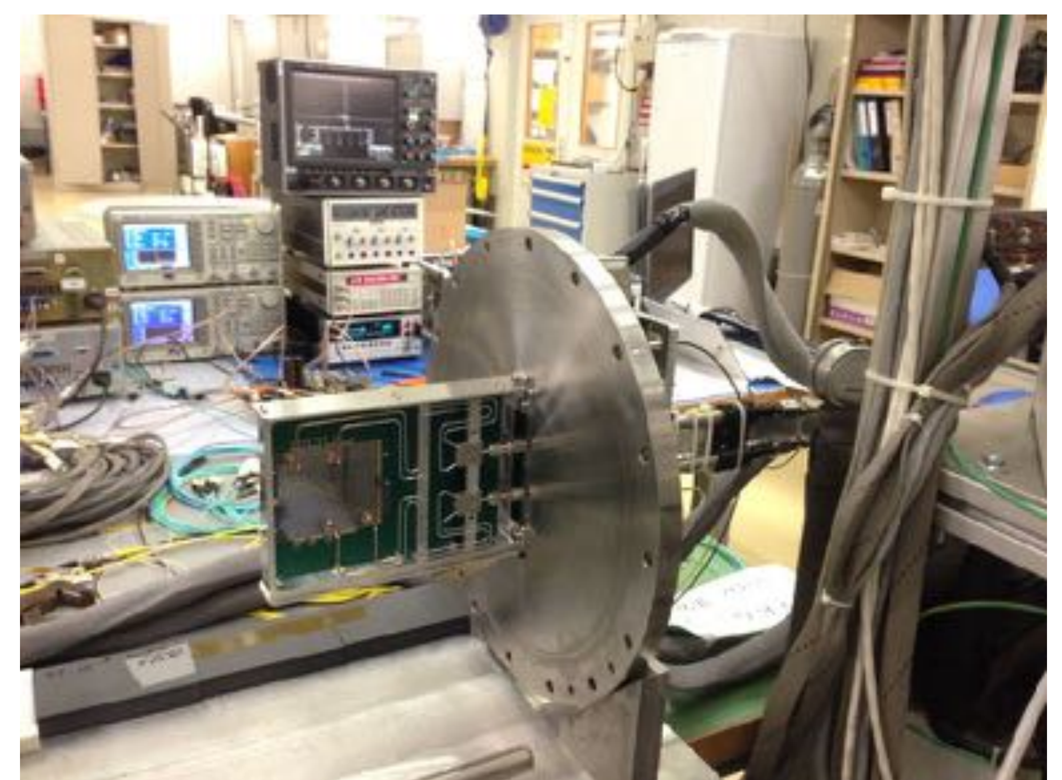
Metrology of fluidic inlet/outlet





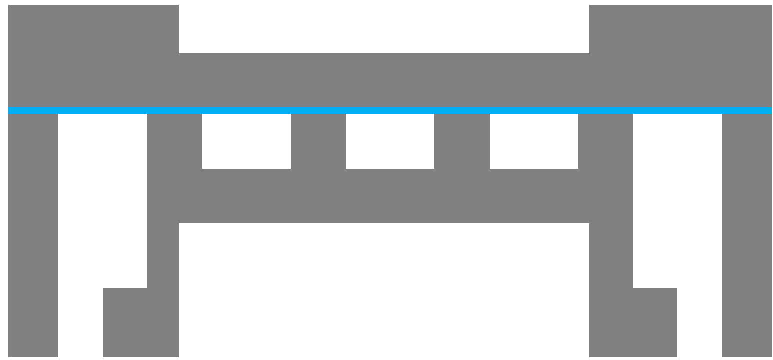


Pressure testing of silicon microchannels

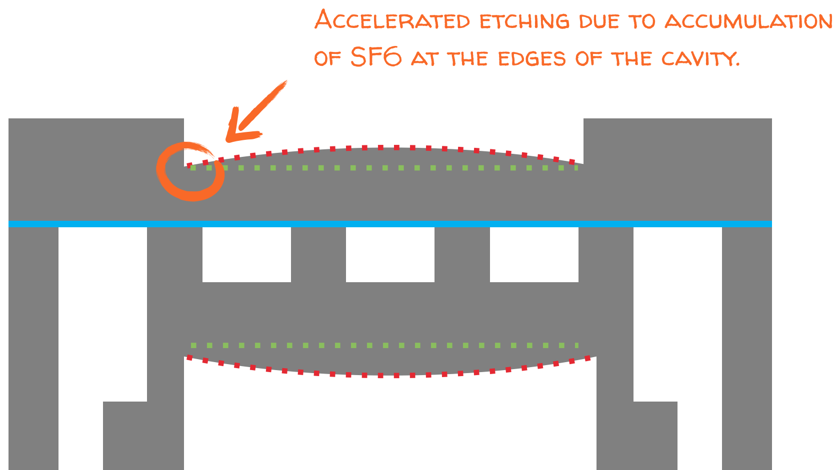


Cooling test setup at CERN

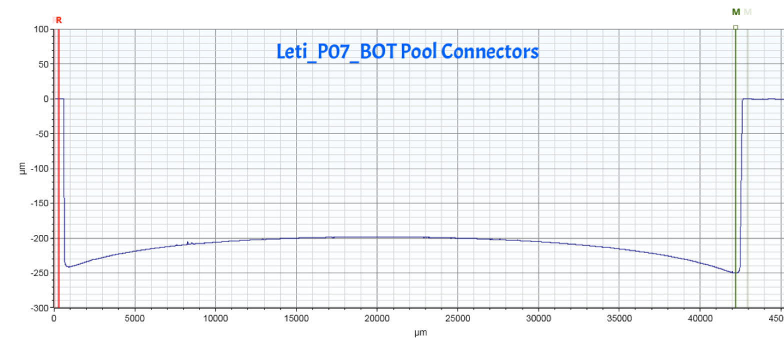
Thinning the cooling plates in the acceptance

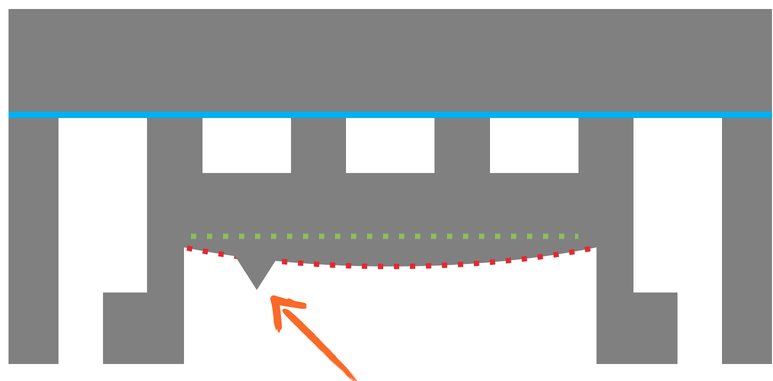


- Bulk wafer bonded to another bulk wafer.
- Flat surfaces expected with DRIE in the “pools”.

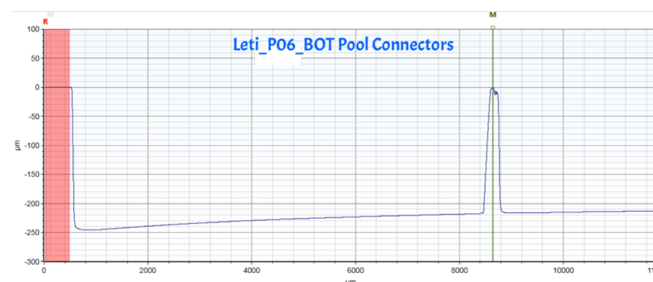


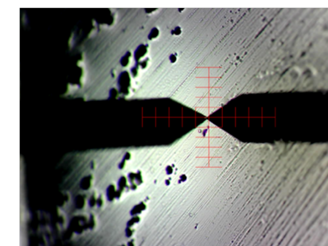
- DRIE in the acceptance led to **convex** surfaces.

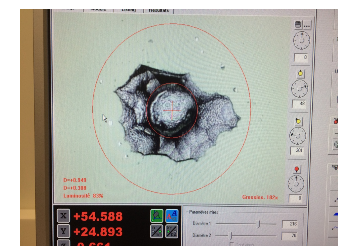




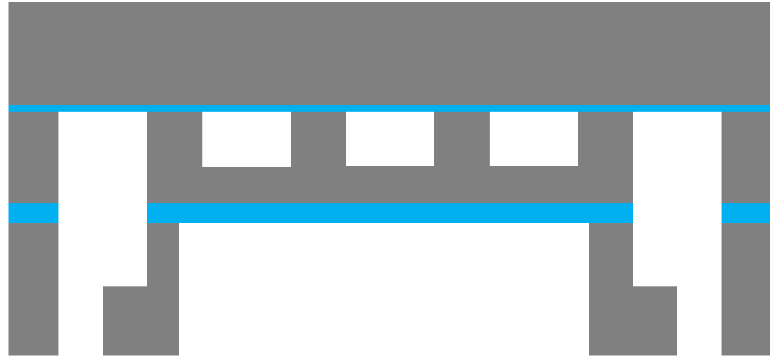
- No thinning of the top wafer.
- Convex backside with **defects**.



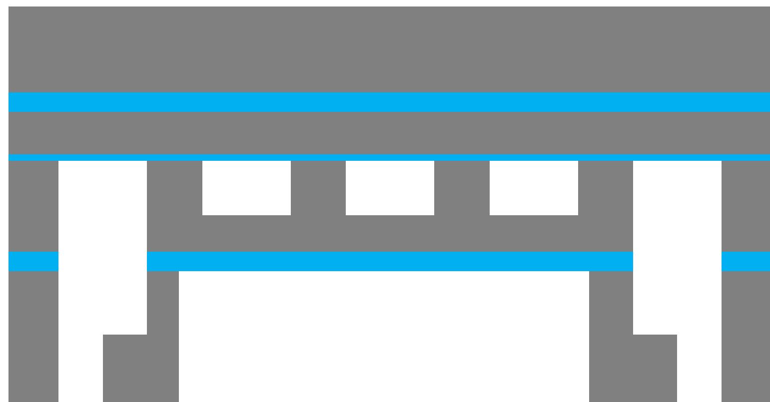




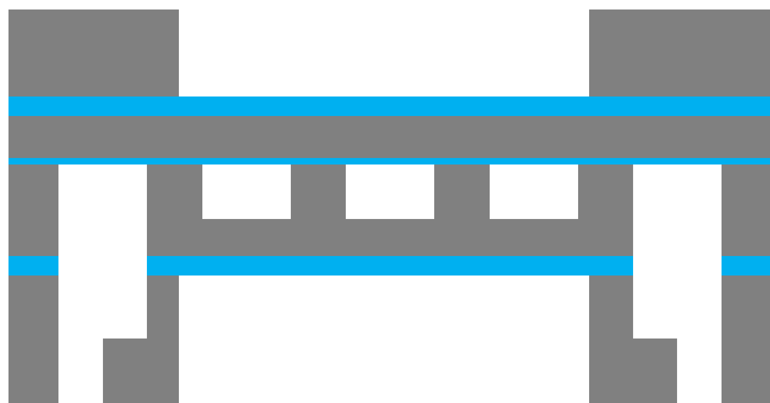
Process optimisation with SOI wafers



- Channels etched in SOI wafer
- Bulk wafer bonded to close the channels.
- Effort required to get good bonding quality with SOI.



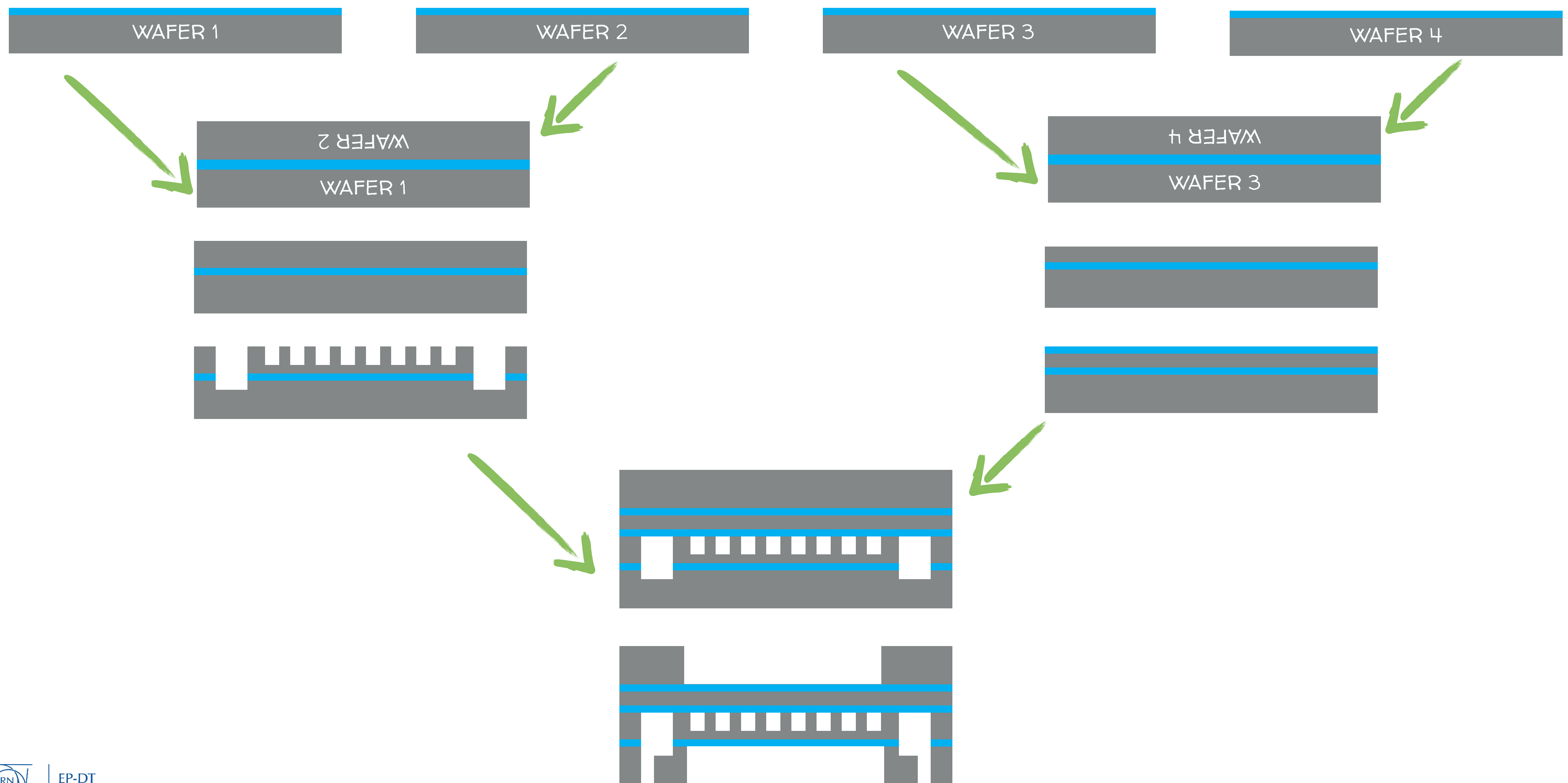
- Validation of SOI to SOI bonding.
- Only backside thinning.



- SOI to SOI wafer bonding.
- Thinning topside and backside.

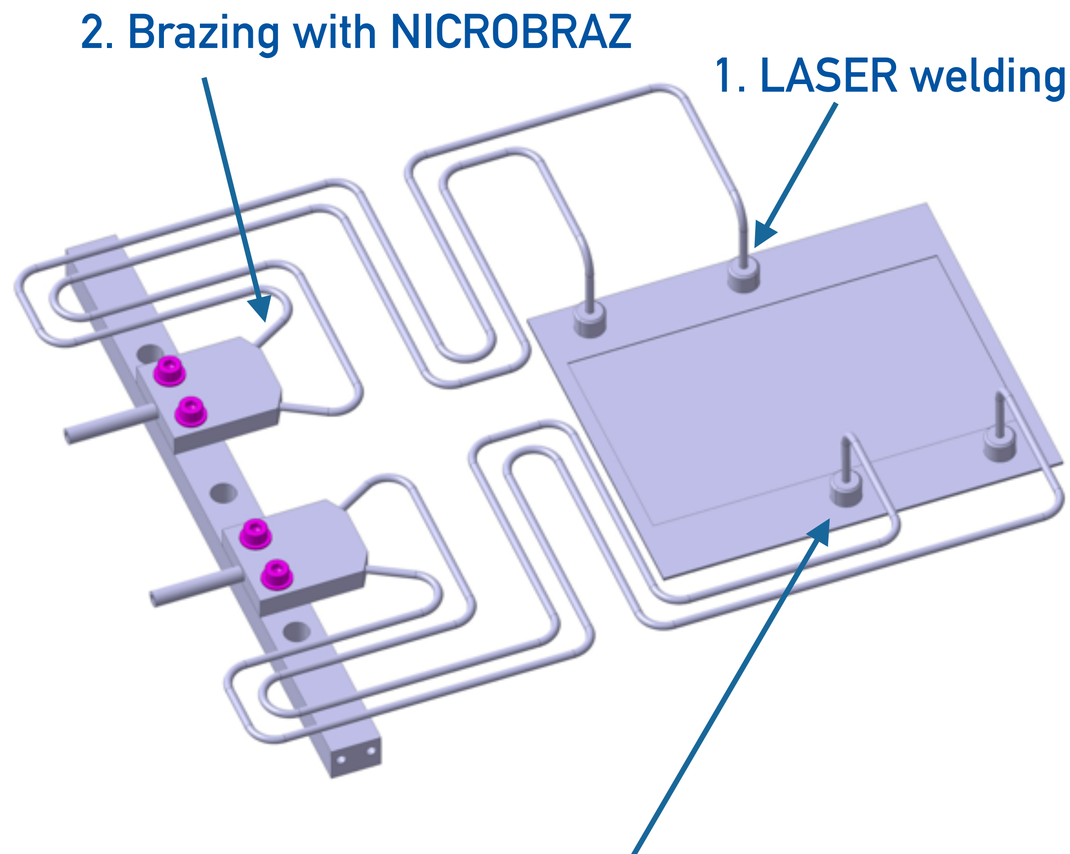
SOI-to-SOI… 4 wafers stack

- The SOI wafers used in this process are B-SOI (Bonded SOI).
- The cooling plates are a stack of four Si wafers bonded together.
- The thickness in the acceptance is defined by the thicknesses of the device layers of each SOI.



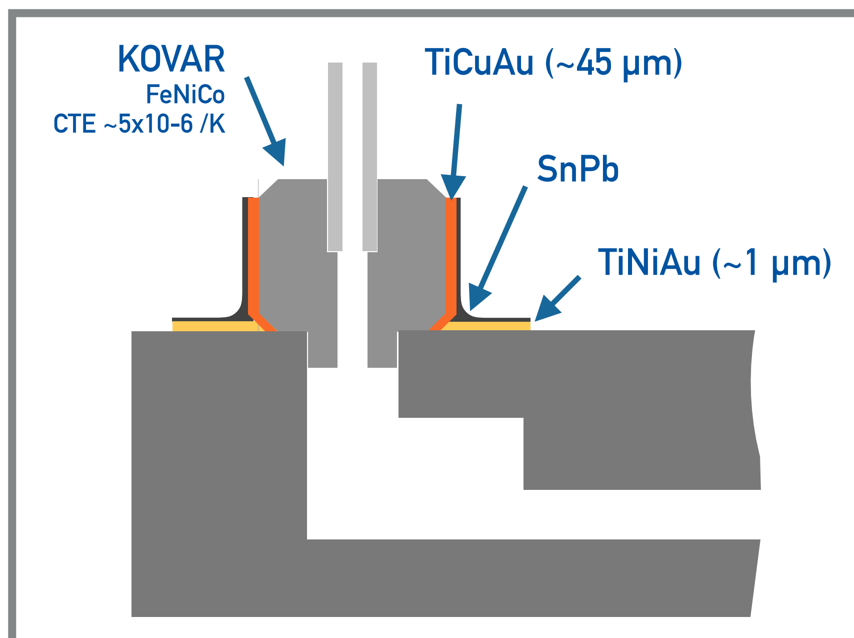
Microfluidic system integration

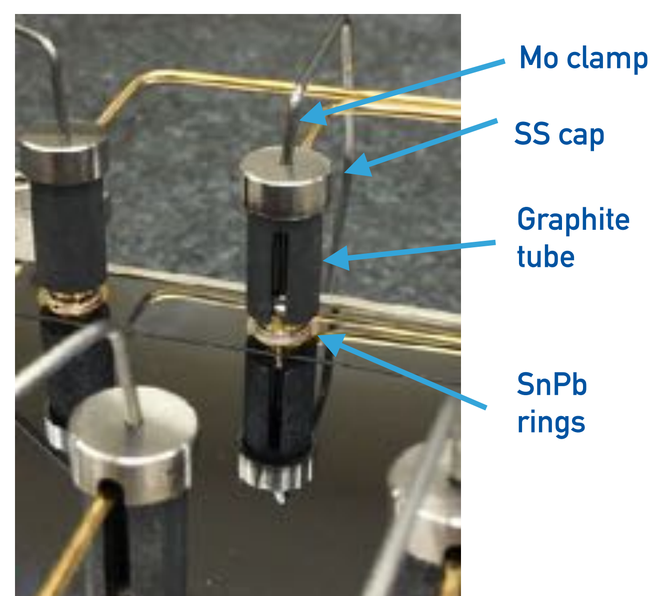
common development with LHCb

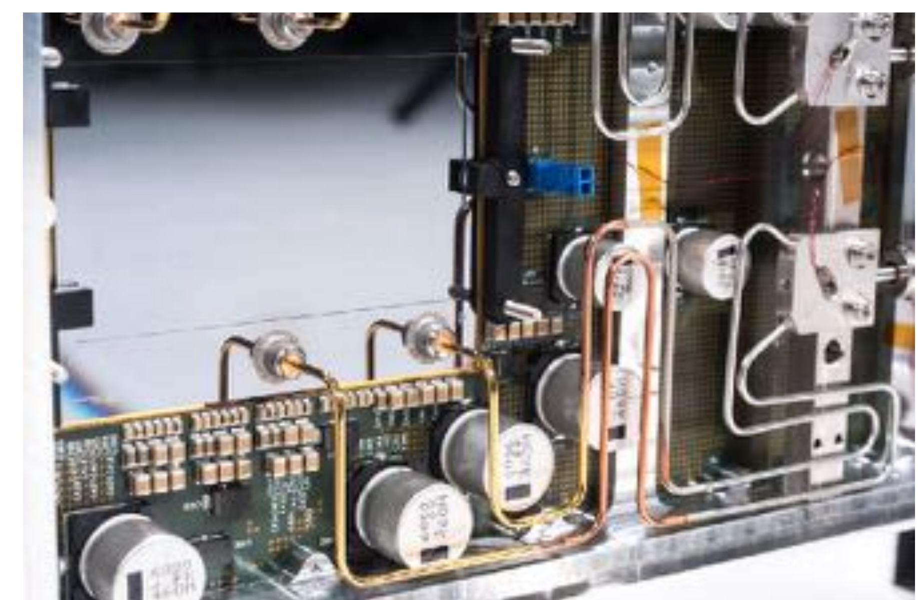


- Machining of KOVAR connectors
- LASER welding of connectors to capillaries
- Bending the capillaries
- Brazing the other end of the capillaries to SS manifolds
- NiCuAu plating of connectors
- Soldering of connectors to silicon
- QA/QC:
  - After each joining step the He leak rate is measured. (Acceptance leak rate: 10^{-10} mbar l^{-1} s^{-1}).
  - Pressure testing of the cooling plate at 1.43 x P_{op}

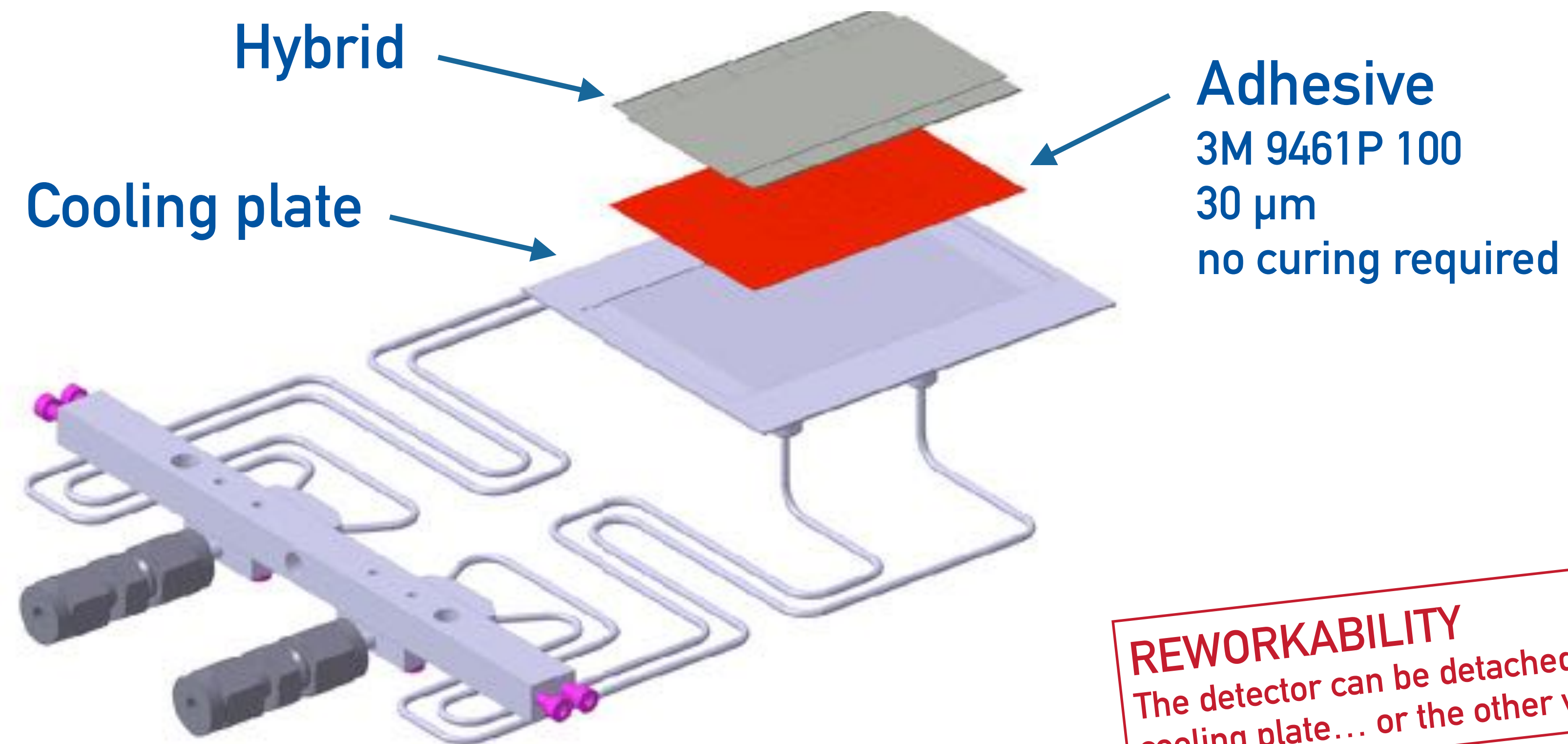
3. Soldering KOVAR connectors to silicon



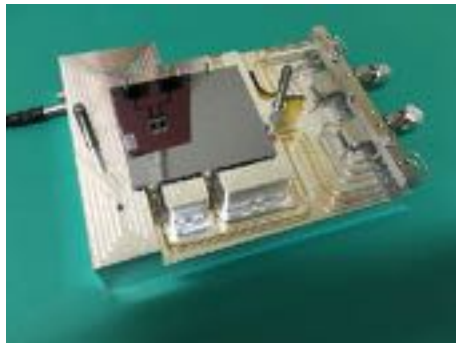


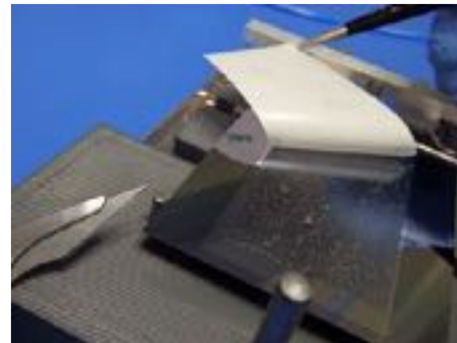


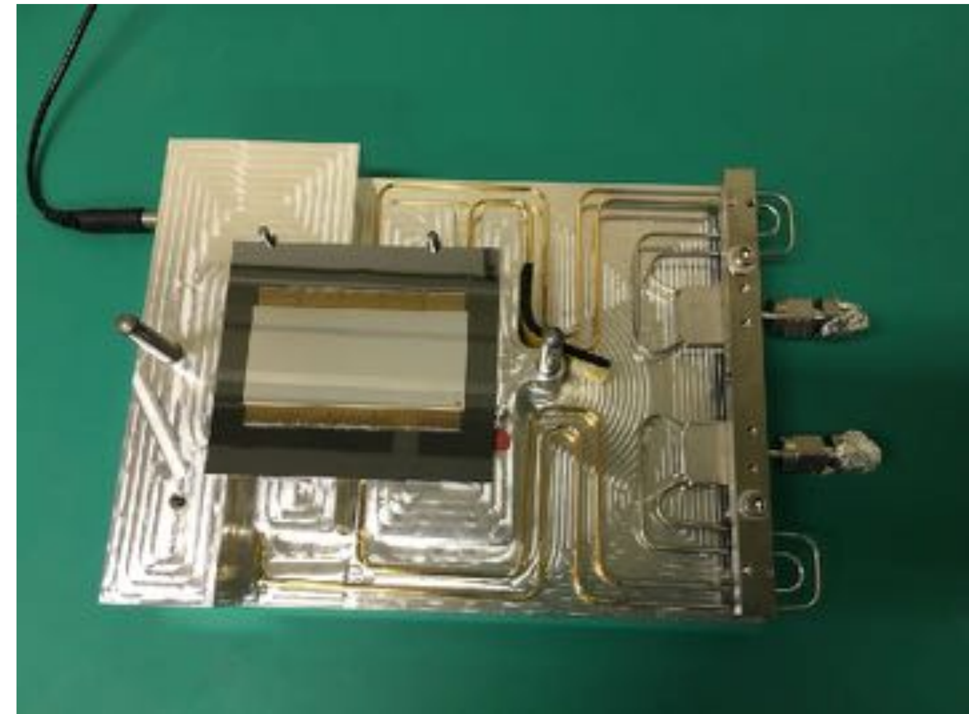
Glueing the hybrid on the cooling plate

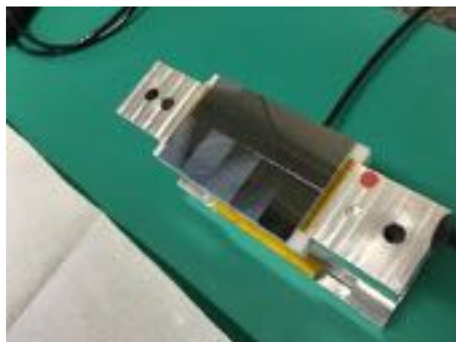


REWORKABILITY
The detector can be detached from the cooling plate… or the other way around.



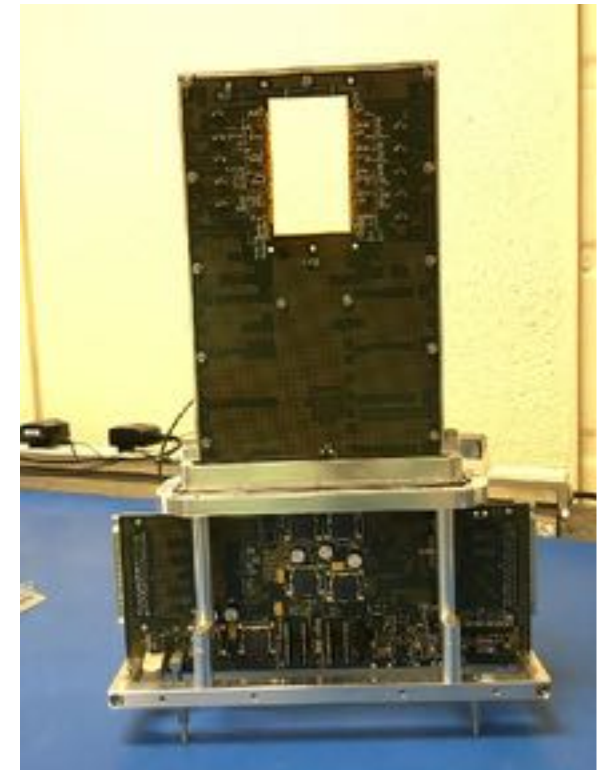


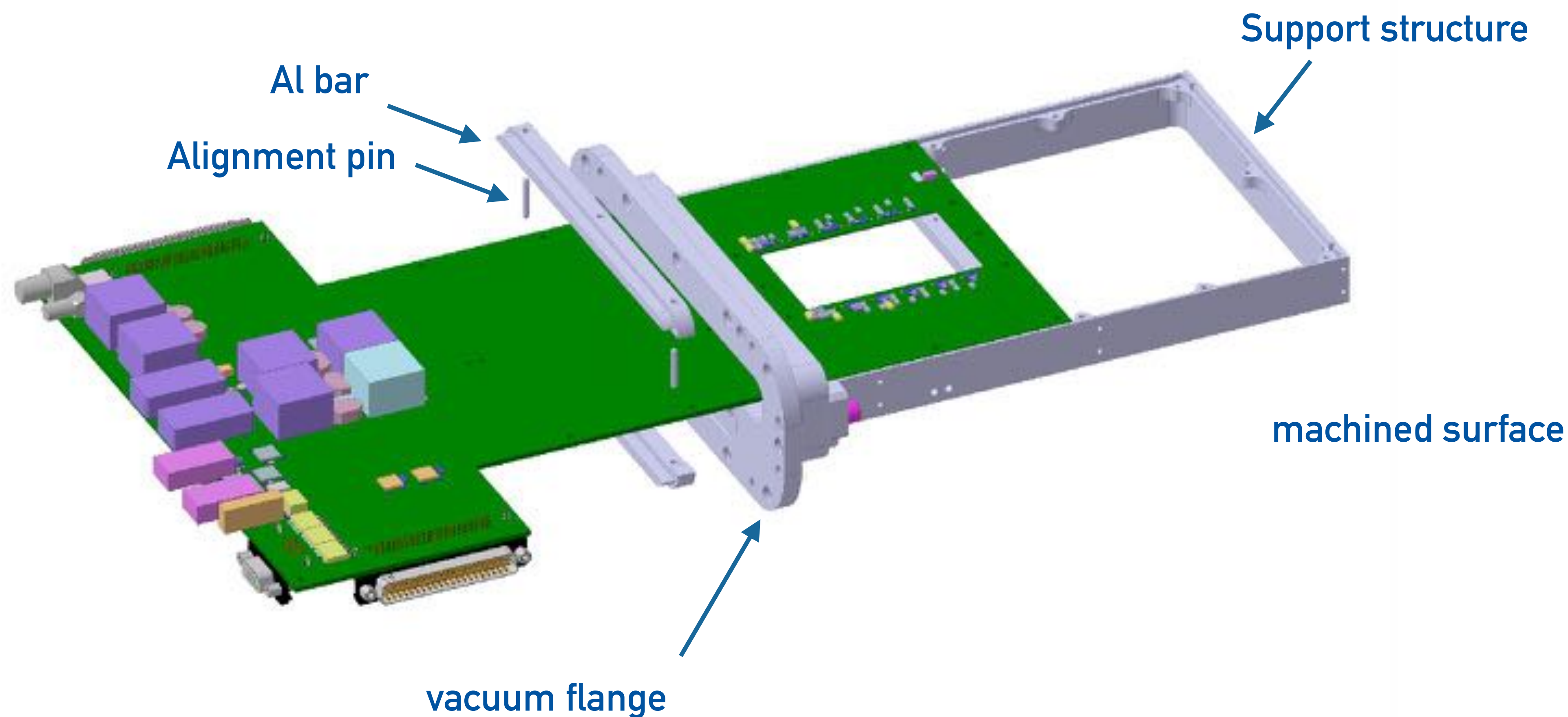


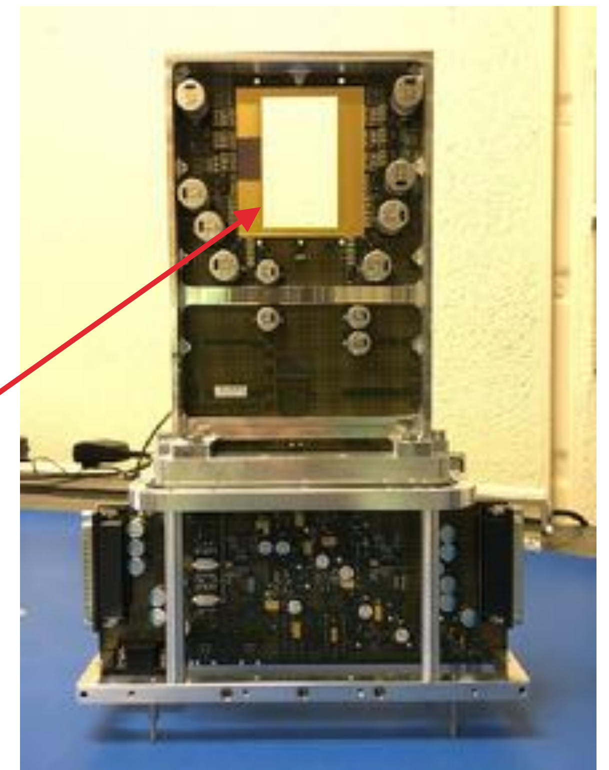


The GTK_carrier

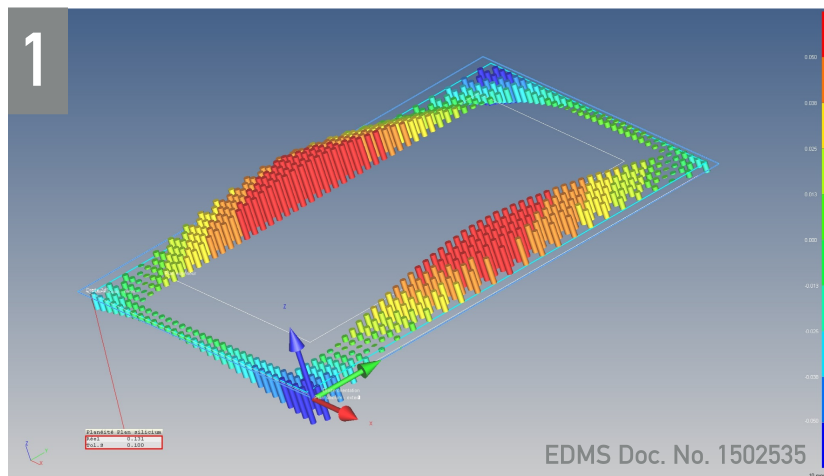
- Position Al bars around PCB.
- Insert the PCB in the vacuum flange and fix it to support.
- Glue the PCB in the flange.
- Measure He leak rate (<10^{-10} mbar l^{-1} s^{-1}).

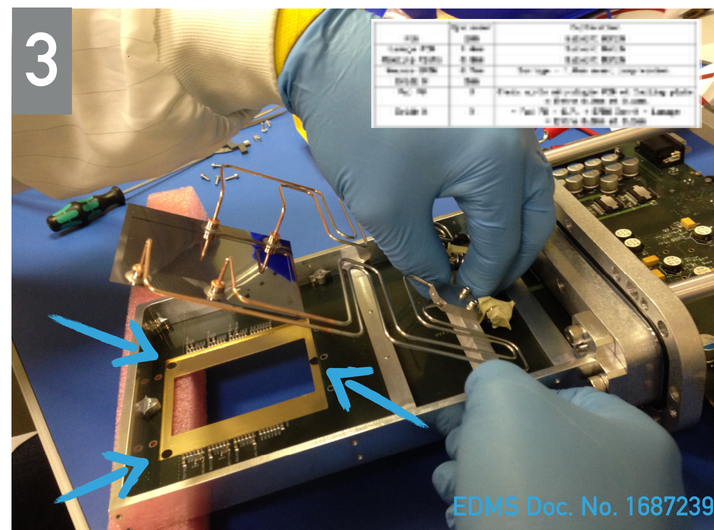


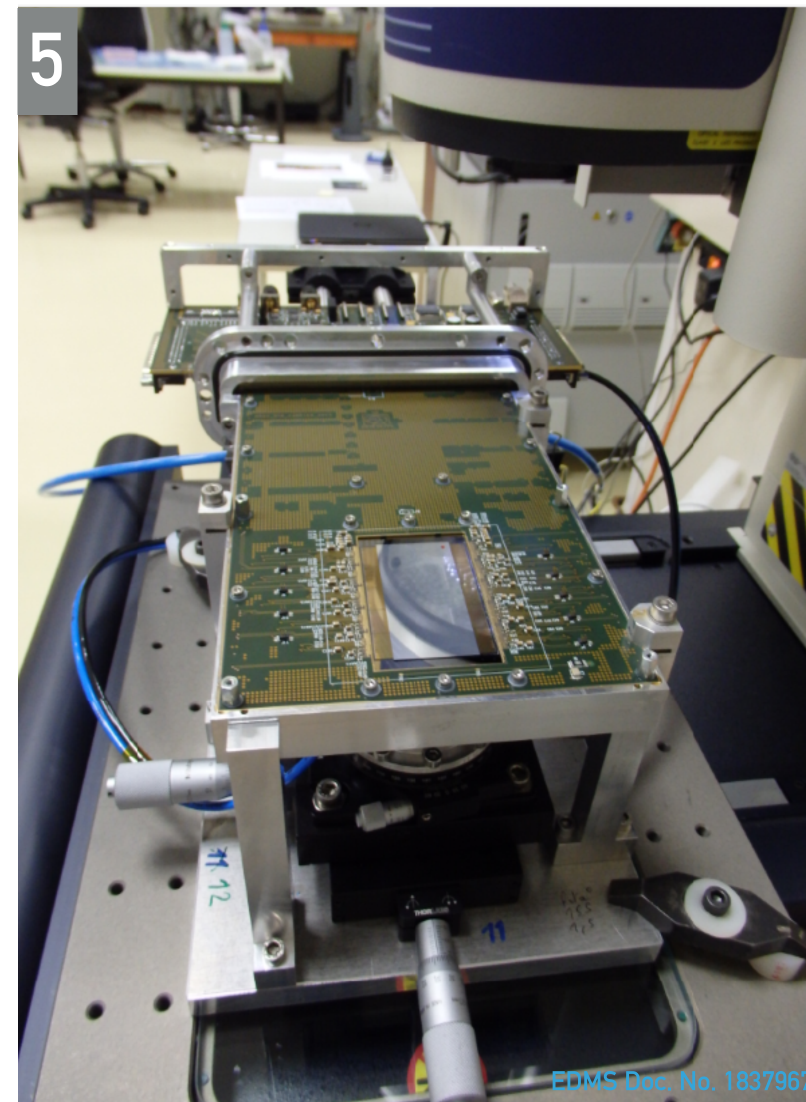


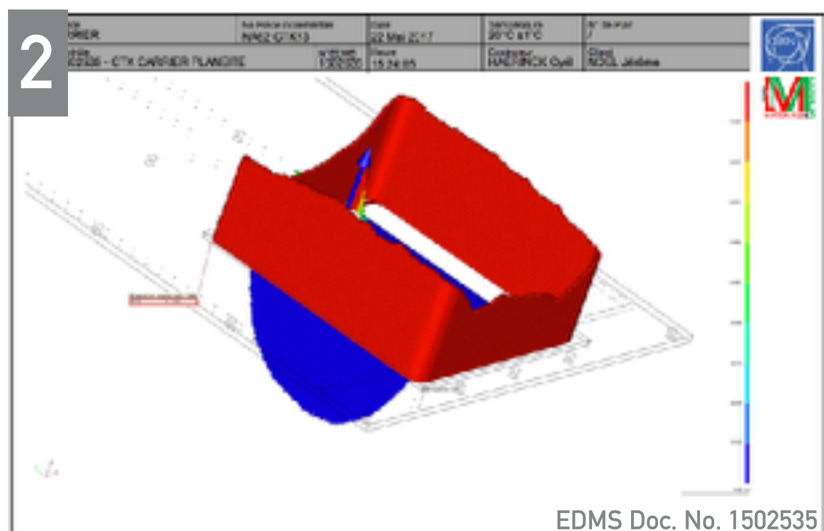


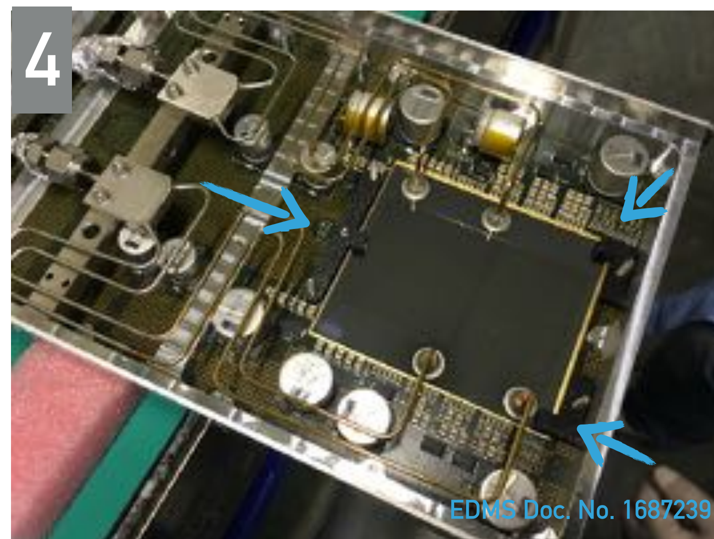
Clamping the cooling plate to the PCB





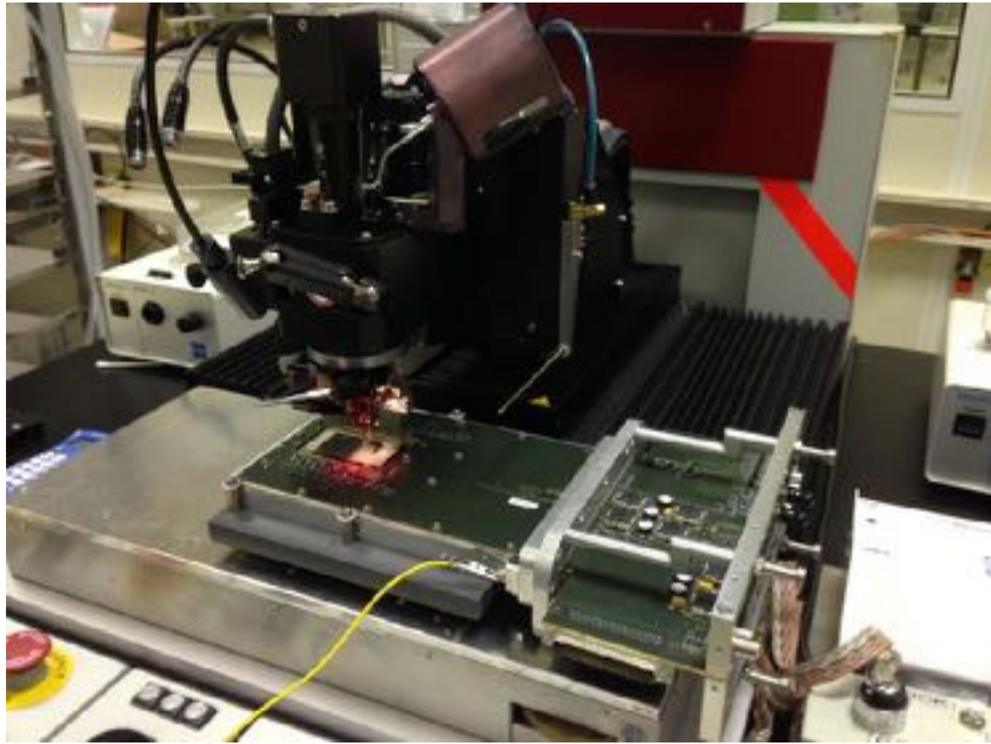




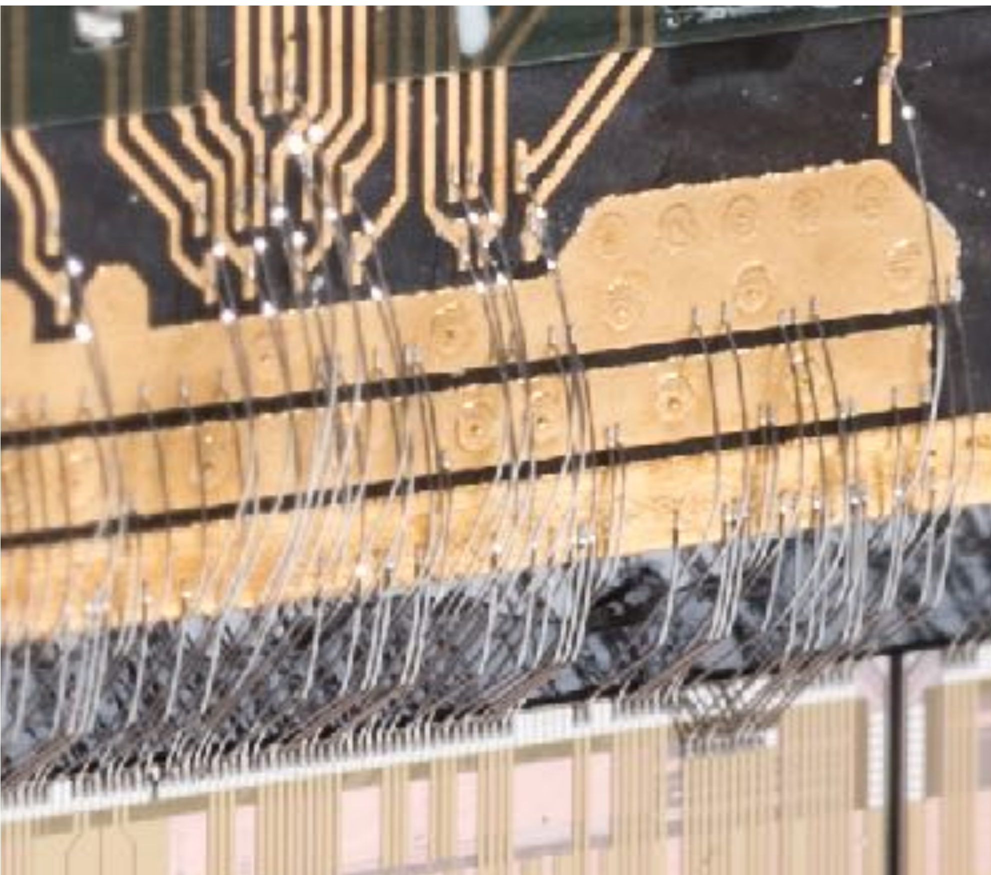


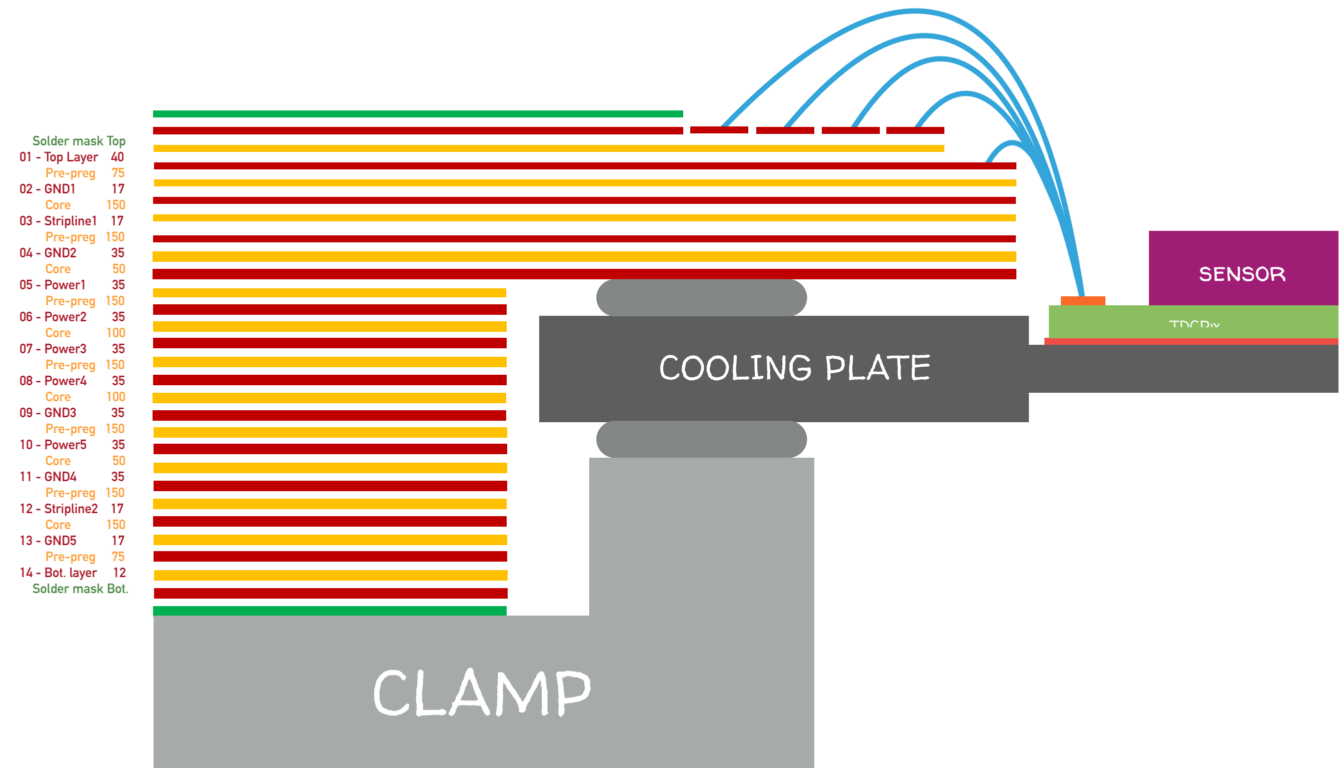
- Metrology of (1) cooling plate and (2) GTK_Carrier.
- (3) Fabrication of EPDM spacers glued to GTK_Carrier.
- (4) Fixing of cooling plate to GTK_Carrier with 3D-printed clamps.
- (5) Alignment of TDCPix pads to GTK_Carrier pads.

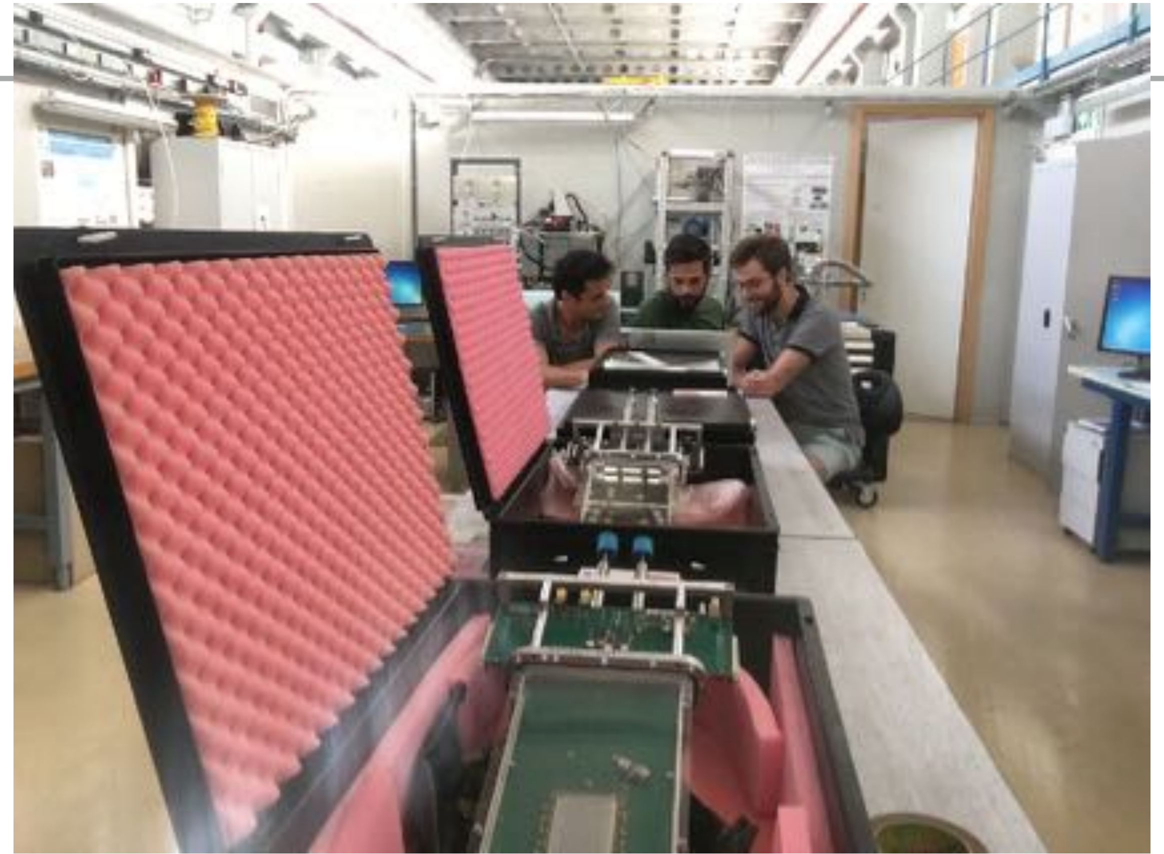
Wire-bonding

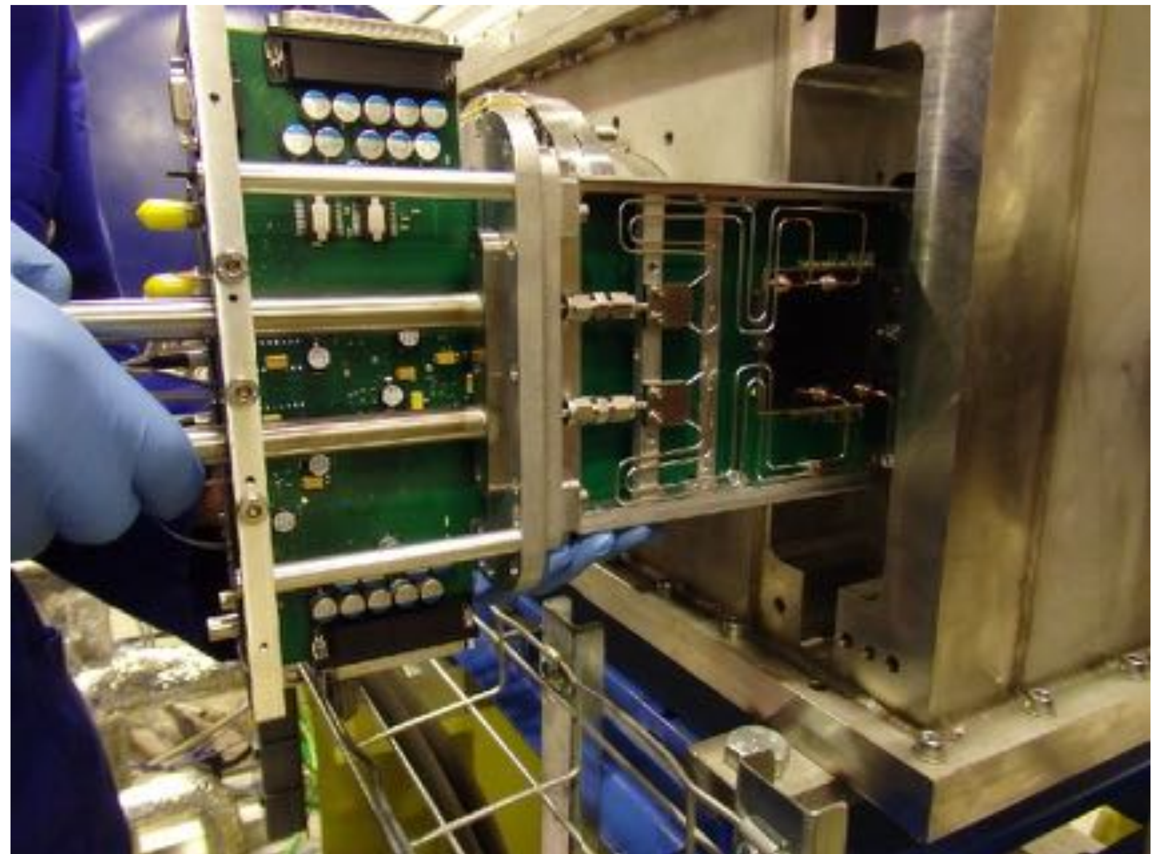


- Wire-bonding is performed at CERN
  - http://bondlab-qa.web.cern.ch/
- 18000 wire bonds per module with a pitch of 73 µm
- Height difference between PCB pads and TDCPix pads.









Summary and outlook

- 2009 - Presentation of the concept of silicon microchannel cooling for the GTK.
- 2010 - First working prototype at CERN.
- 2012 - Selection of this technology for the GTK.
- Since then, 9 silicon microchannel cooling plates have been integrated into GTK modules and used in the experiment.
- 2014 - installation of the first GTK, pioneering the use of microfluidics for the thermal management of silicon pixel detectors
- 2016 - Data taking with 3 GTK detectors.
  - Reworkability: one of the cooling plates currently installed in the beam was recycled from a previous module.
- 2017 - 6 modules are currently being assembled and tested at CERN.
- 2018 - 6 modules will be assembled in 2018 with new cooling plates and new sensors.

Talk by Ernesto MIGLIORE about the NA62 GTK on Thursday

Talk by Oscar AUGUSTO about CO2 in microchannels for the LHCb Velo upgrade next.

Relevant publications

- The NA62 Collaboration, **The beam and detector of the NA62 experiment at CERN**, 2017 JINST 12 P05025, goo.gl/LP4umG
- G. Romagnoli et al., **Silicon micro-fluidic cooling for NA62 GTK pixel detectors**, Microelec. Eng. 145 (2015) 133-137, goo.gl/VwuawR
- P. Petagna et al., **Application of micro-channel cooling to the local thermal management of detectors electronics for particle physics**, Microelec. Journal 44 (2013) 612–618, goo.gl/VRijT4
- A. Mapelli et al., **Low mass integrated cooling**, PoS(Vertex 2013)046, https://goo.gl/SUqkwJ
- A. Mapelli et al., **Low material budget microfabricated cooling devices for particle detectors and front-end electronics**, Nuclear Physics B (Proc. Suppl.) 215 (2011) 349–352, goo.gl/Kx3v4v

BACKUP

In the beam today

- currently in the beam
  - https://indico.cern.ch/event/604134/contributions/2704831/
  - Station GTK1: Module GTK_8, sensor n-in-p, CP 280 μm, TDCPix 450 μm
  - Station GTK2: Module GTK_9, sensor n-in-p, CP 380 μm, TDCPix 100 μm
  - Station GTK3: Module GTK_7, sensor n-in-p, CP 280 μm, TDCPix 100 μm

- STATION_1 - MODULE GTK_8
  - 3.3bar
  - ~3g/s
  - Tin:-14C
  - Tout:-2.5C

- STATION_2 - MODULE GTK_9
  - 4g/s
  - 3.3bar
  - Tin:-15C
  - Tout:-8.7C

- STATION_3 - MODULE GTK_7
  - 3g/s
  - 3.3bar
  - Tin:-12C
  - Tout:-1.6C

MICROFABRICATION OF ON-DETECTOR COOLING SYSTEMS

Fabrication of structures with features below the mm.
Same techniques as used for microelectronics and silicon detectors.

Novel high performance compact systems based on microfluidics.

Scintillation Particle Detectors Based on Plastic Optical Fibres and Microfluidics

THÈSE N° 5033 (2011)

PRÉSENTÉE LE 2 SEPTEMBRE 2011
À LA FACULTÉ SCIENCES ET TECHNIQUES DE L'INGÉNIEUR
LABORATOIRE DE MICROSYSTÈMES 4
PROGRAMME DOCTORAL EN MICROSYSTÈMES ET MICROÉLECTRONIQUE

ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE

POUR L'OBTENTION DU GRADE DE DOCTEUR ÈS SCIENCES

EPFL
ÉCOLE POLYTECHNIQUE FÉDÉRALE DE LAUSANNE
Suisse
2011

2. ***Detector cooling*** *(see detailed text of original propositions)*
   a. *CO_2 cooling studies for trackers (Onnela, Catinaccio)*
   b. *CO_2 cooling studies for other detectors, like crystal calorimeters (Petagna)*
   c. *Application of nano-technologies for local cooling (Petagna)*
   d. *Cooling pipework and joining techniques (Onnela, Catinaccio)*
   e. *Organisation of a workshop on detector cooling*

Silicon microchannel cooling

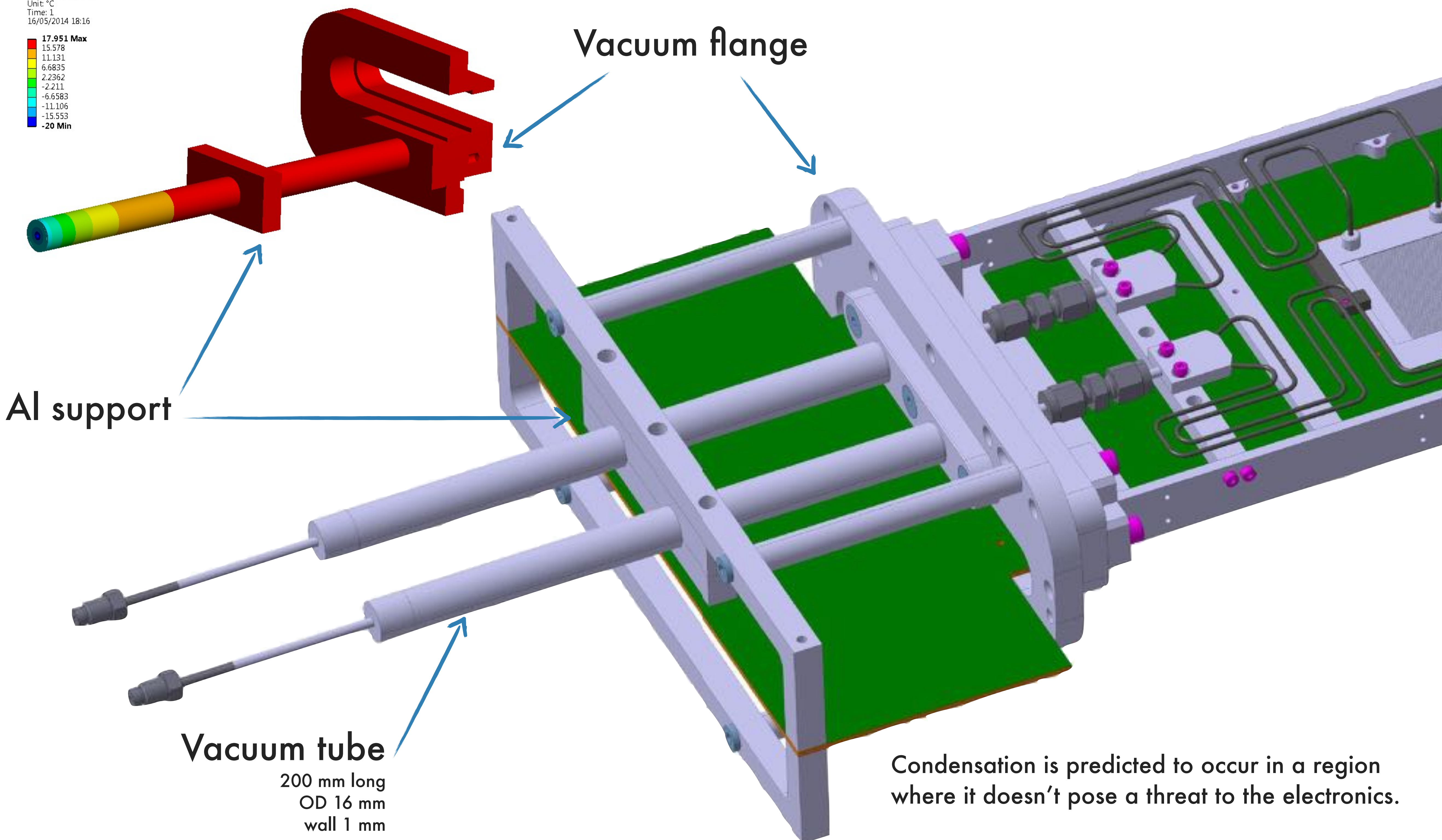
J. Buytaert, A. Catinaccio, J. Daguin, R. Dumps, K. Howell, A. Kluge, A. Mapelli, M. Morel, J. Noel,
G. Nuessle, P. Petagna, Ph. Renaud (EPFL), G. Romagnoli, J. Thome (EPFL)

PROCEEDINGS SUPPLEMENTS
...ics B (Proc. Suppl.) 215 (2011) 349–352
www.elsevier.com/locate/npbps

Low material budget microfabricated cooling devices for particle detectors and front-end electronics

A. Mapelli[a b] *, A. Catinaccio[a], J. Daguin[a], H. van Lintel[b], G.Nuessle[c], P. Petagna[a], P. Renaud[b],
[a]Physics Department, CERN, Geneva, Switzerland
[b]Laboratoire de Microsystèmes, Ecole Polytechnique Fédérale de Lausanne, Switzerland
[c]CP3, Université catholique de Louvain, Louvain-la-Neuve, Belgique

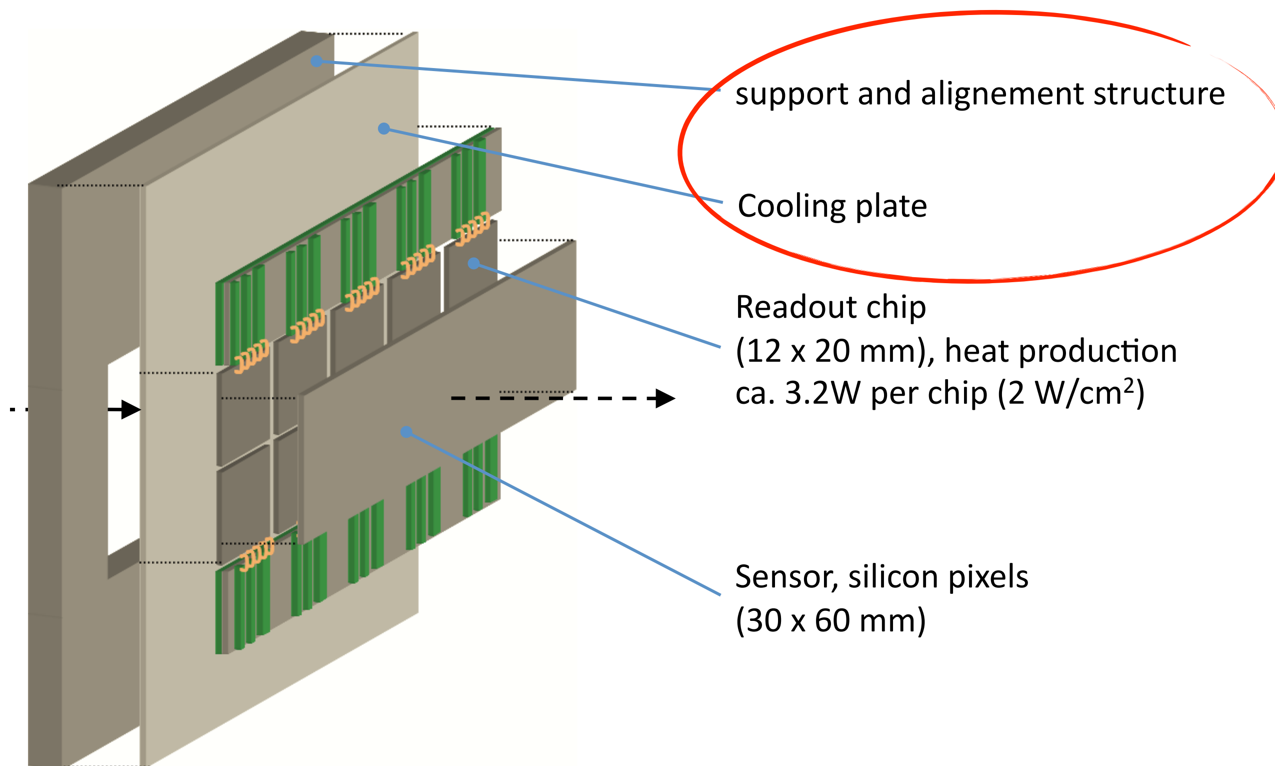
vacuum insulation of cooling capillaries out of the vessel

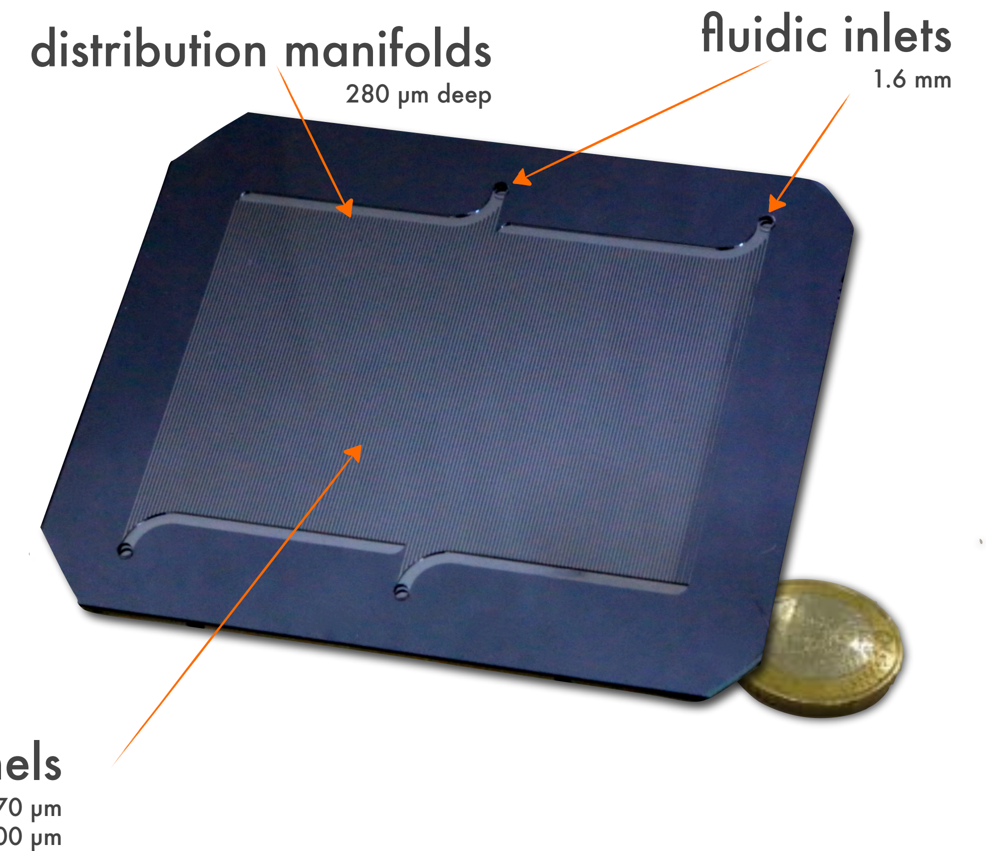


Condensation is predicted to occur in a region where it doesn't pose a threat to the electronics.

silicon microchannel cooling plate

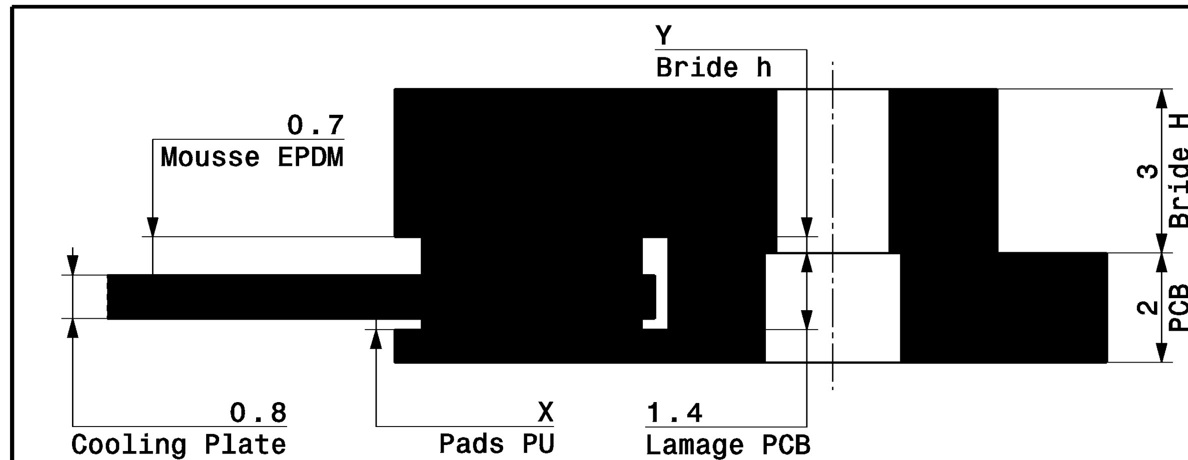
- The GTK pixel detectors are the first HEP detectors to be cooled with silicon microchannels.
- Each GTK station is made of one hybrid silicon pixel detector (29.3 mm x 63.1 mm with 18000 pixels 300 µm x 300 µm) flip-chip bonded to 10 ASIC front-end chips TDCPix.
- 2009 - concept of micro-cooling for the GTK presented to NA62: https://indico.cern.ch/event/58370/
- 2014 - First GTK in the experiment
- 2016 - Data taking with 3 GTK detectors
- 2017 - Assembly of 6 GTK modules for 2018



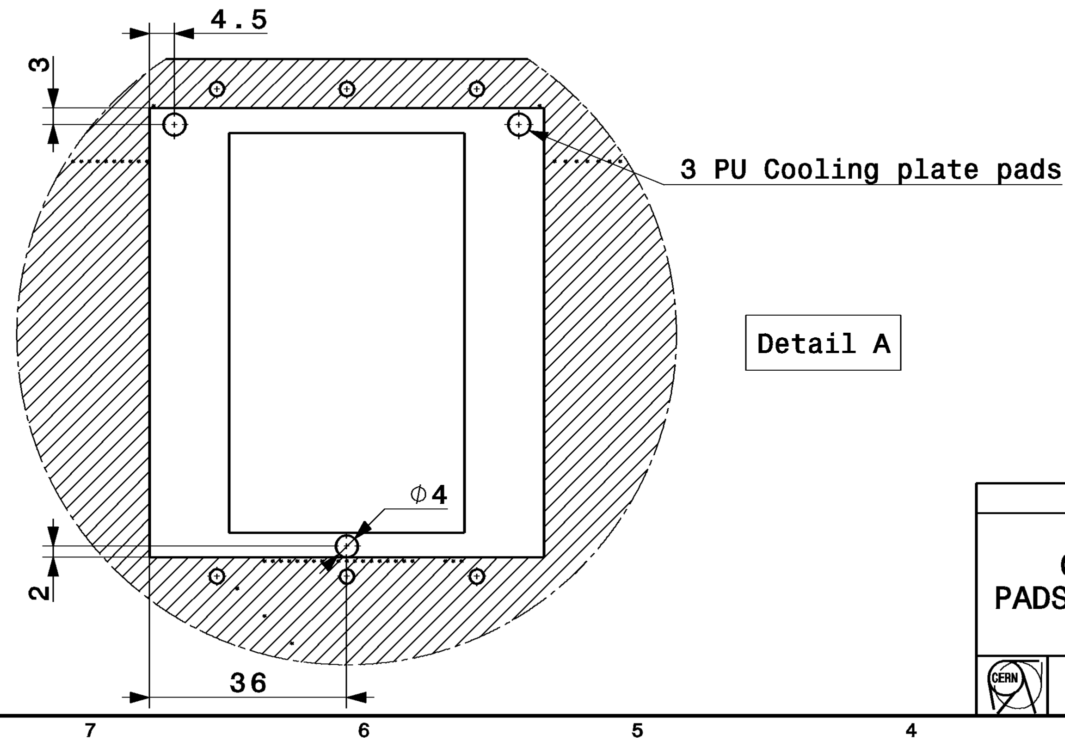


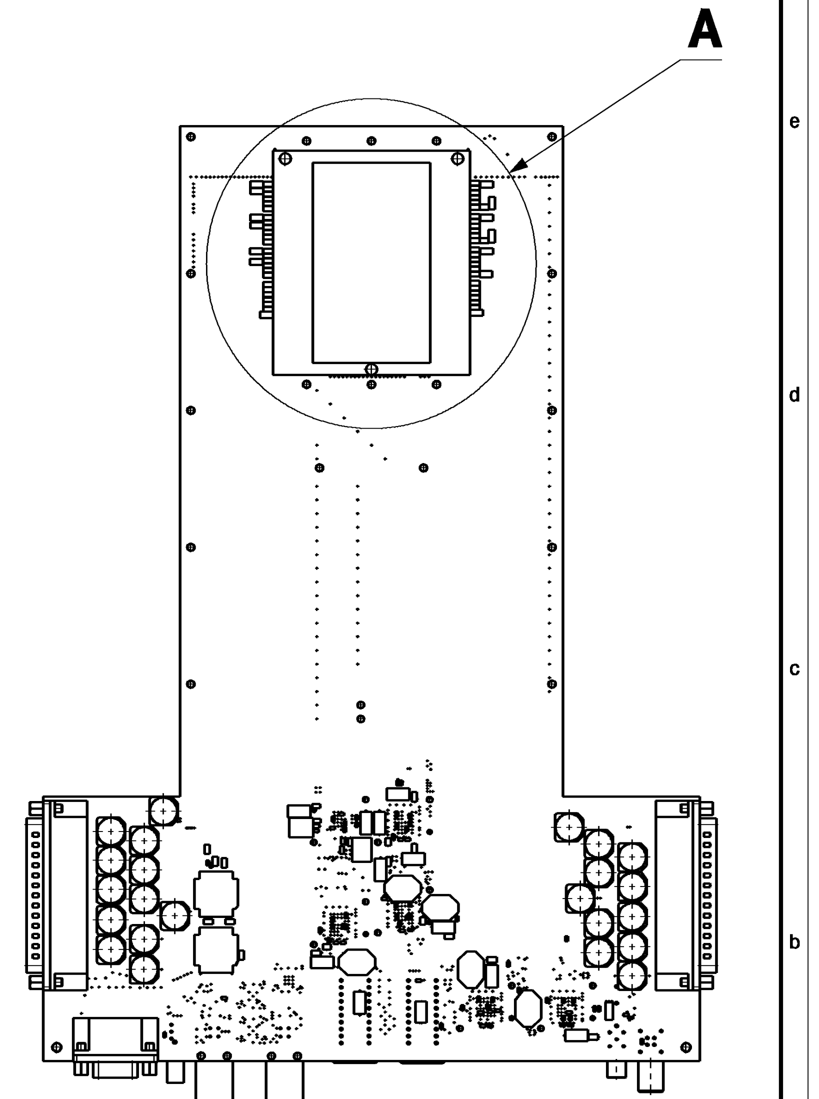
A. Mapelli et al. 2012 JINST 7 C01111
P. Petagna et al., Microelec. Journal 44 (2013) 612–618
G. Romagnoli et al., Microelec. Eng. 145 (2015) 133-137

Clamping the sensor to the PCB



	Epaisseur	Explication
PCB	2mm	Suivant Batch
Lamage PCB	1.4mm	Suivant Batch
Cooling Plate	0.8mm	Suivant Batch
Mousse EPDM	0.7mm	Serrage - 1.6mm avant compression.
Bride H	3mm	
Pad PU	X	Choix après métrologie PCB et Cooling plate = Entre 0.2mm et 0.4mm.
Bride h	Y	= Pad PU + C.P. + EPDM Serré - Lamage = Entre 0.3mm et 0.5mm





DESSIN, RUGOSITE, TOLERANCES SELON NORMES ISO
DRAWING, RUGOSITY, TOLERANCES ACCORDING TO ISO STANDARDS
PROJECTION

ORGANISATION EUROPEENNE POUR LA RECHERCHE NUCLEAIRE
EUROPEAN ORGANIZATION FOR NUCLEAR RESEARCH
GENEVE

Ce dessin ne peut être utilisé à des fins commerciales sans autorisation écrite
This drawing may not be used for commercial purposes without written authorisation

NA62 Experiment - GigaTracKer - Module

GTK CARRIER ASSEMBLY
PADS & CLAMPS DIMENSIONNING

SCALE	1:1

DES/DRA.	J.DEGRANGE	2016-05-13
CONTROLLED	-	-
RELEASED	J.NOEL	2016-05-17
APPROVED		

CAD Document Number ST0546962_03

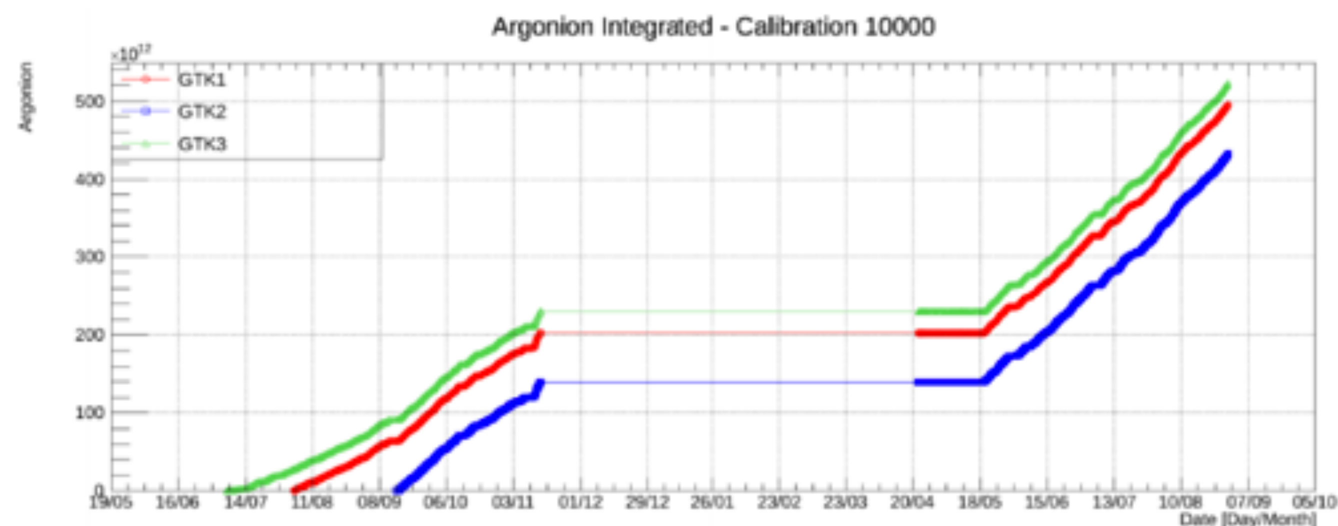
REPLACES

RELEASED BY DESIGN OFFICE | FOR INFORMATION | QAC - | N62GTMOD0034 | SIZE 3 | IND.

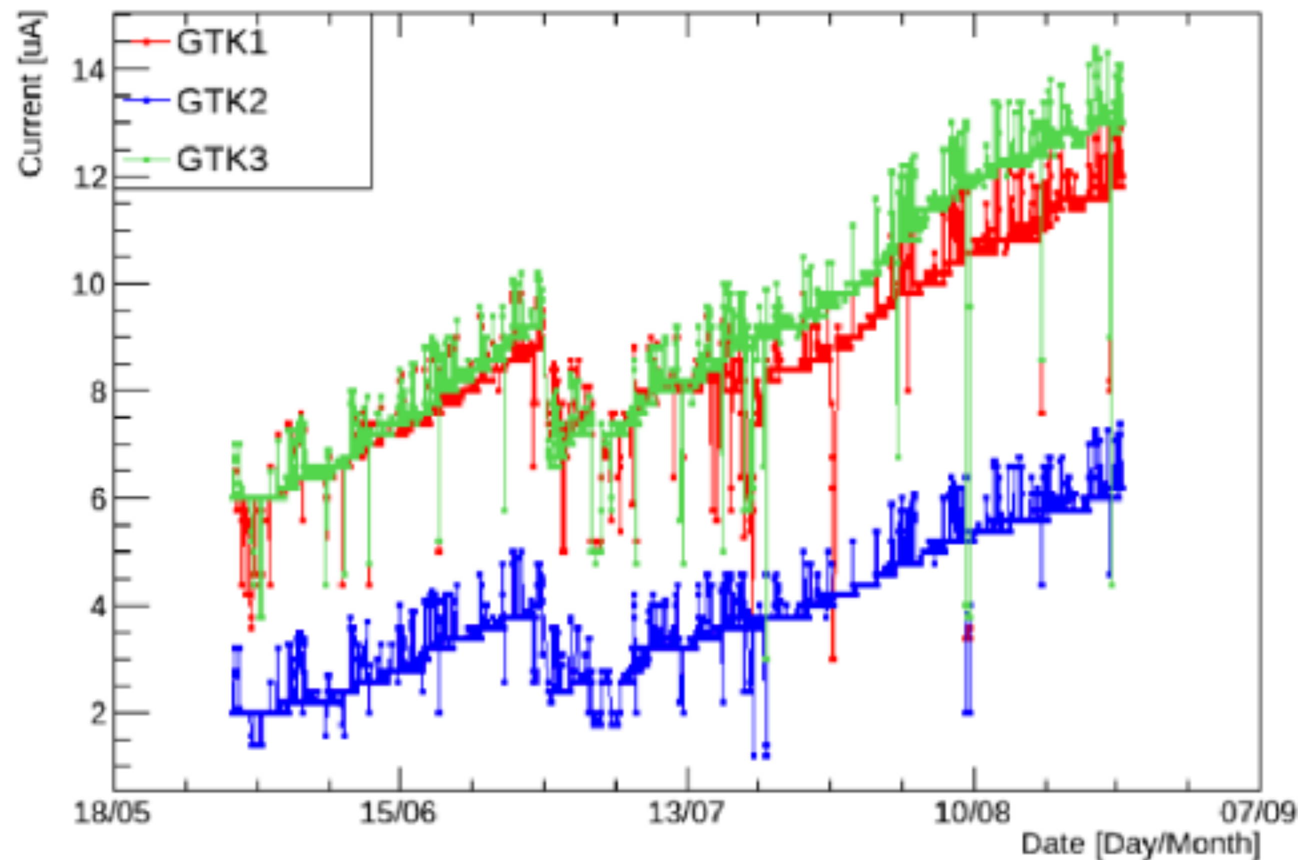
7 6 5 4 3 2 1

e d c b a

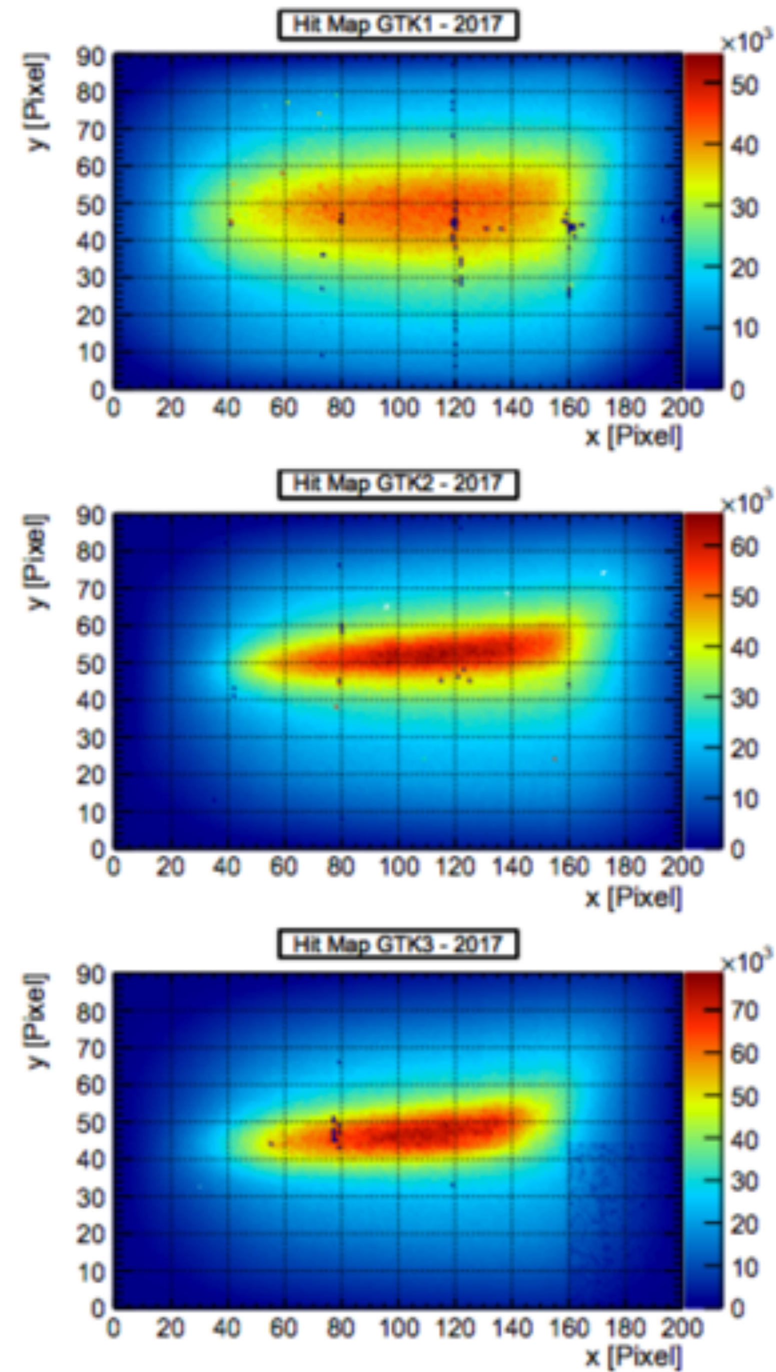
dose on GTK and leakage current at 100 V



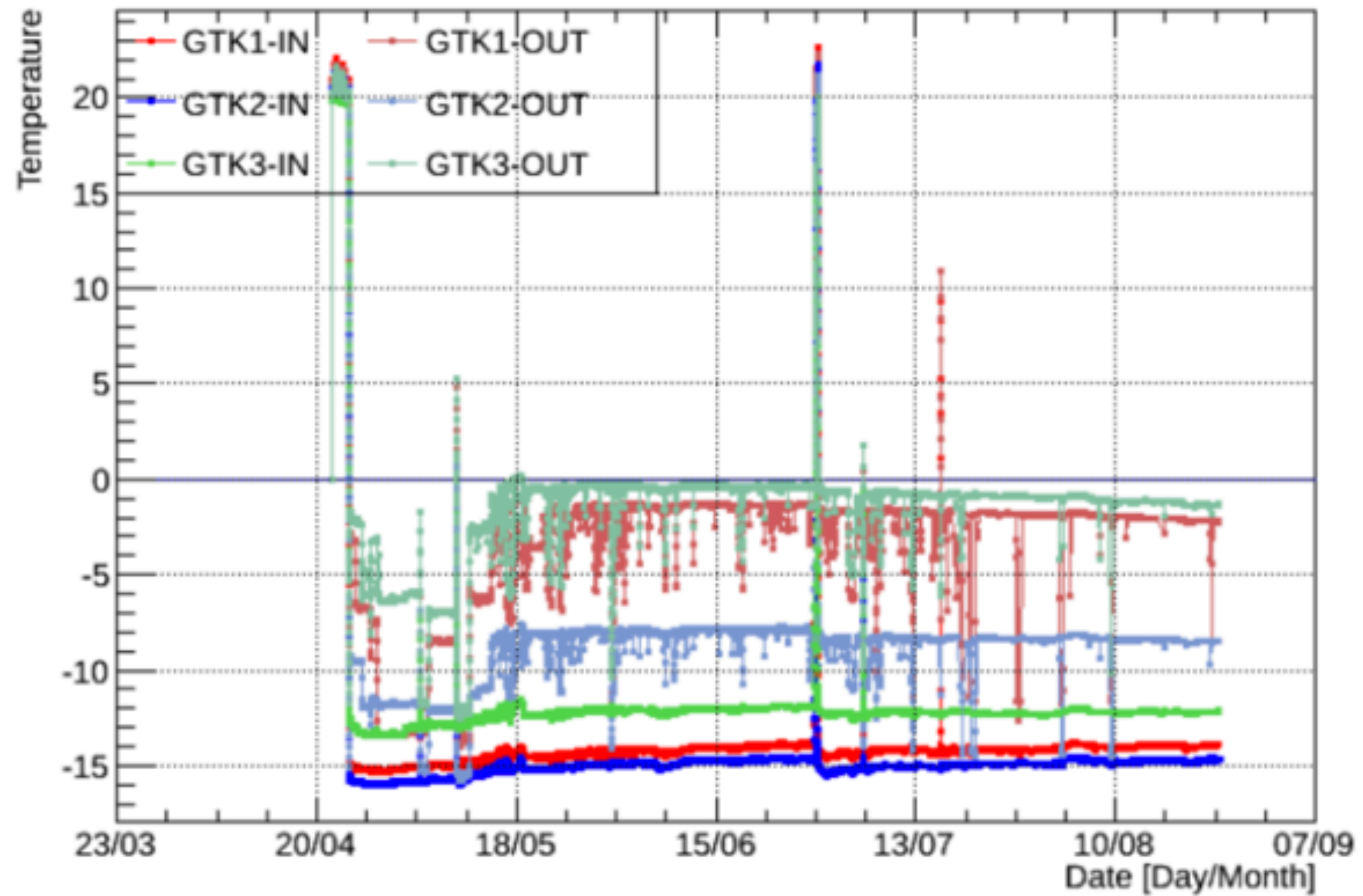
Total Integrated Argonion	5×10^{14}
Total Integrated Average Dose	0.7 MRad
Total Integrated Peak Dose	3.5 MRad
	1/2 a nominal year



hit maps of GTKs



cooling plant



silicon thermal mockups

HEATER
MICROCHANNEL
RESISTIVE TEMPERATURE DETECTOR
MICROFLUIDIC INLET
MICROFLUIDIC OUTLET
INLET CAPILLARY
OUTLET MANIFOLD
SOLDERING PAD
SOLDERING PAD

- Test complex silicon microchannel layouts in the new CO_2 test setup at CERN.

CO_2 TEST SETUP AT CERN

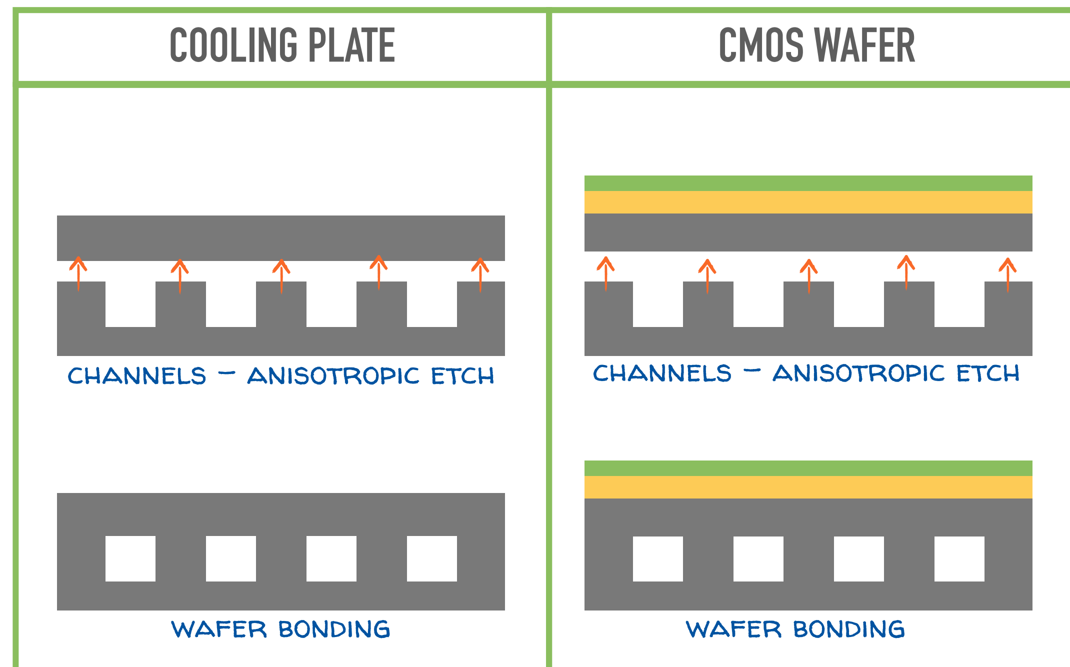
- Controlled CO_2 recirculation cooling unit
- Test setup fully under vacuum
- Temperature and pressure measurements
- High speed camera for flow visualization
- Infrared camera for thermal visualization
- Deliverable of Task 9.2 due in October 2017 - on schedule.

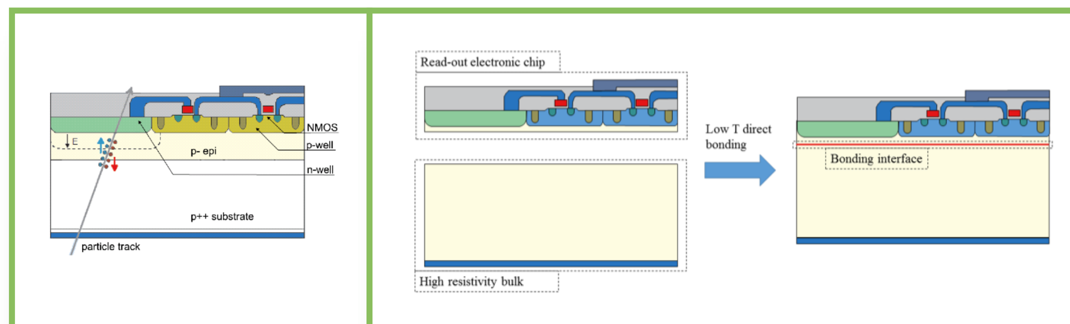
- Study boiling at the microscale level in simple single channels and tubes.
  - Glass, Stainless Steel, Titanium, Silicon
  - Round ID: 0.1 – 1.0 mm
  - Square Dh: 0.1 - 0.8 mm
- Test complex microchannel layouts in silicon substrates designed for HEP experiments.

INTEGRATING MICROCHANNELS ON PIXEL DETECTORS

"LOW TEMPERATURE" WAFER BONDING
CEA-Leti, EPFL, G-Ray

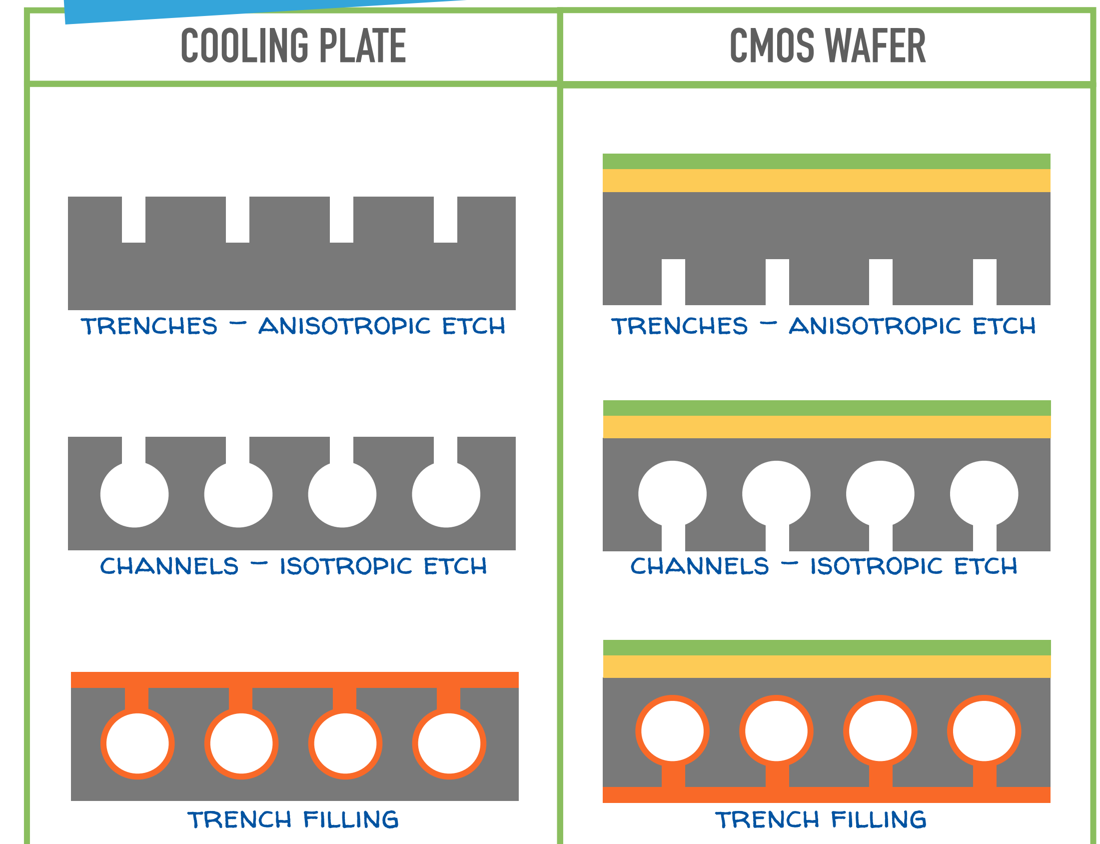
Jacopo BRONUZZI, PhD EPFL, 2018

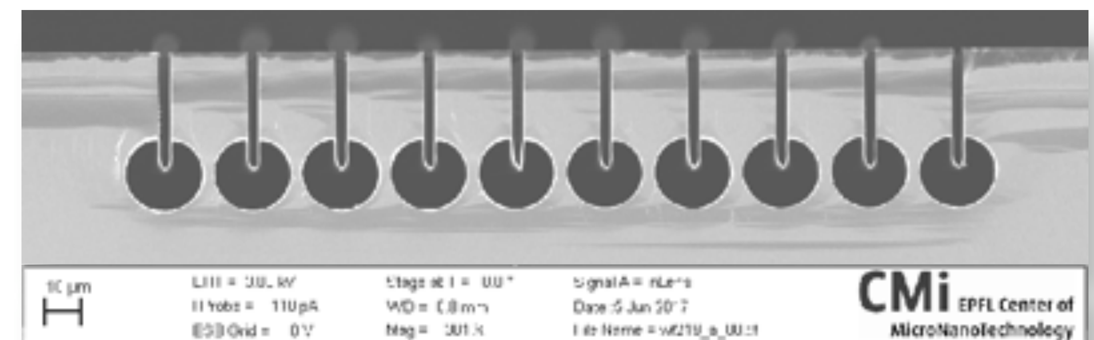




BURIED CHANNELS
EPFL, FBK

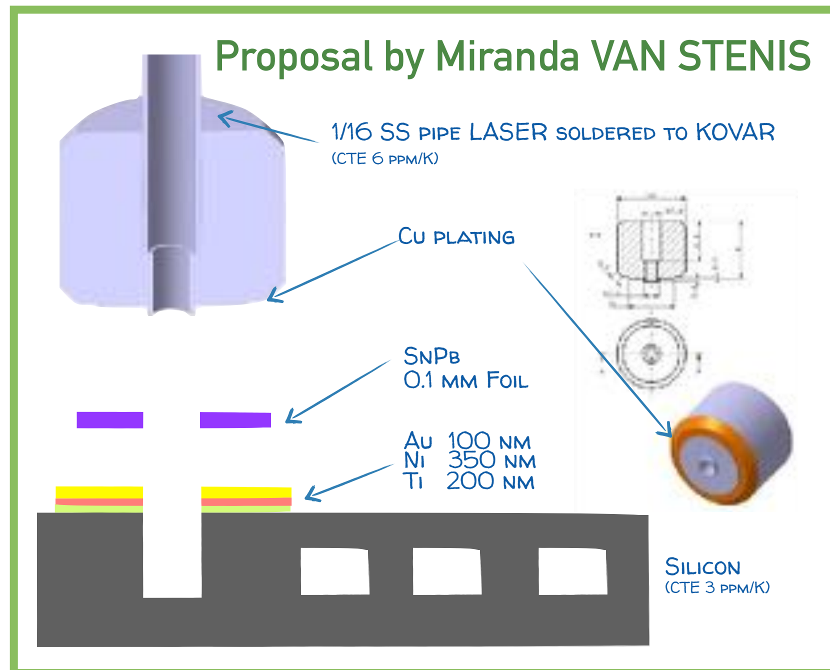
Clémentine LIPP, MSc EPFL, 2017

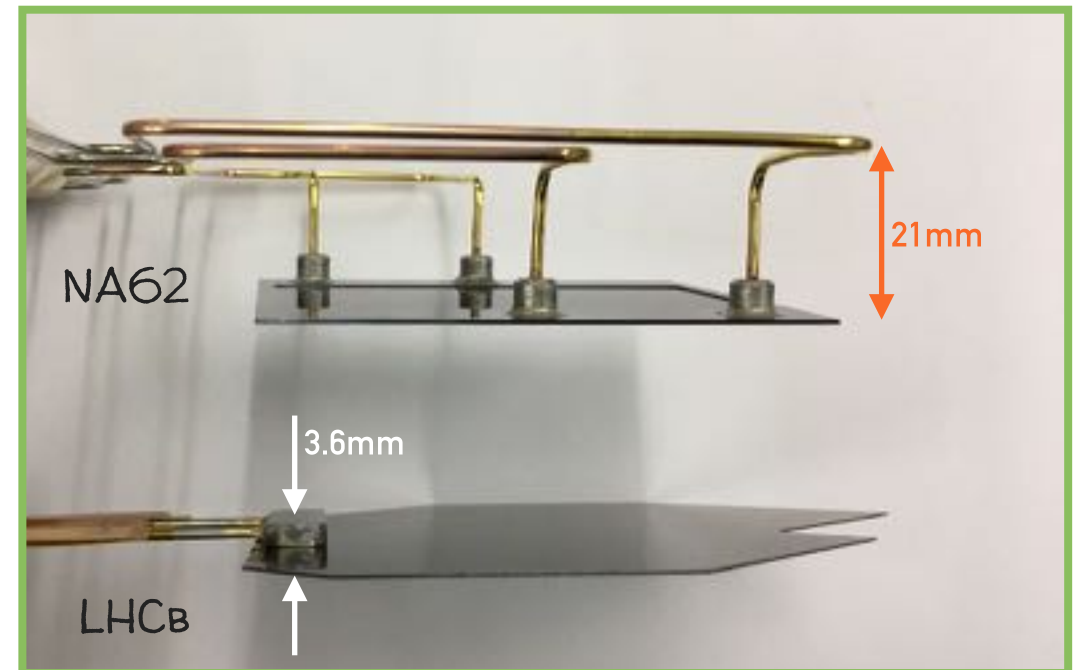


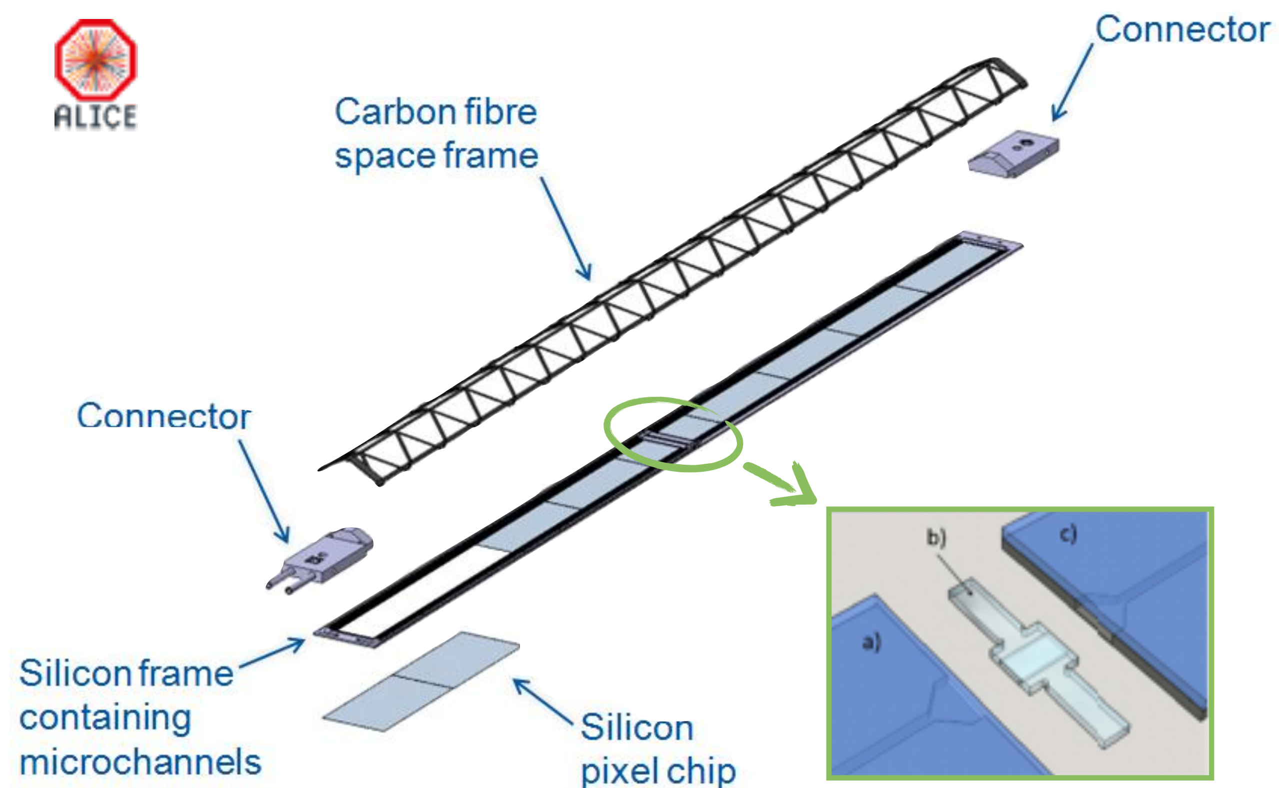


- Tests ongoing with blank wafers
- **Embed microchannels** on the backside of CMOS wafers, tests later this year.

INTERCONNECTIVITY – DAISY CHAINING MICROFLUIDICS







See Corrado GARGIULO's talk.

- NA62 and LHCb cooling plates
  - limited surfaces
  - access from the side
- For **larger systems** we need in-plane **interconnections**.