Commissioning and first results from the CMS phase-1 upgrade pixel detector

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on behalf of the pixel upgrade team

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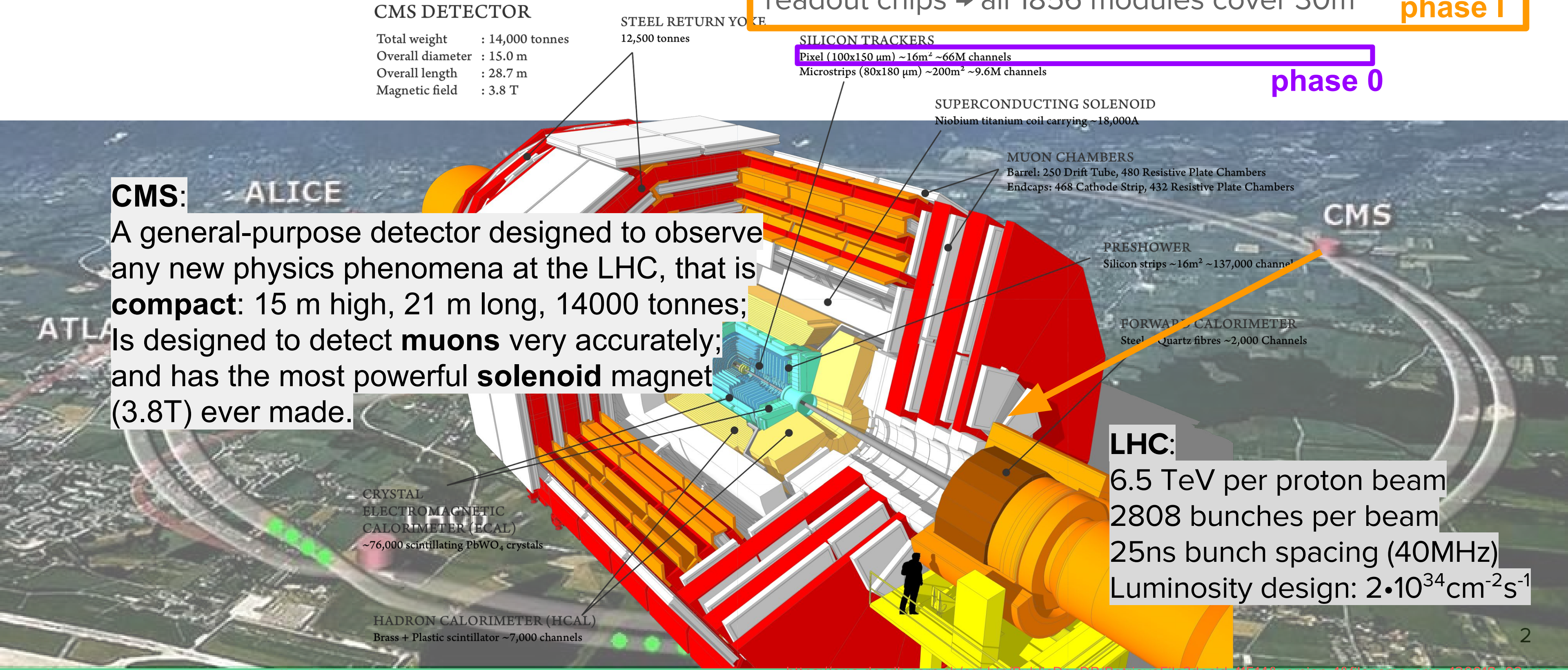
http://www.physik.uzh.ch/dam/jcr:ac888487-cd67-4e6f-b8e8-f5daffb43a39/CMSnew.jpg

CMS
Compact Muon Solenoid

Compact Muon Solenoid

124 million pixel channels (87.7% more pixels compared to the previous system)
n+ in n sensors with 66560 pixels of size 100x150 μm^2
Total active area 16.2 x 64.8 mm^2 covered with 16 readout chips ➔ all 1856 modules cover 30m^2 **phase I**



CMS:
A general-purpose detector designed to observe any new physics phenomena at the LHC, that is **compact**: 15 m high, 21 m long, 14000 tonnes;
Is designed to detect **muons** very accurately;
and has the most powerful **solenoid** magnet (3.8T) ever made.

LHC:
6.5 TeV per proton beam
2808 bunches per beam
25ns bunch spacing (40MHz)
Luminosity design: $2 \cdot 10^{34} cm^{-2} s^{-1}$

http://sites.uci.edu/energyobserver/files/2012/11/lhc-aerial.jpg
https://cms-docdb.cern.ch/cgi-bin/PublicDocDB/RetrieveFile?docid=11514&version=1&filename=cms_120918_03.png

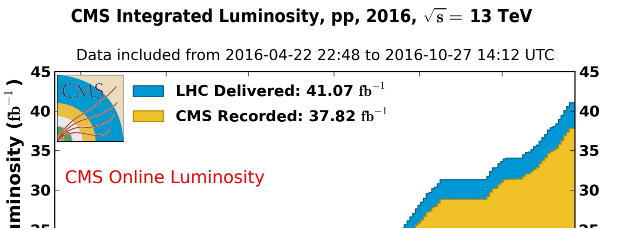
New CMS Phase I Pixel detector

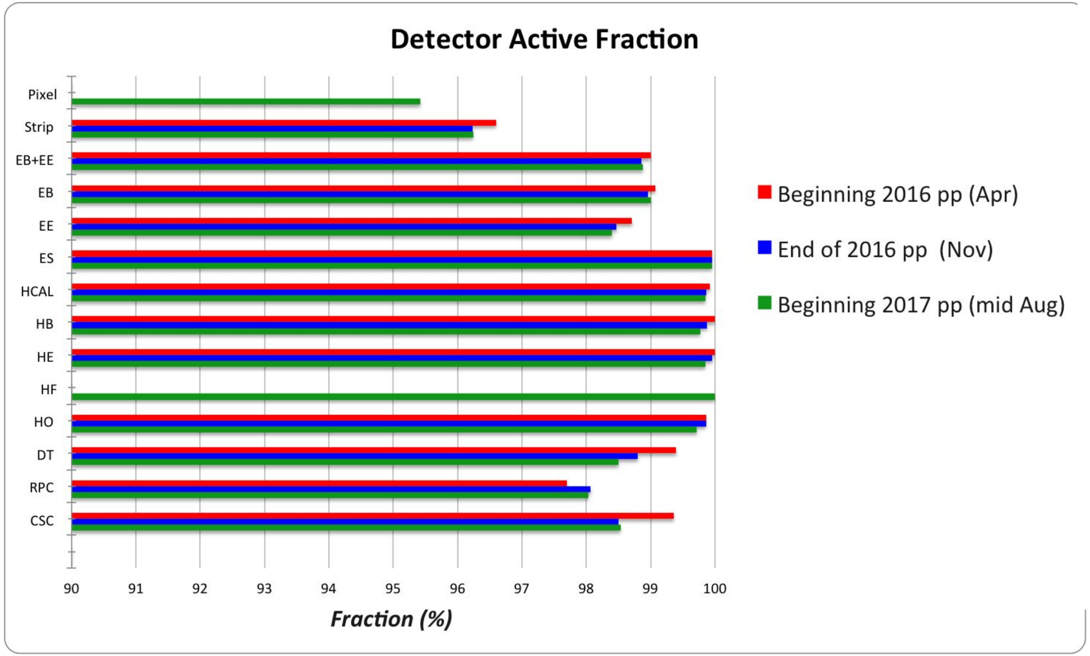
	Phase 0	Phase I
disks per forward pixel detector	2	**3**
layers per barrel pixel detector	3	**4**
readout	40MHz analog	**160 Mbit digital**
For luminosities (lumi) up to:	$1.53 \cdot 10^{33} cm^{-2} s^{-1}$ (peak lumi)	$2 \cdot 10^{34} cm^{-2} s^{-1}$
Backend	VME(Versa Module Europa)-based	**micro-TCA**(Telecommunications Computing Architecture)-based
Cooling	Single-phase C_6F_{14} cooling	**Two-phase CO_2**: reduced material budget
Channels	~66 million channels	**124 million pixel channels: 87.7% more pixels** compared to the previous system

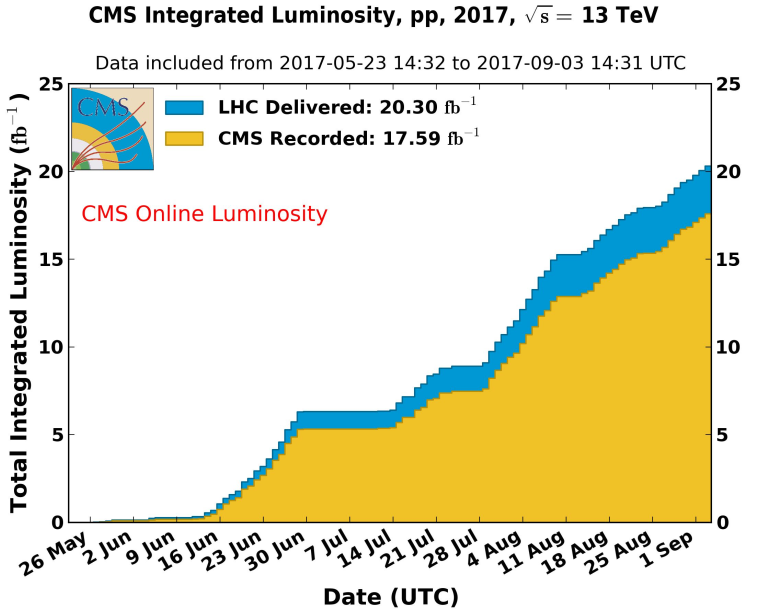
http://v-cuplov.net/wp-content/uploads/2011/07/silicon_pixel_detector.jpg

Peak lumi: https://cms-service-lumi.web.cern.ch/cms-service-lumi/publicplots/peak_lumi_per_day_pp_2016.png

CMS and LHC Performance







https://cms-service-lumi.web.cern.ch/cms-service-lumi/publicplots/int_lumi_per_day_cumulative_pp_2017OnlineLumi.png

https://twiki.cern.ch/twiki/pub/CMSPublic/HLTplotsEPS2017/_imge432a984a497f158f5656d8b466a88b6.jpeg

Pixel Phase I detector timeline 2017

First global run

PIXEL	IN	Running
TRACKER	IN	Running

Installation: 28/2 → 08/3

Checkout → 25/3

Calibrations → 18/4

B=3.8T

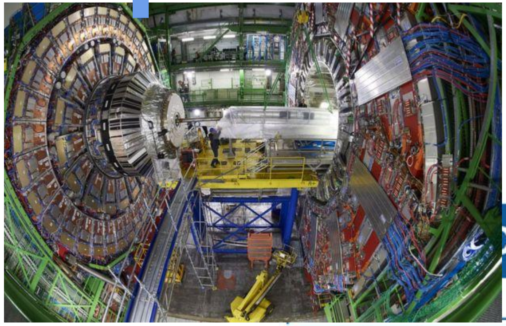
Cosmics → 23/5

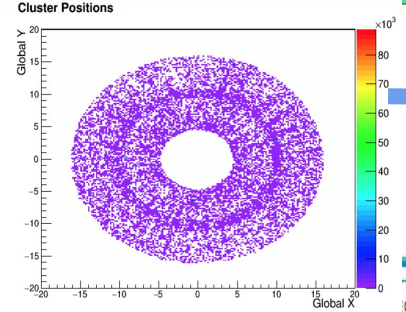
First stable beam: LHC fill 5698

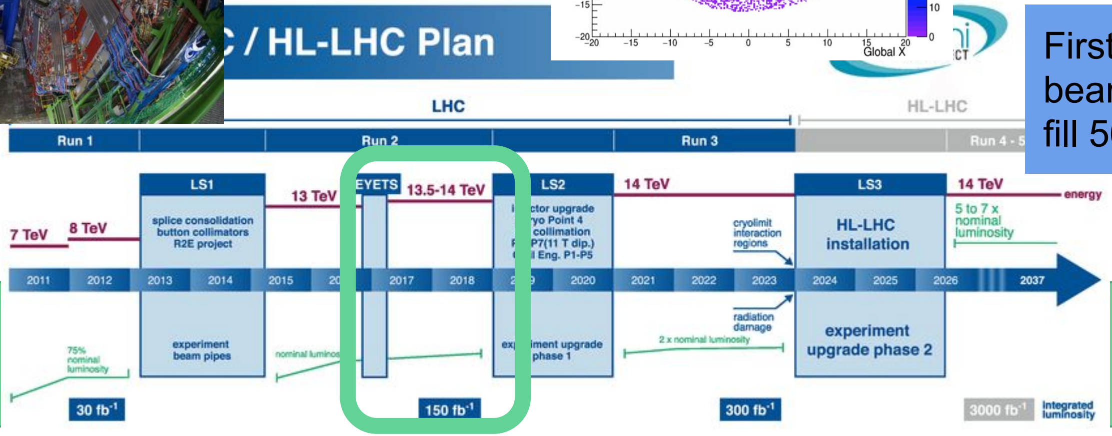
Physics → 23/5

Up to LS2

https://ichef-1.bbci.co.uk/news/624/cpsprodpb/3AC0/production/_94904051_cms2.jpg

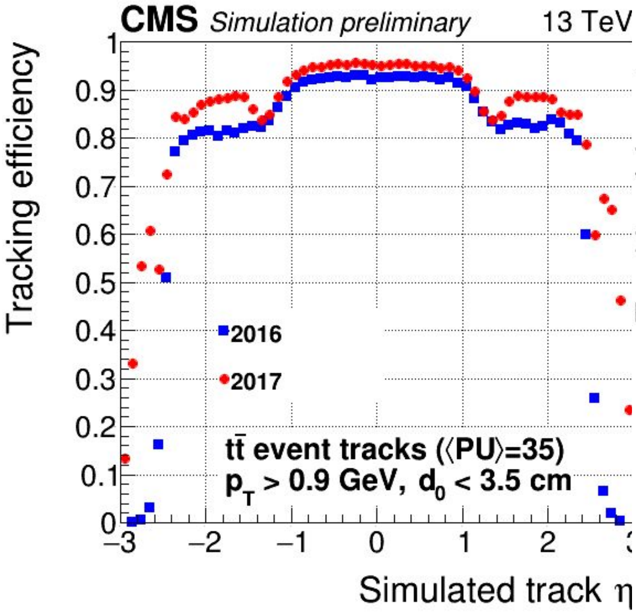


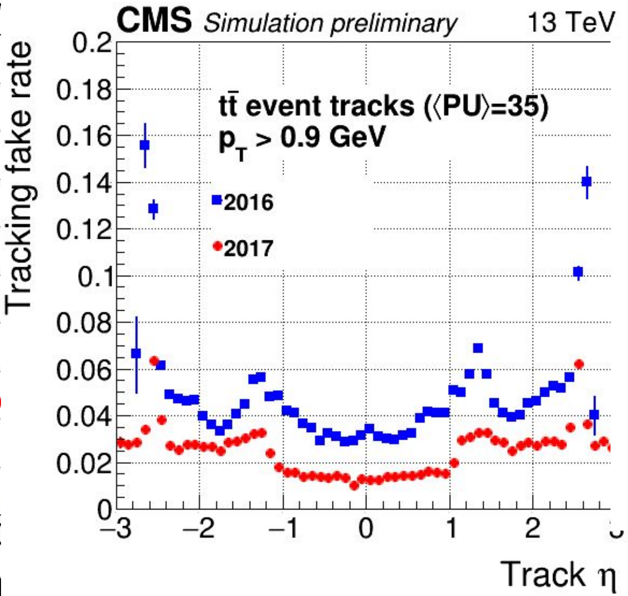


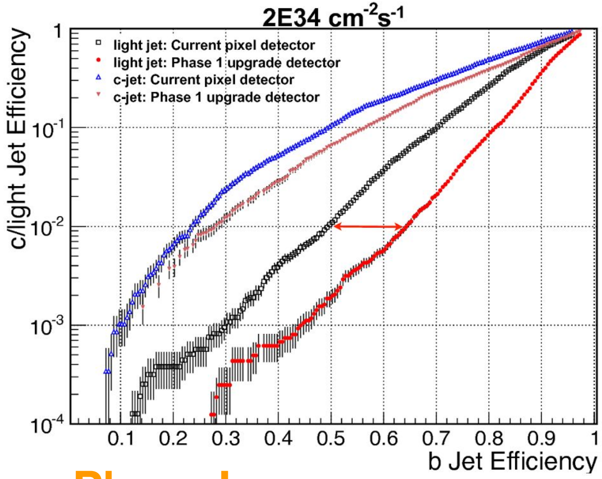


https://www.researchgate.net/publication/316498879/figure/fig1/AS:488254857322496@1493420437934/Figure-1-The-expected-roadmap-towards-High-Luminosity-LHC-1.ppm

CMS phase I pixel detector expected performance







Phase I

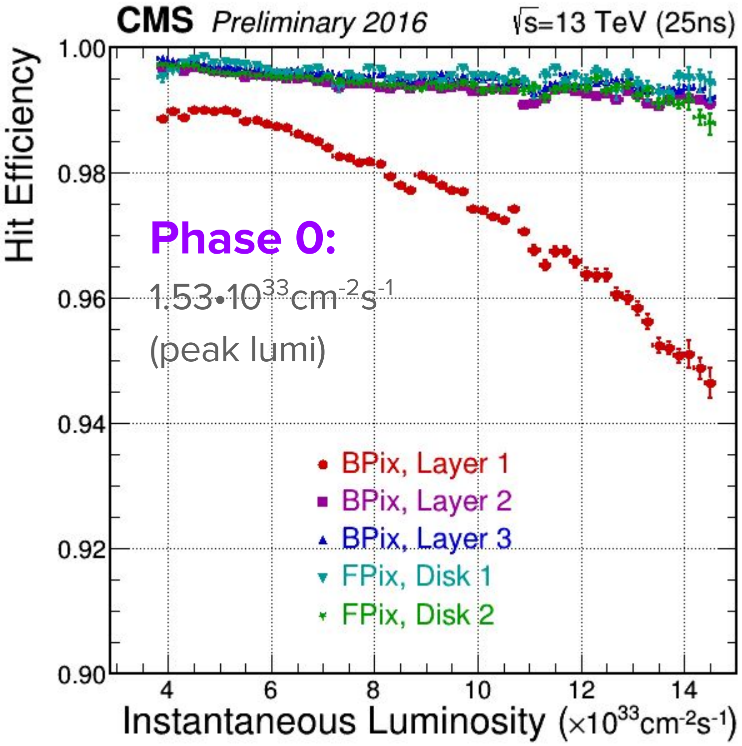
expected

$2 \cdot 10^{34} cm^{-2} s^{-1}$

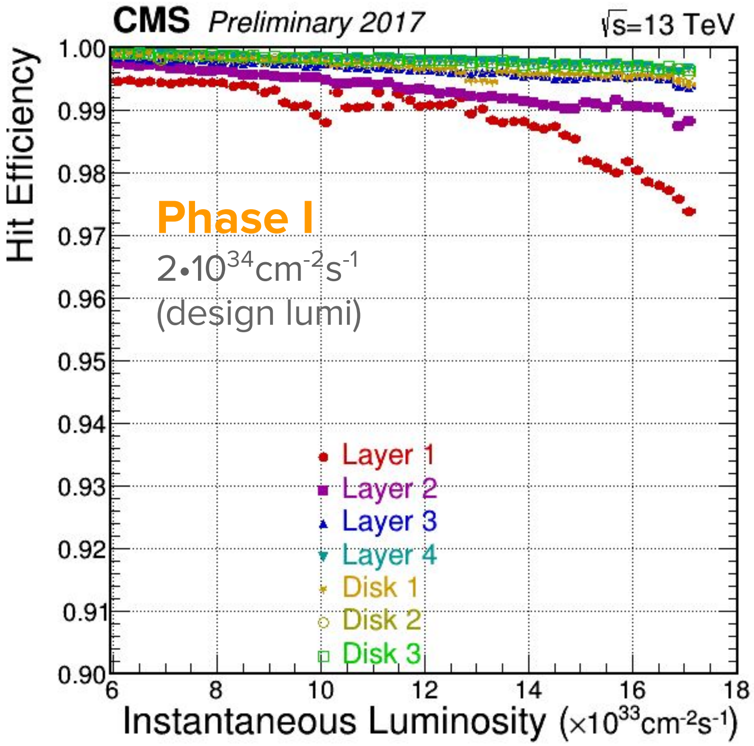
https://twiki.cern.ch/twiki/pub/CMSPublic/TrackingPOGPerformance2017MC

CMS TDR http://cds.cern.ch/record/1481838

CMS phase I pixel detector efficiency



Phase 0:
$1.53 \cdot 10^{33} cm^{-2}s^{-1}$
(peak lumi)

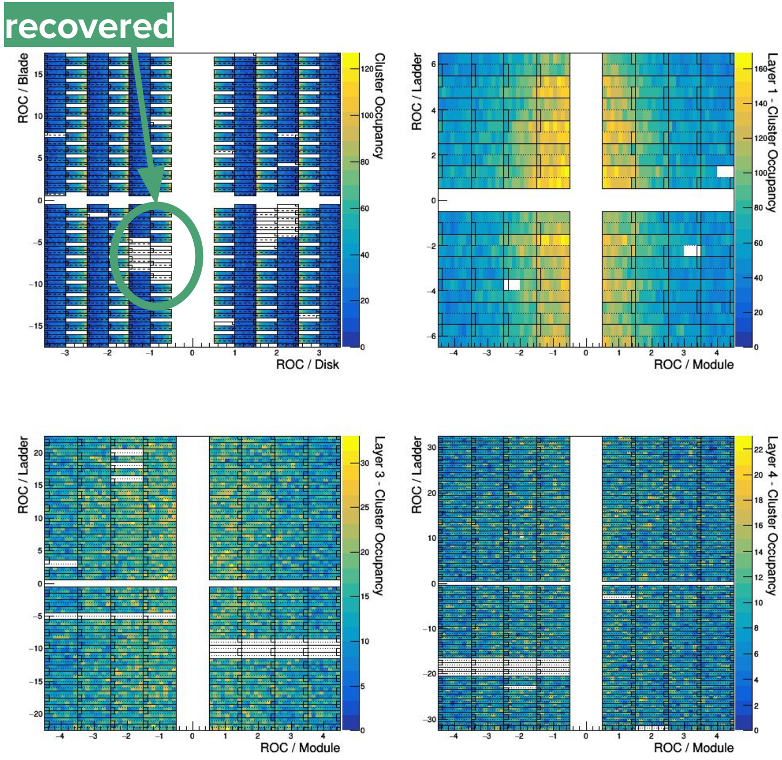


Phase I
$2 \cdot 10^{34} cm^{-2}s^{-1}$
(design lumi)

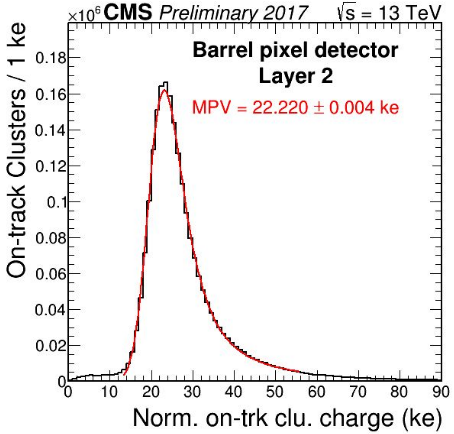
https://twiki.cern.ch/twiki/pub//CMS/PixelOfflinePlotsAugust2017/HitEfficiency_vs_InstLumi_LayersDisks_2017Data.png

https://twiki.cern.ch/twiki/pub/CMSPublic/PixelOfflinePlots2016/HitEfficiency_vs_InstLumi_LayersDisks_2016Data_Update.png

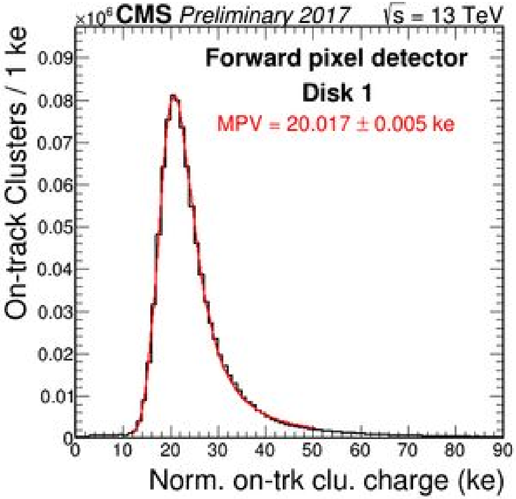
CMS phase I pixel detector performance



https://twiki.cern.ch/twiki/pub//CMSPublic/PixelOfflinePlots2017/SiPixelQuality-run297099.png



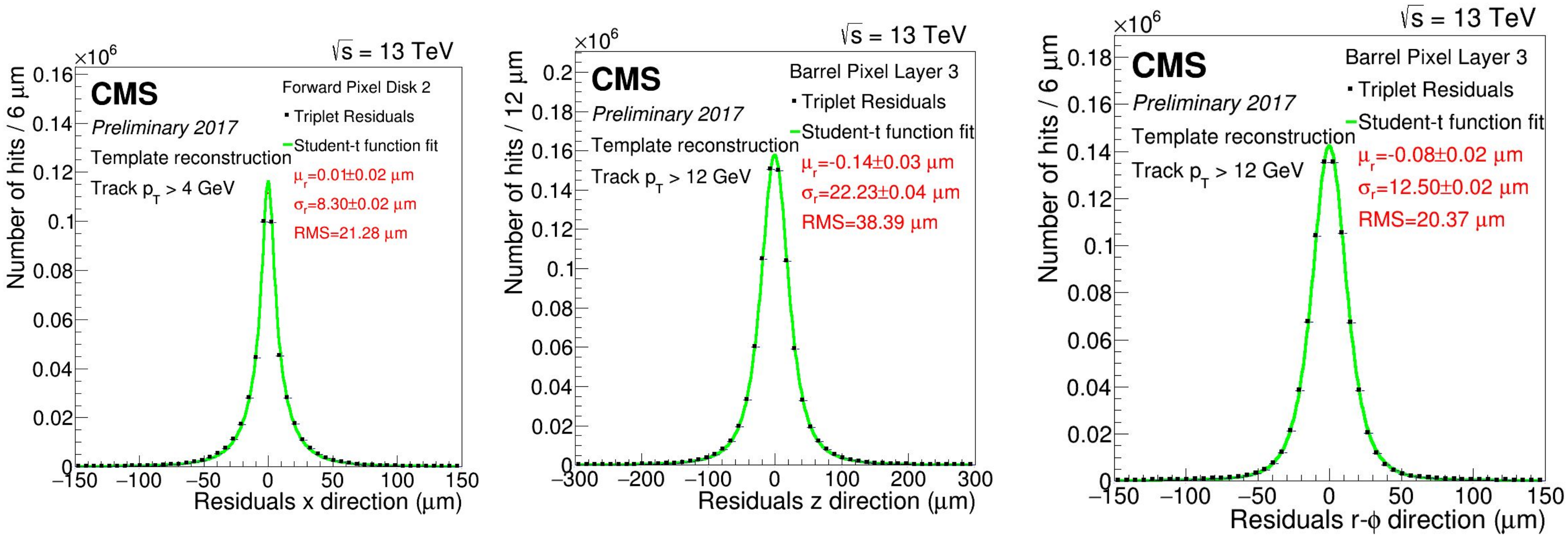
https://twiki.cern.ch/twiki/pub//CMSPublic/PixelOfflinePlots2017/OnCluChargeNorm_Lay2Phase1.png



https://twiki.cern.ch/twiki/pub/CMSPublic/PixelOfflinePlots2017/_300___OnCluChargeNorm_Diskp1Phase1.png

See talk by Viktor Veszpremi on tracking performance and alignment

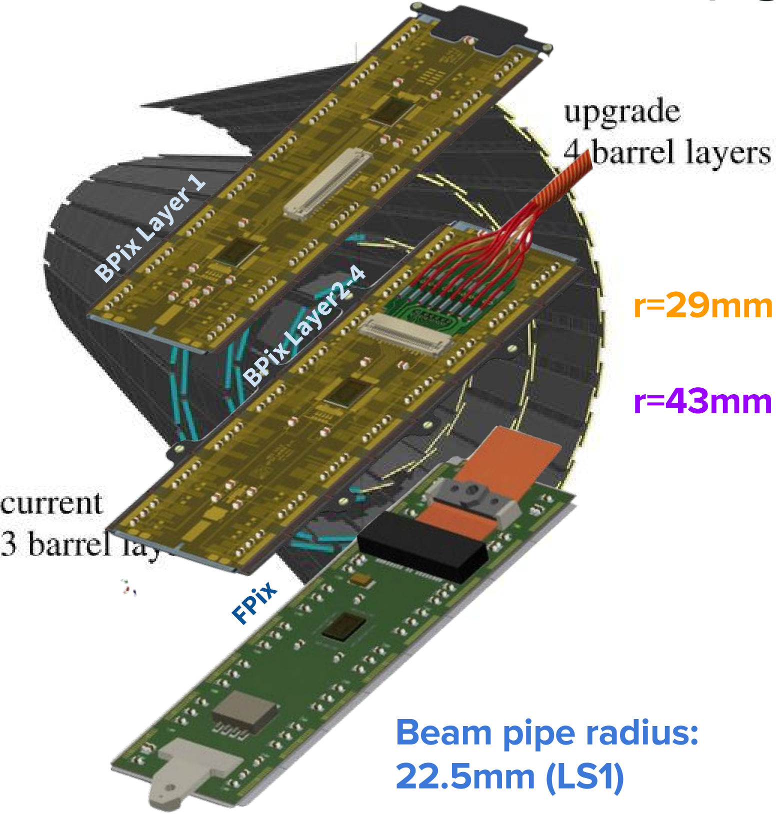
CMS Phase I pixel detector hit resolution



See also talk by Viktor Veszpremi on tracking performance and alignment

https://twiki.cern.ch/twiki/pub//CMS/PixelOfflinePlotsAugust2017

The CMS Phase-I upgrade pixel detector



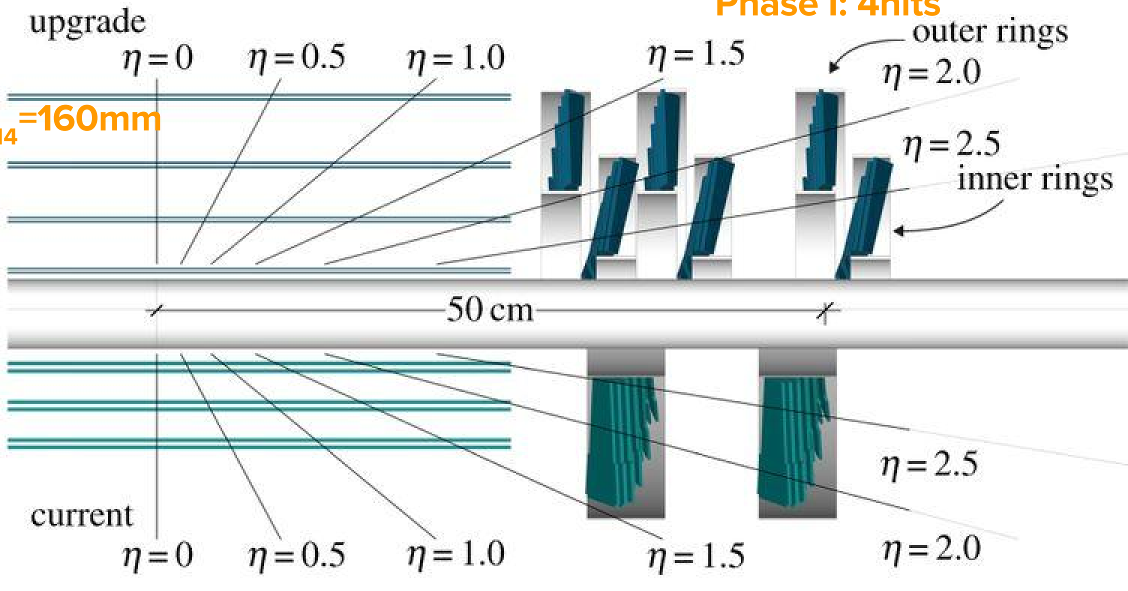
r_{l4}=160mm

r=29mm

r=43mm

Beam pipe radius: 22.5mm (LS1)

Phase I: 4hits

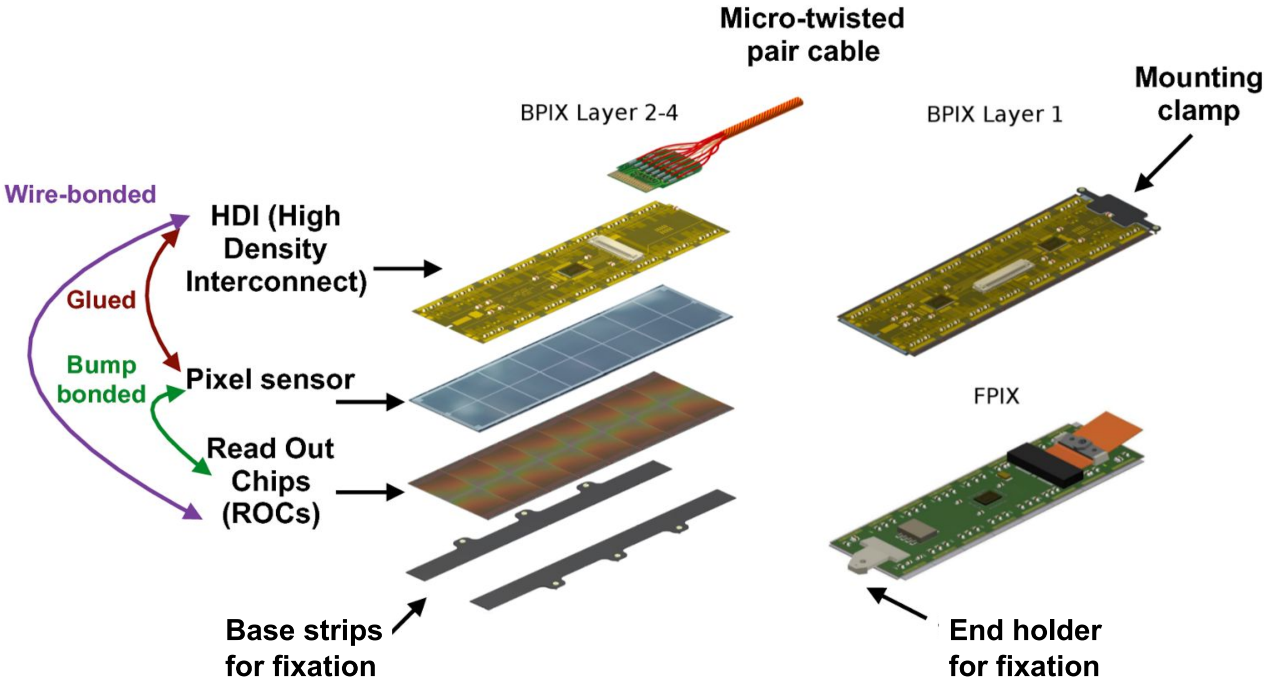


Phase 0: 3 hits

http://d29qn7q9z0j1p6.cloudfront.net/content/roypta/373/2032/20140046/F2.large.jpg

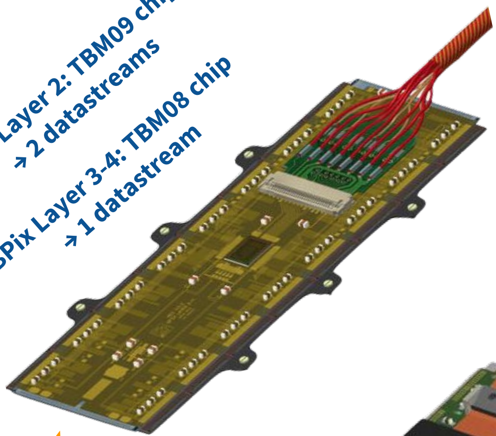
Phase I modules

- 285 µm thick n^{+}-in-n silicon sensors (same)
- 100x150 μm^2 pixel size (same)
- **One sensor geometry** for entire pixel detector
- **2 × 8 readout chips** (ROCs) per module
- **Faster digital ROCs**: 40 MHz analog ➔ 160 Mbit/s digital
- Module **readout bandwidth increased** by a factor of 2 (4 for layers 1 and 2): 40 MHz ➔ 320 Mbit/s

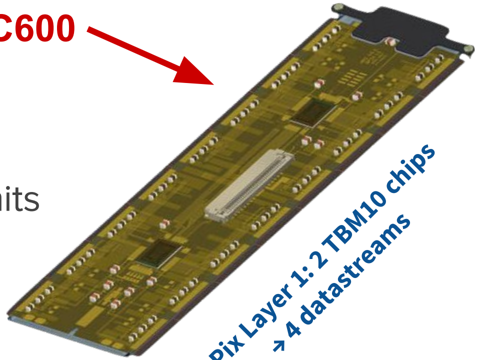


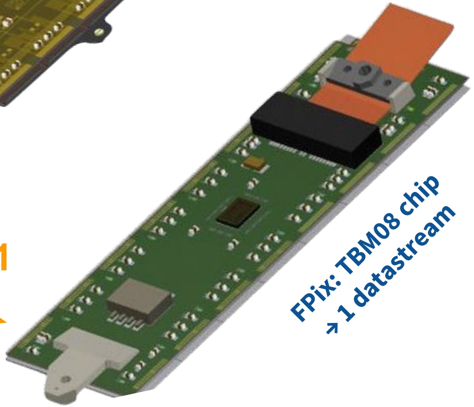
See also https://agenda.infn.it/getFile.py/access?contribId=130&sessionId=10&resId=0&materialId=slides&confId=10190

Phase I readout chips



Readout chip (ROC) PROC600
- CMOS ASIC
- handles hit rate of 600 MHz/cm^2
- 2x2 clusters in the double columns: transmits cluster information
- Dose expected for Layer 1: 120 MRad
- thresholds ~3000 e-



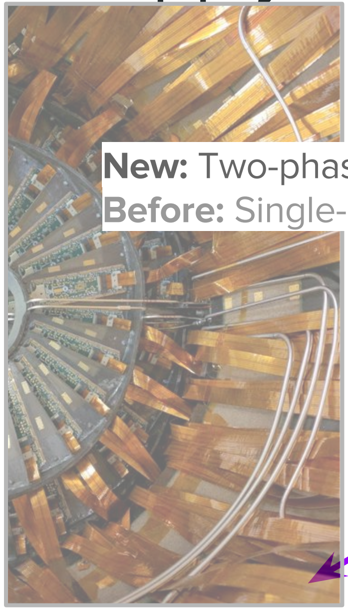


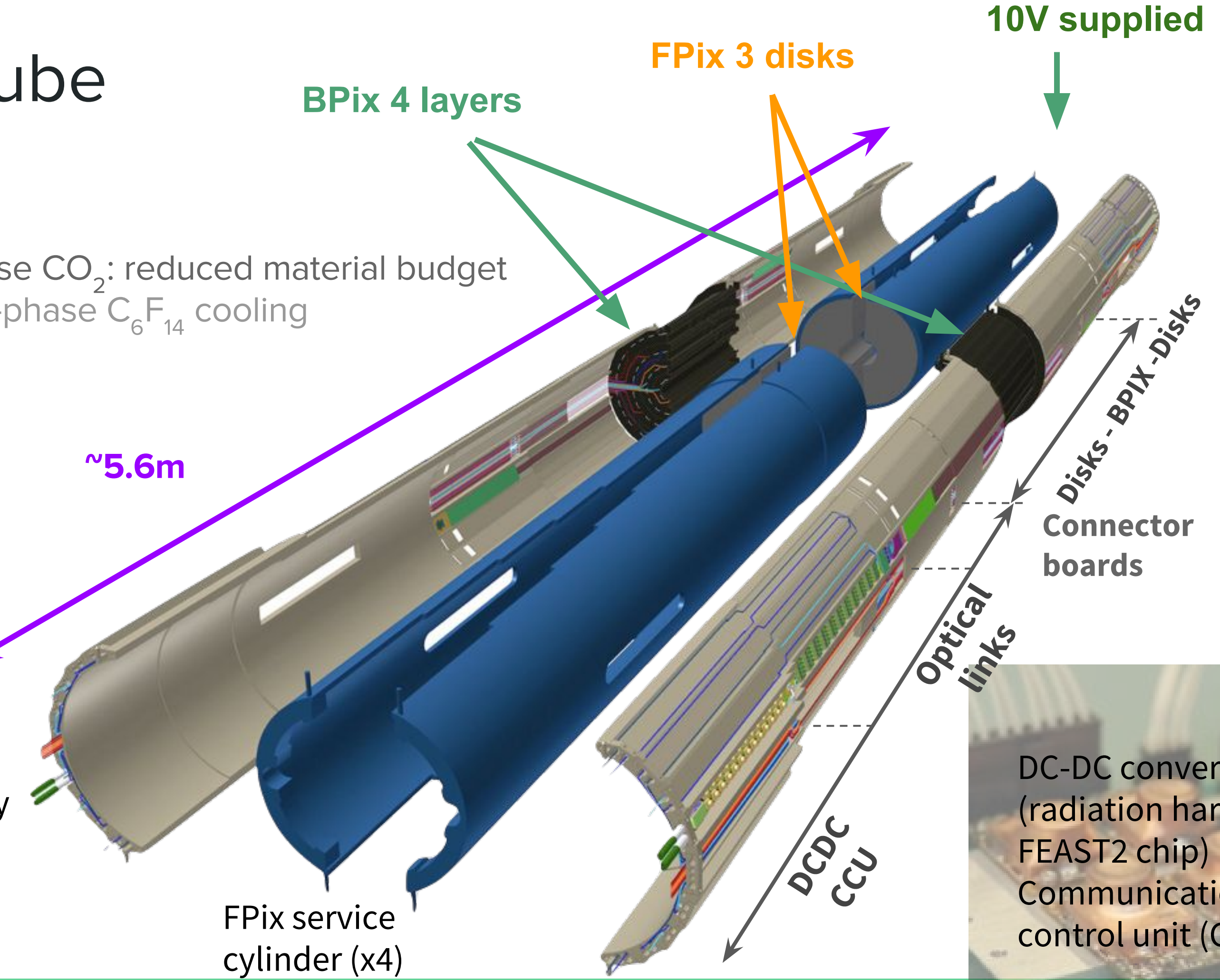
Readout chip (ROC) psi46dig v2.1r
- 250nm complementary-symmetry metal–oxide–semiconductor (CMOS) application-specific integrated circuit (ASIC)
- 80x52 pixels
- pulse-height readout
- 160 Megabit per second (Mbps) at (multiplexed) 160 MHz
- double column drain architecture
- 8bit analog-to-digital converter (ADC)
- thresholds ~1800 e- (was: 3500-e)
- data streams from 2 ROC banks merged inside the TBM ✿❀

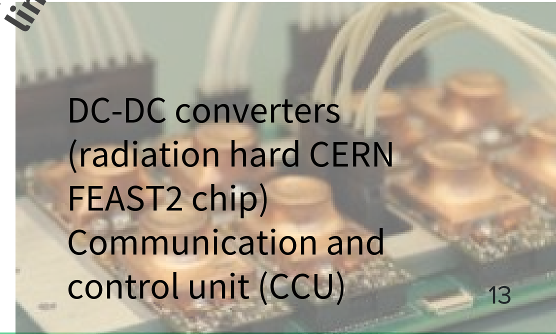
Token bit manager (TBM):
320 Mbps parallel readout at 400MHz

Supply tube

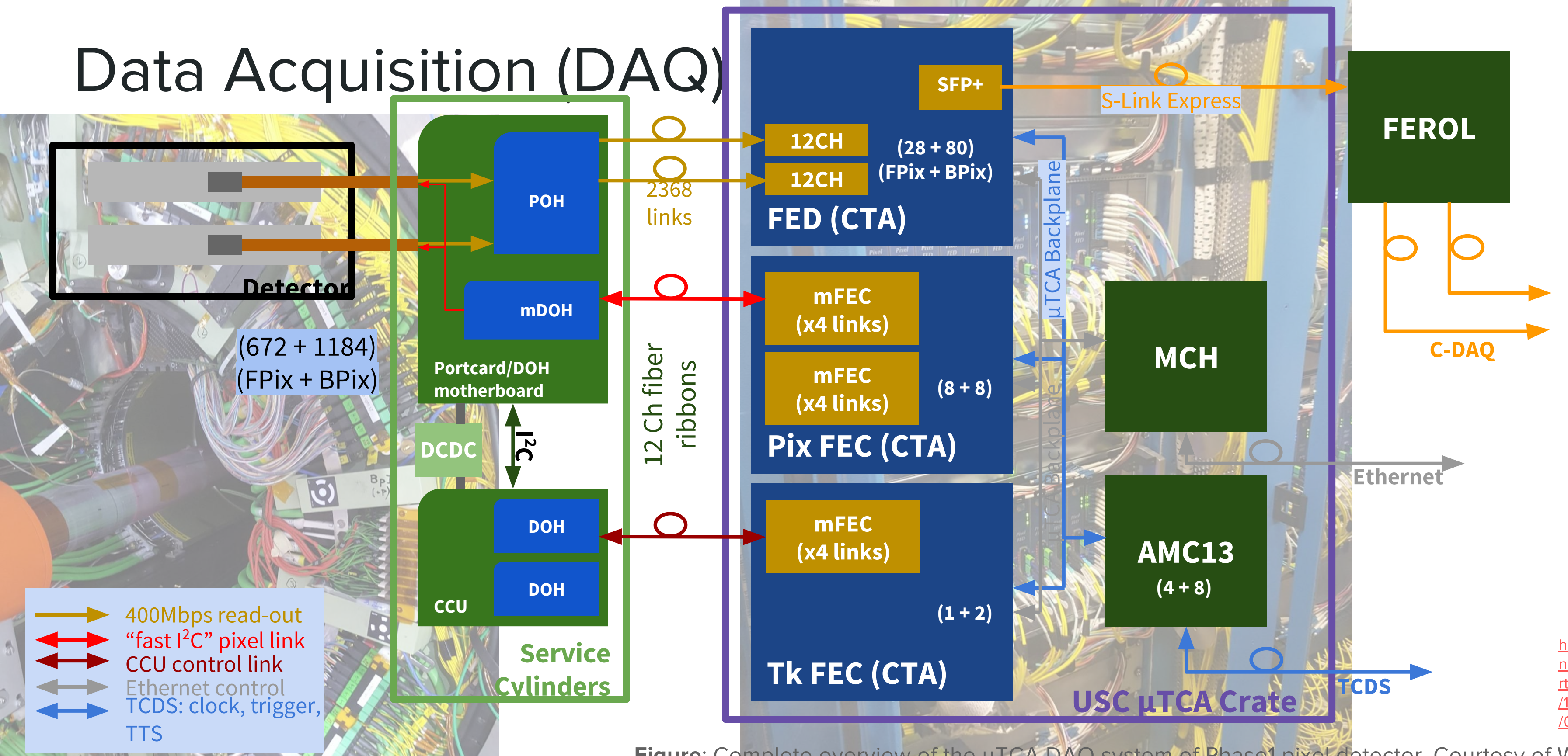
New: Two-phase CO_2: reduced material budget
Before: Single-phase C_6F_{14} cooling







Data Acquisition (DAQ)



http://iopscience.iop.org/article/10.1088/1748-0221/11/01/C01056

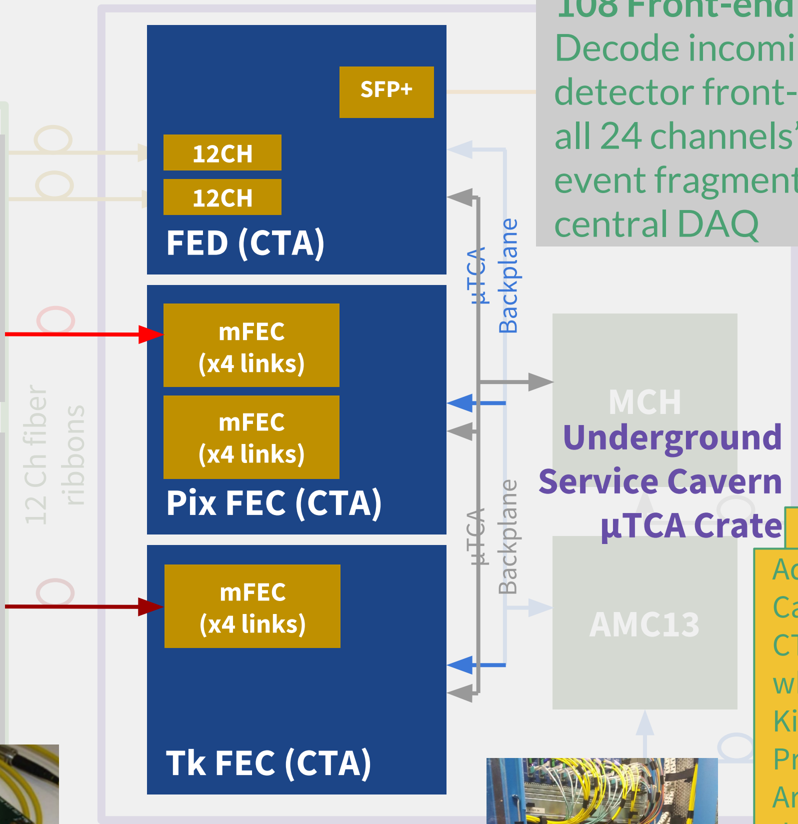
Figure: Complete overview of the μTCA DAQ system of Phase1 pixel detector. Courtesy of Weinan Si.

New: micro-TCA(Telecommunications Computing Architecture)-based DAQ
Before: VME(Versa Module Europa)-based

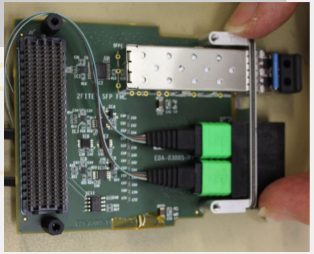
DAQ System

16 Pixel front-end controller (Pixel FECs):
Distribute clock, trigger and fast signals to pixel modules, program digital to analog converter (DAC) registers of ROC and TBM

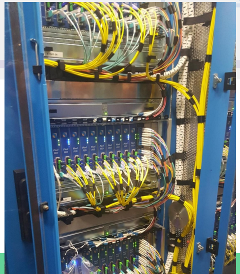
3 Tracker FECs:
program auxiliary components in pixel supply electronics like opto-hybrids and DC-DC converters via inter-integrated circuit (I^2C) interface and peripheral interface adapter (PIA) port of a CCU



108 Front-end drivers (FEDs):
Decode incoming data stream from detector front-end, each assemble all 24 channels' (12 fibers) data into event fragments, then push to central DAQ



Advanced Mezzanine Card (AMC), based on CTA card (variant of FC7) which holds a Xilinx Kintex 7 Field Programmable Gate Array (FPGA). Capable to drive/receive links of up to 10Gb/s

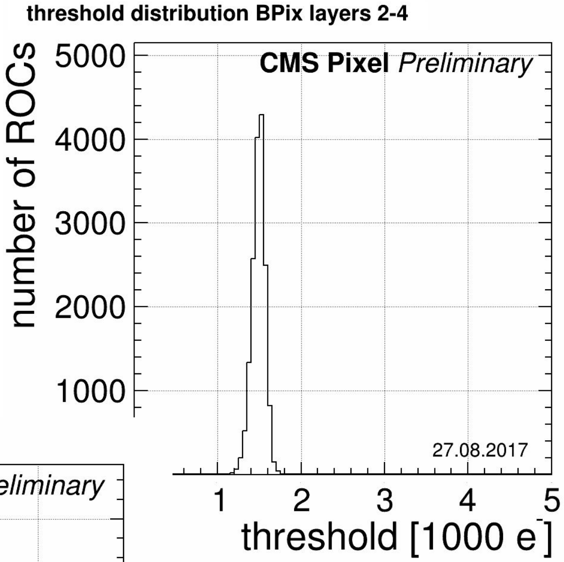


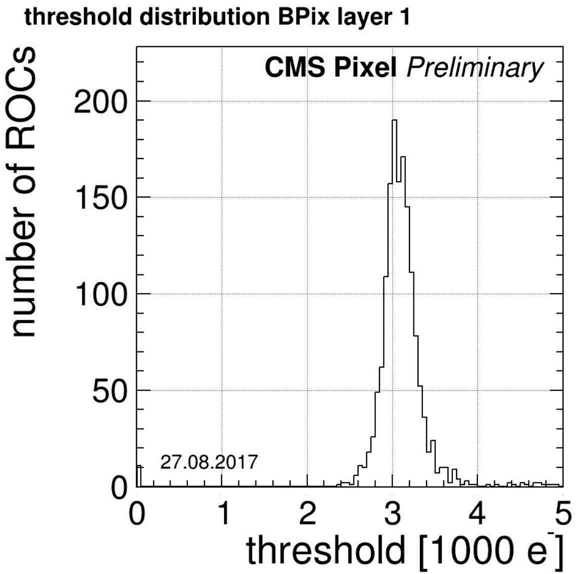
See also https://indico.cern.ch/event/299180/contributions/1659595/attachments/563055/775699/FC7.pdf

Checkout

1. **optimize and test basic optical connection**
   ➔ see light from the fiber
2. **adjust supply: signal delays, light yield…**
   ➔ see idle pattern of module
3. **adjust external 400MHz TBM phase**
   ➔ see TBM headers/trailers
4. **adjust internal 160MHz TBM phase/ ROC ports**
   ➔ see ROC headers
5. **inject and readout test hits**
   ➔ see hits

Thresholds in barrel pixel detector



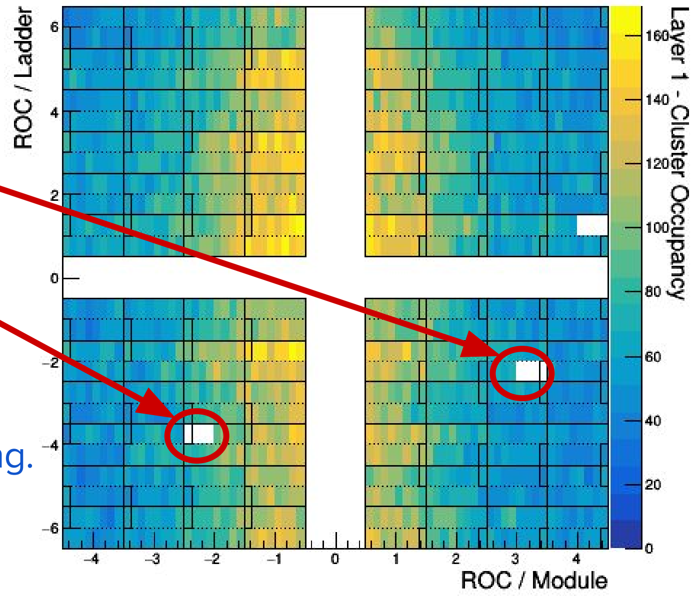


Assumed: 1 ROC internal charge unit is 50e-

https://twiki.cern.ch/twiki/bin/view/CMS/PixelApprovedPlots

Single Event Upsets (SEUs)

- Stuck TBMs
  Solution: powercycle
- Loss of portcards
  Solution: Reprogram portcard
- Conventional ROC SEUs
  Solution: Reprogram ROCs

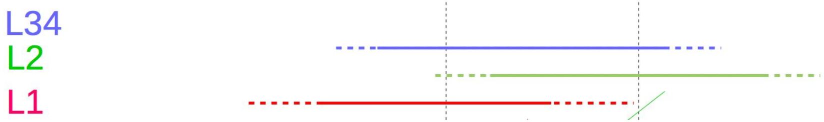


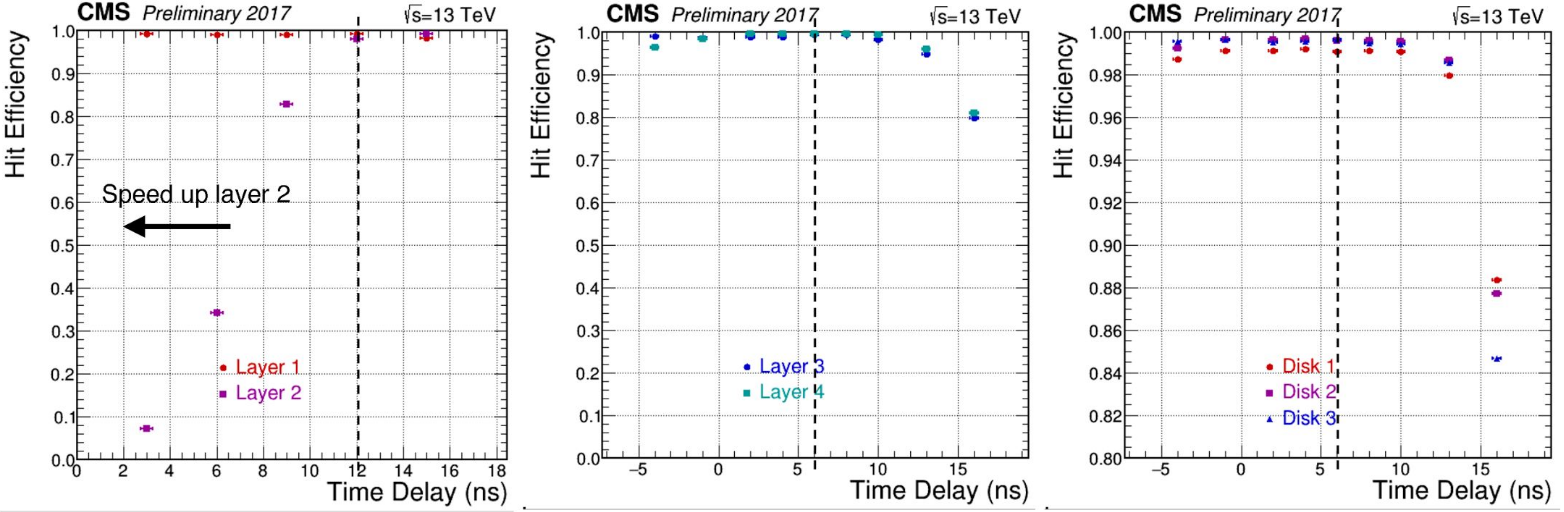
https://twiki.cern.ch/twiki/pub//CMSPublic/PixelOfflinePlots2017/SiPixelQuality-run297099.png

And also:

- To reduce pixel dead time:
  - Automatization of powercycling and reprogramming.
- To improve cluster properties:
  - Private synchronized ROC reset:
    i. Pause triggers
    ii. Pause for *m*1 orbits (read out buffers)
    iii. Send pixel only resync command
    iv. Pause for *m*2 orbits
    v. Re-enable triggers

Layer 1 and 2 timing





1/2 clock shift between barrel layer 1 and 2 but delay chip shared in single φ sector

PROC600 faster than psi46dig

➜ Speed up L2, slow down L1, with working point of 98% efficiency, e.g.:

Layer 2 100 ➜ 250V gained 1-2 ns

See also talk by Viktor Veszpremi on tracking performance and alignment

Leakage current in phase 0 barrel pixel detector

Average current per ROC normalized to active sensor volume [µA/cm 3]

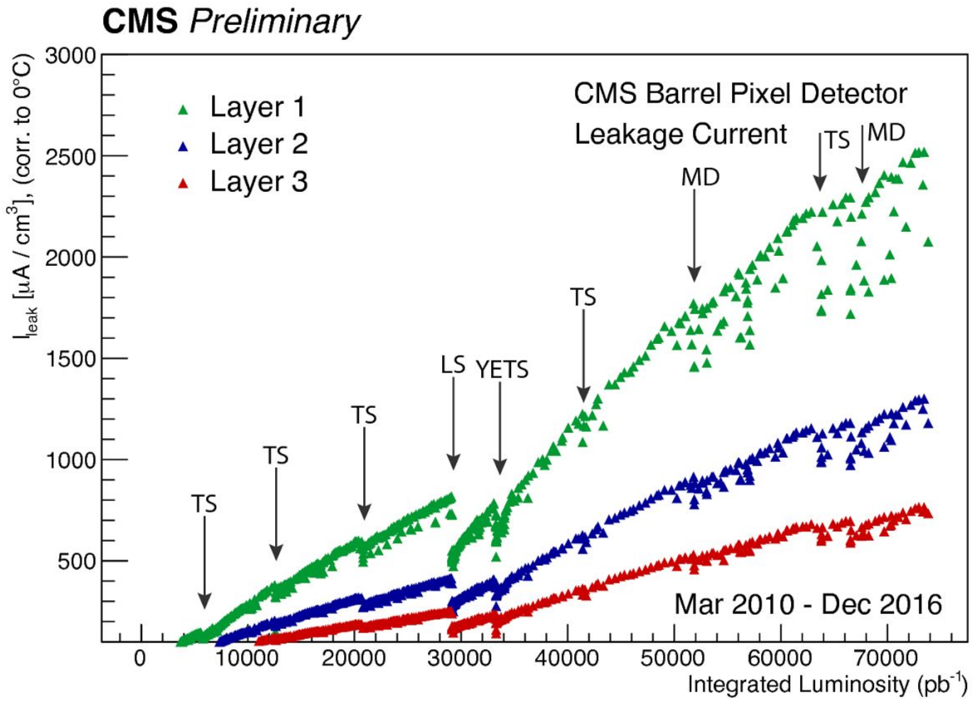
V = 0.81 cm x 0.81 cm x 285 µm

E_g = 1.21 eV, T_{ref} = 273.15 K)

Actual sensor temperature:

$T = T_{coolant} + 10°C$

- Detector temperature -10°C ➜ sensors 0°C
- Fluctuations due to temperature fluctuations (not taken into account)
- Currents averaged over all channels in a layer.



$$I(T_{ref}) = I(T)\left(\frac{T_{ref}}{T}\right)^2 \exp\left(-\frac{E_g}{2k_B}\left[\frac{1}{T_{ref}} - \frac{1}{T}\right]\right)$$

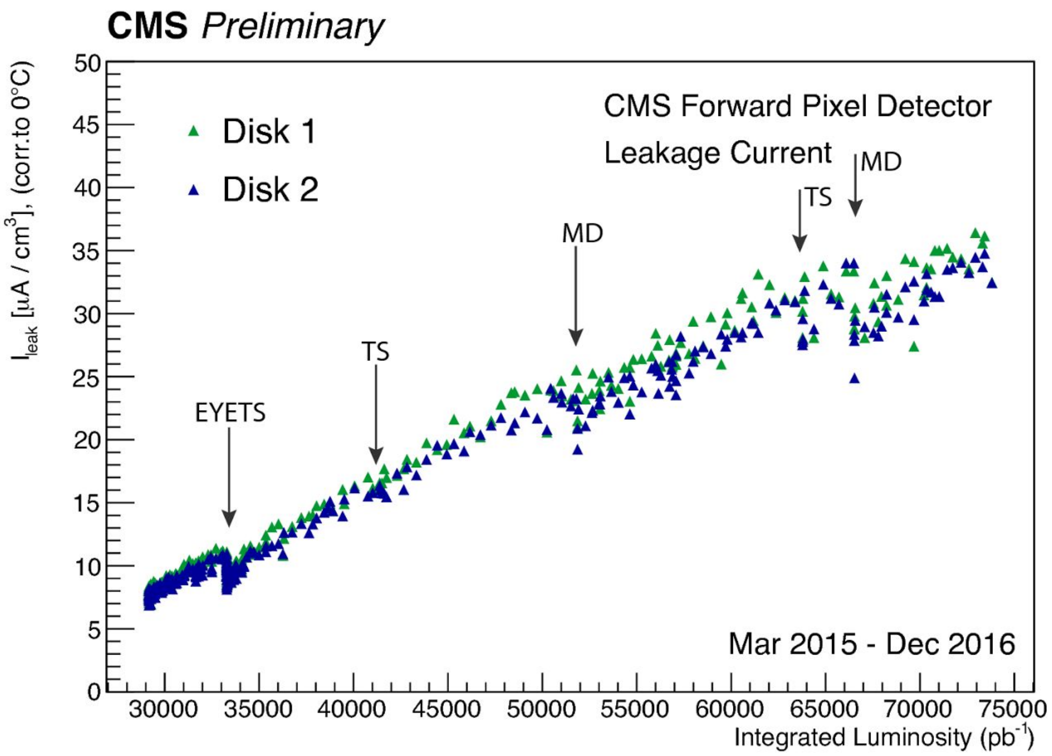
Leakage current in phase 0 forward pixel detector

- Detector temperature -10°C ➔ sensors 0°C
- Fluctuations due to temperature fluctuations (not taken into account)
- Currents averaged over all channels in a disk.

TS technical stop

YETS year end technical stop

MD machine development



Leakage current phase I barrel pixel detector run 2

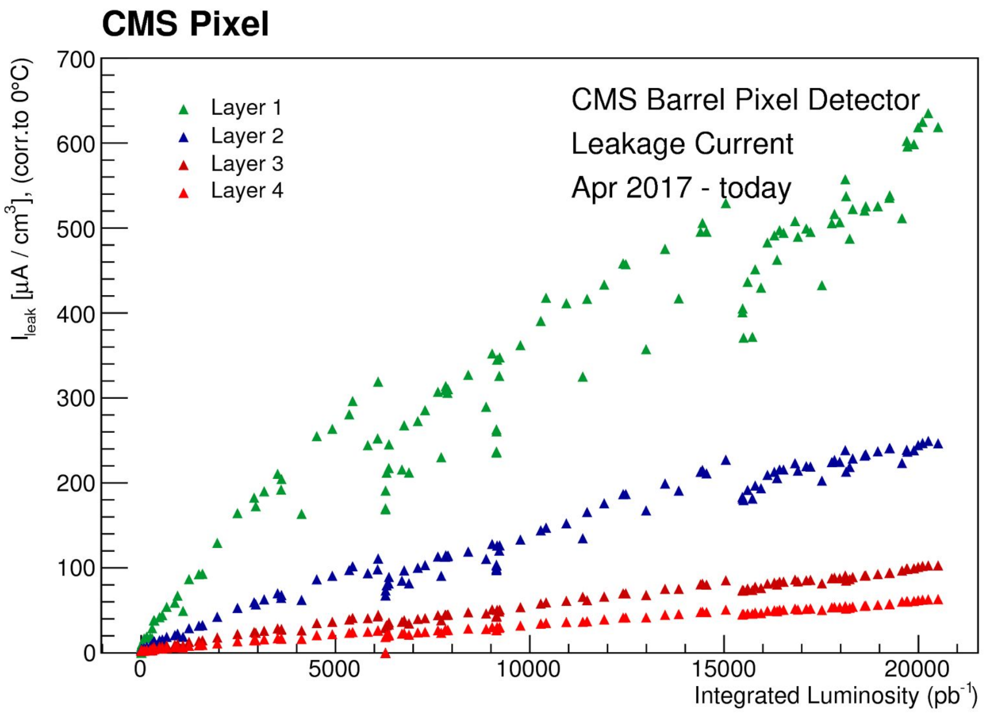
Average current per ROC normalized to active sensor volume [µA/cm 3]

V = 0.81 cm x 0.81 cm x 285 µm

E_g = 1.21 eV, T_{ref} = 273.15 K)

Actual sensor temperature:

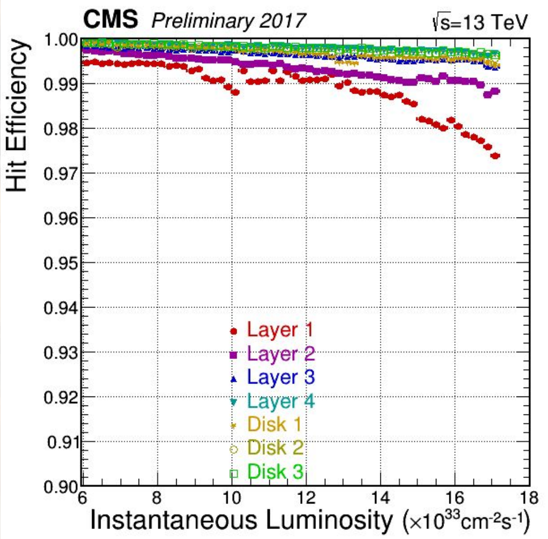
$T = T_{coolant} + 10°C$



https://twiki.cern.ch/twiki/bin/view/CMS/PixelApprovedPlots

Conclusion

- Phase 1 pixel upgrade successfully installed during winter 2016-2017 EYETS: this was a significant milestone in the CMS phase I upgrade project;
- 2017 pixel commissioning was challenging but performance benefits are starting to be realized;
- The CMS phase I pixel system is now successfully taking data;
- DAQ is performing smoothly;
- Initial studies show that performance of more complex functions like *vertexing* is already better than with the phase 0 pixel detector.



We successfully commissioned the CMS Phase I pixel detector to achieve performance of the same level as the phase 0 pixel detector under higher instantaneous luminosity and will continue commissioning to improve performance.

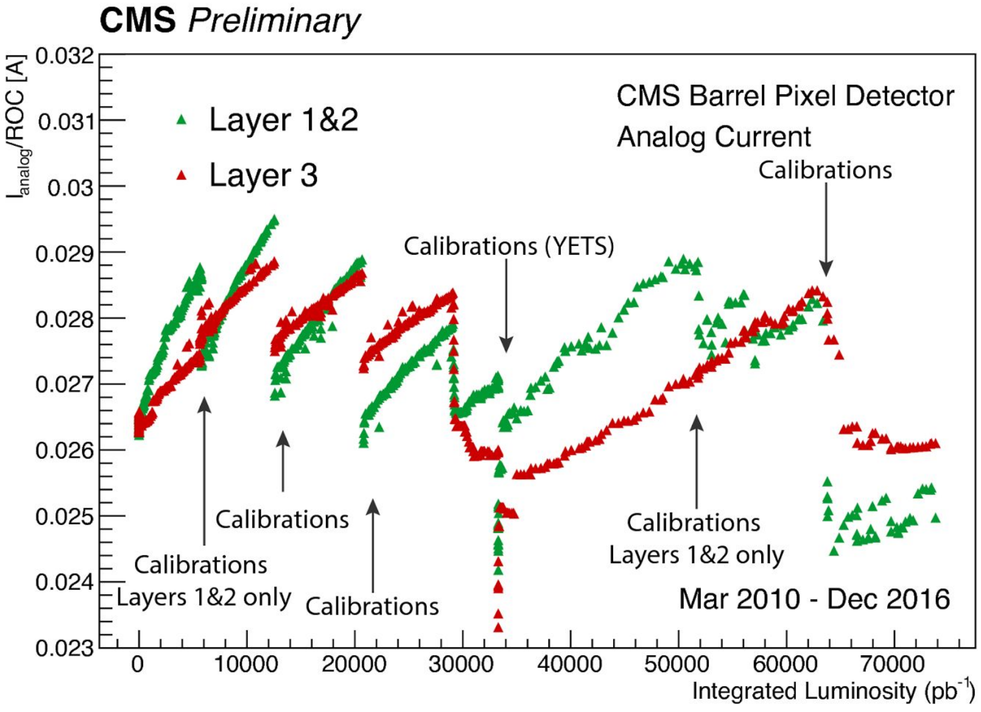
Backup

Analog current for phase 0 barrel detector

Analog current per readout chip averaged over all channels in each layer group.

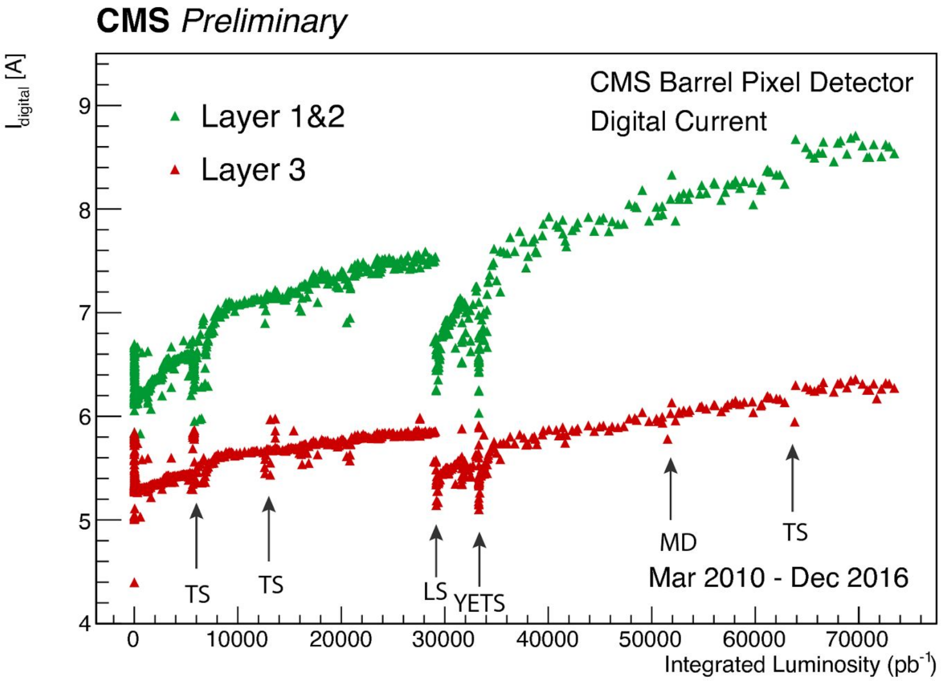
Note: layer 3 was calibrated less often.

TS technical stop
YETS year end technical stop
MD machine development



Digital current for phase 0 barrel detector

Digital current per readout chip averaged over all channels in each layer group.



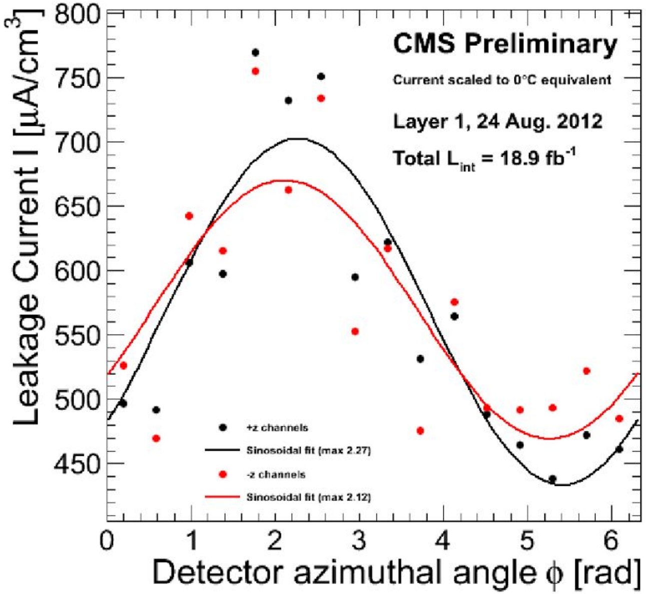
LS long shutdown

TS technical stop

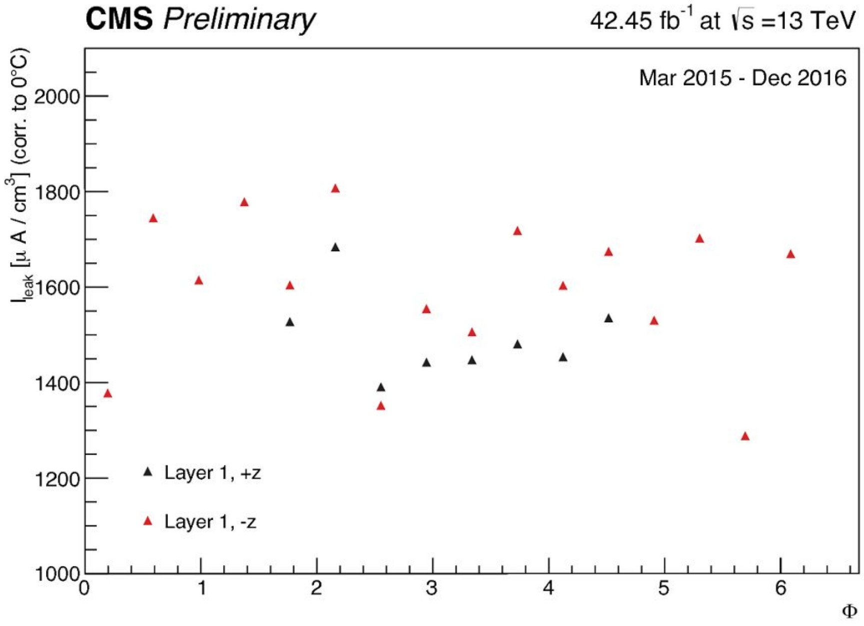
YETS year end technical stop

MD machine development

Leakage current in phase 0 pixel barrel layer 1: transverse plane

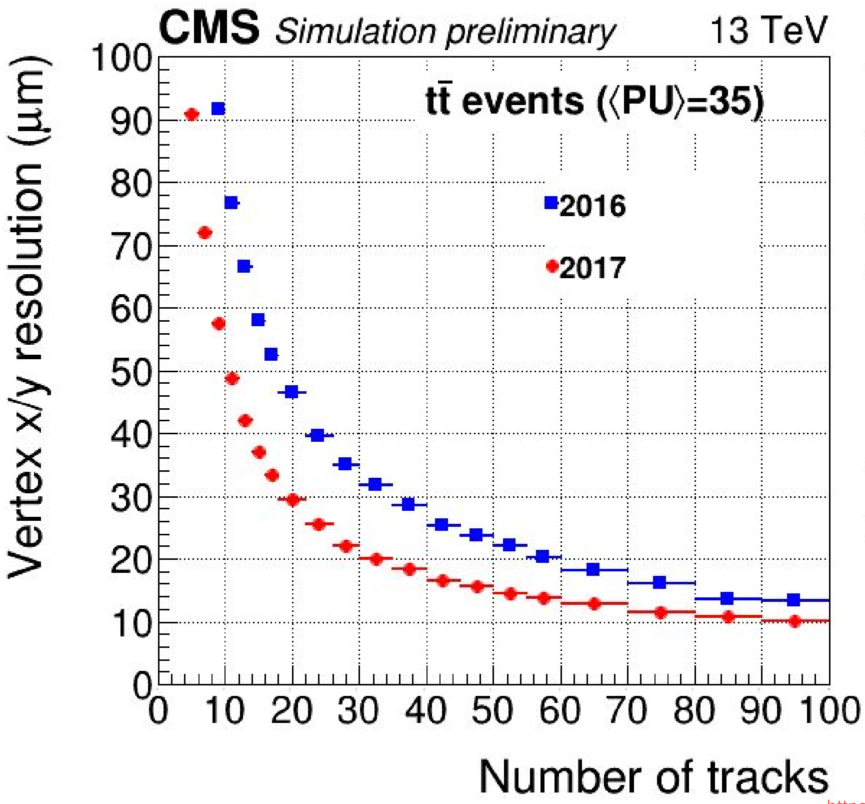


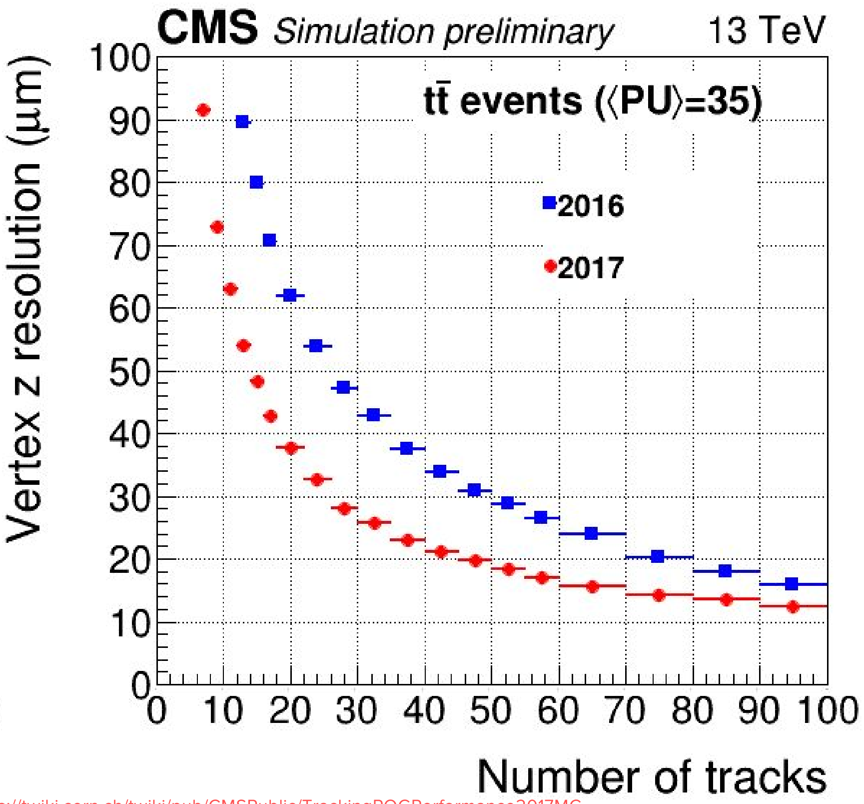
Nonhomogeneous increase due to displacement of barrel detector center with respect to beam spot



Run 2, after recentering the barrel detector with respect to beam spot, excluding new modules installed in LS1 (➔ radiation dose differences)

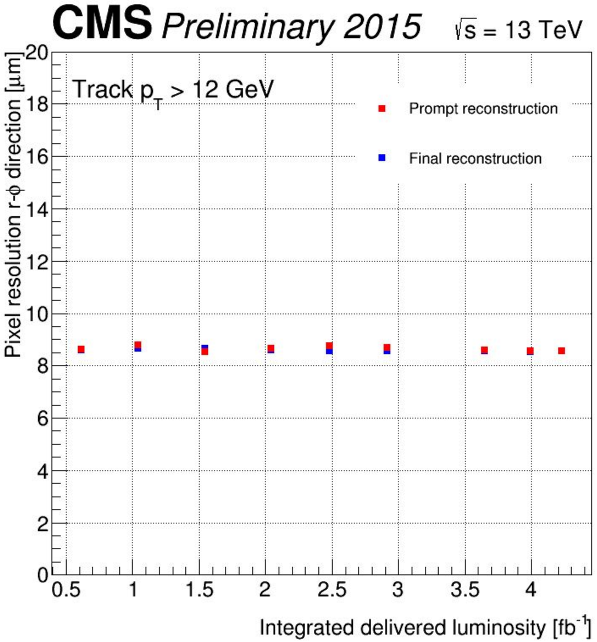
Phase 0 vs phase I resolutions from simulation

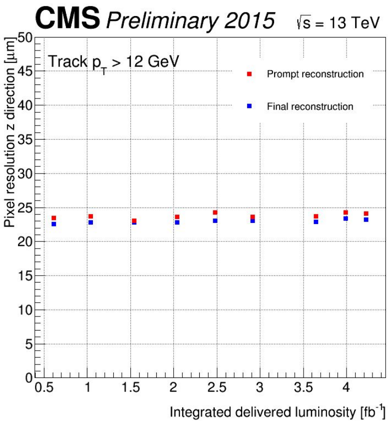


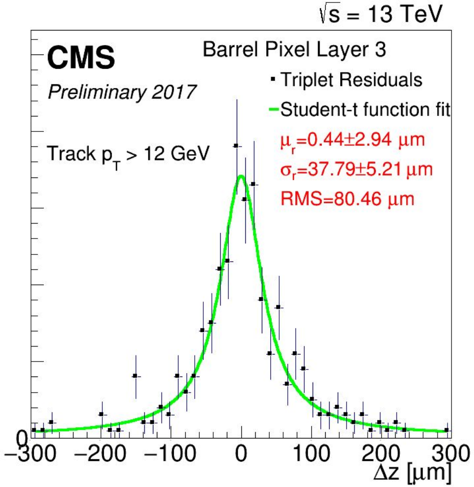


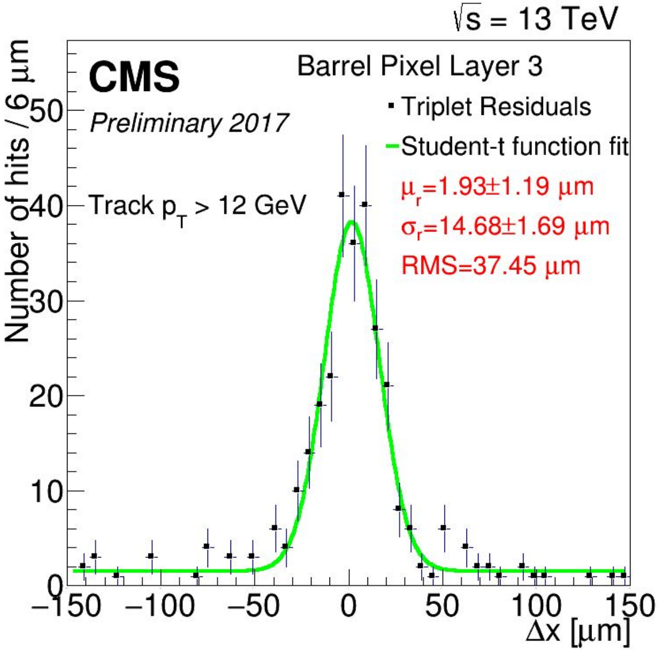
https://twiki.cern.ch/twiki/pub/CMSPublic/TrackingPOGPerformance2017MC

Pixel phase 0 and I detector resolution





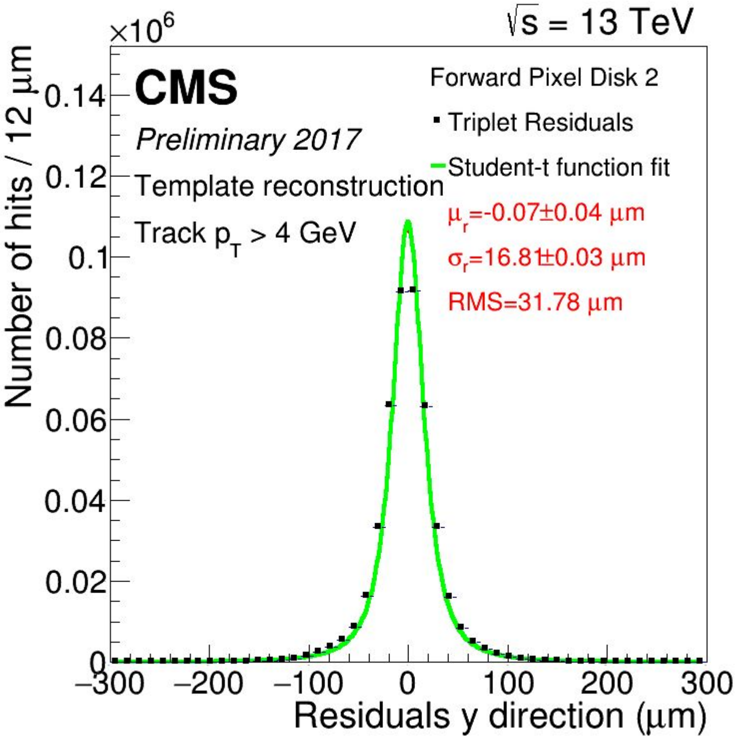


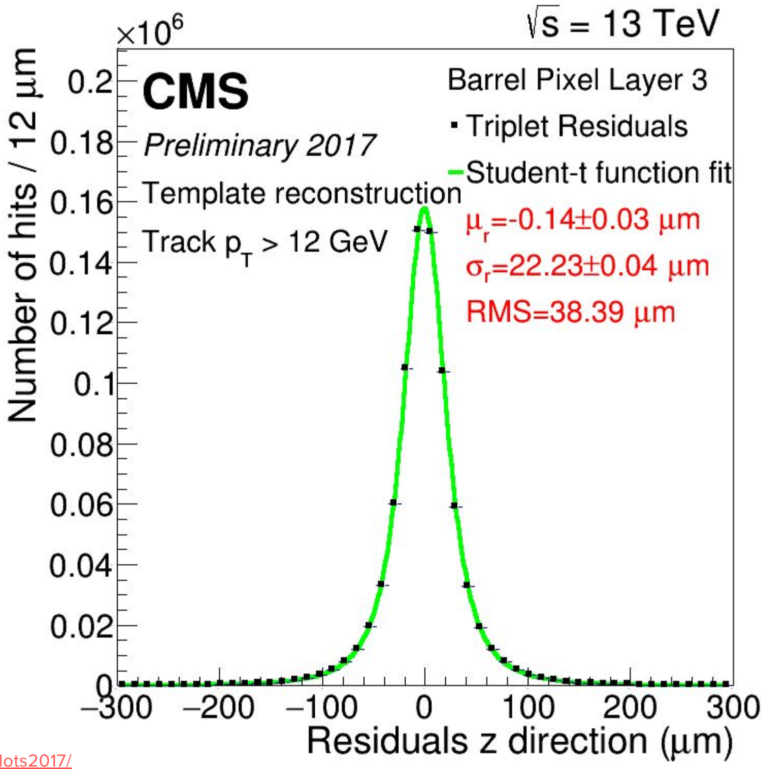


https://twiki.cern.ch/twiki/pub//CMSPublic/PixelOfflinePlots2017/

https://twiki.cern.ch/twiki/pub/CMSPublic/PixelOfflinePlots2016/

Residuals CMS Phase I pixel detector





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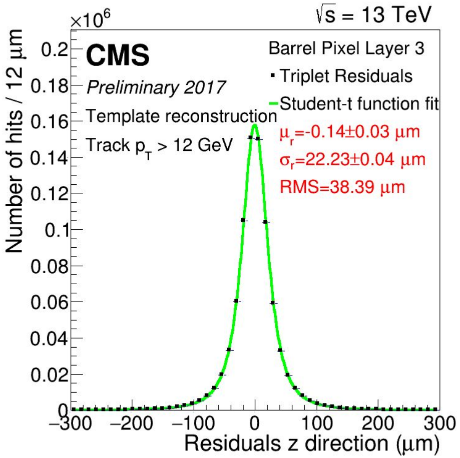
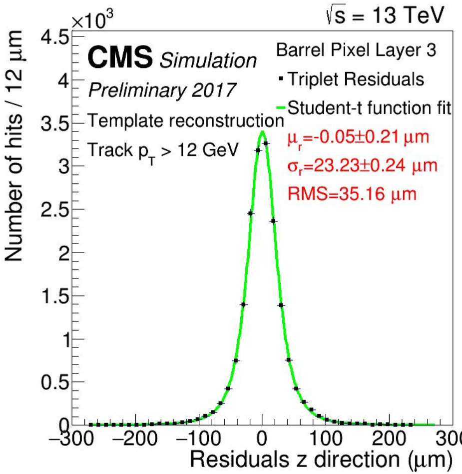
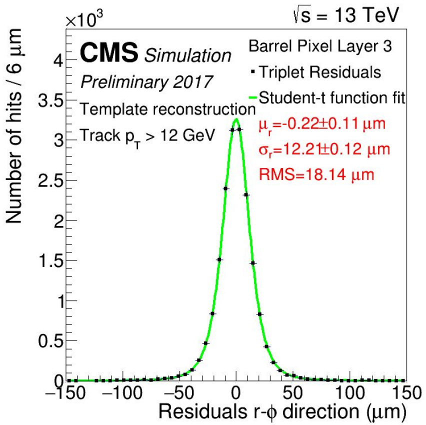
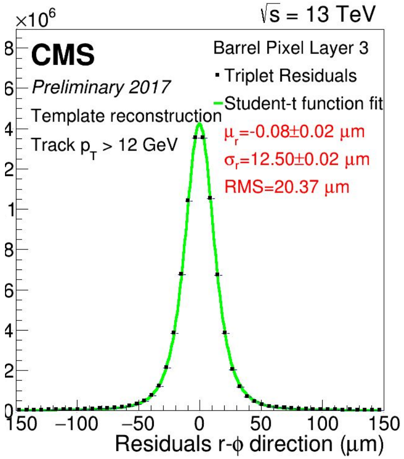
Residuals in data and simulation









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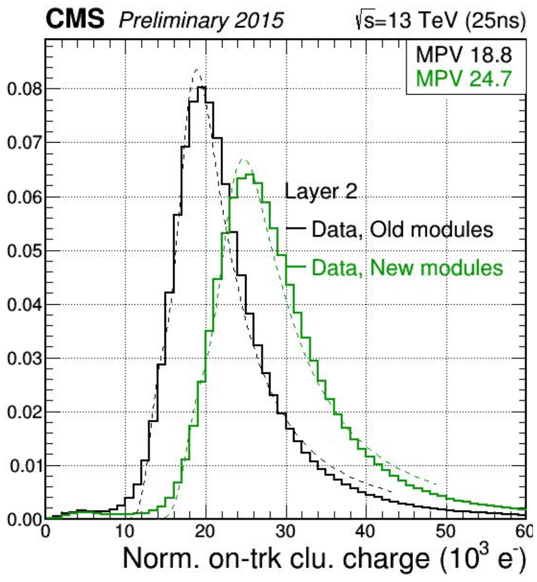
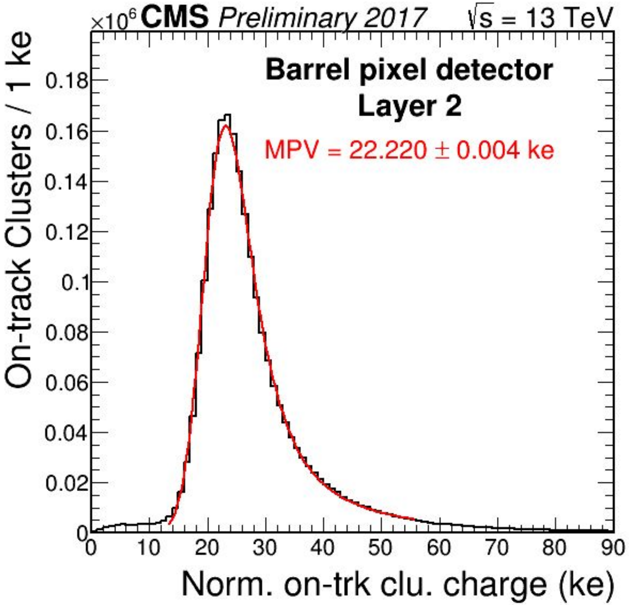
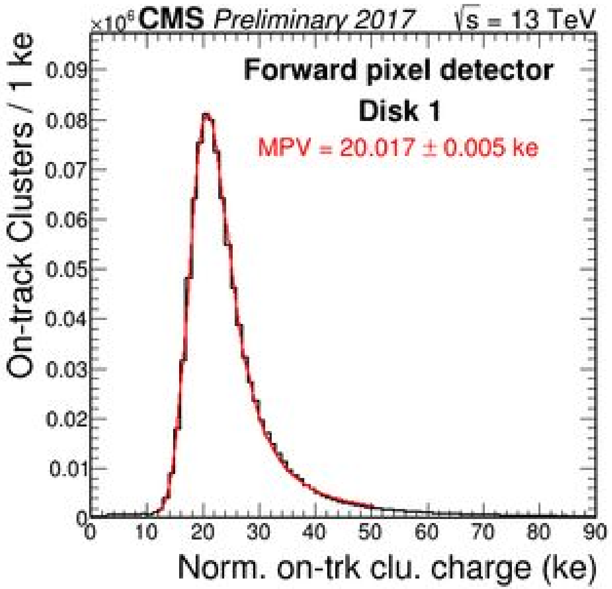
CMS phase I and phase 0 on track cluster charge







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