MAPS-based Vertex Detectors: Operational Experience in STAR and Future Applications



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Outline

- First MAPS-based Vertex detector:
 - STAR HFT
 - Design
 - Operations experience
 - Performance and Physics
- Next generation MAPS:
 - ALICE ITS Upgrade
 - sPHENIX MVTX



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The STAR Heavy Flavor Tracker

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high multiplicity environment

SSD – Silicon Strip Detector

improved resolution:

IST – Intermediate Silicon Tracker

Tracking inwards with gradually

 $\sigma = ~1 \text{ mm}$

 $\sigma = \sim 300 \ \mu m$

 $\sigma = ~250 \ \mu m$

 $\sigma = <30 \ \mu m$

Extend the measurement capabilities in the *heavy flavor* domain, good probe to QGP:

Direct topological reconstruction of charm hadrons (e.g. $D^0 \rightarrow K \pi, c\tau \sim 120 \mu m$)





PXL Design Parameters

DCA Pointing resolution	(10 ⊕ 24 GeV/p·c) μm
Layer locations	Layer I at 2.8 cm radius
	Layer 2 at 8 cm radius
Pixel size	20.7 μm X 20.7 μm
Hit resolution	3.7 μm (6 μm geometric)
Position stability	5 μm RMS (20 μm envelope)
Sensor thickness	50 μm
Power dissipation	170 mW/cm ²
Material budget first layer	$X/X_0 = 0.39\%$ (Al conductor cable)
Integration time (affects pileup)	185.6 μs
Radiation environment	20 to 90 kRad / year
	2*10 ¹¹ to 10 ¹² 1MeV n eq/cm ²
Rapid detector replacement	< I day

356 M pixels on ~0.16 m² of Silicon



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PXL System Overview





The PiXeL detector (PXL)

First vertex detector at a collider experiment based on Monolithic Active Pixel Sensor technology





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PXL MAPS sensor



ionizing particle

- Ultimate-2: third MIMOSA-family sensor revision developed for PXL at IPHC, Strasbourg
- Monolithic Active Pixel Sensor technology

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STAR PXL Operations, Performance, Physics Achievements

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PXL timeline and operations



- > 2013 Engineering Run (3 prototype sectors) allowed discovering and fixing:
 - Shorts between power and GND, or LVDS outputs
 - Mechanical interference in the driver boards on the existing design
 - Missing power control, monitoring and overcurrent thresholds functionalities

> 2014-2016 **Physics Runs**: PXL Operations

- Hit multiplicity: up to 1000/inner-sensor
- Typical trigger rate: 0.8-1 kHz
- ► 2014 Run: ~ I.2 Billion Au+Au
- 2015 Run: ~ I Billion p+p, ~ 0.6 Billion p+Au
- ▶ 2016 Run: ~ 2 Billion Au+Au , 0.3 Billion d+Au

- Dead time up to ~6%
- Latch-up reset events: 2 latch-up/min

Minimum bias events in PXL acceptance @ √s_{NN} = 200 GeV

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Operational Aspects



- Operational **latch-up protection and voltage control** limited the effect of LU-related sensor damage (more later in this talk)
- **Detector reset** on a 15 minute schedule limited SEU-related data corruption
- Mechanics
 - The detector halves maintained survey pixel positions after insertion and during operational heating and in the cooling airflow (10 m/s).
 - The rapid insertion and removal mechanism worked well, allowing removal and replacement operation of a 2nd detector in one day.
- Air cooling worked very well, typical variation in sensor temperature over the runs was within 1-2 degree C.



PXL Kinematic mounts

Sector vibration in the radial direction scales as:	flow ²
Sector vibration at full flow:	5 µm RMS
Sector DC displacement scales as:	flow ²
Sector moves in at full flow: (Stable displacement)	25 μm - 30 μm
Sector moves in when ladders powered: (Stable displacement)	3 µm - 8 µm



Composite IR image of PXL test ladders

IR image of production PXL ladders. Max ΔT is 12° C from ambient.





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Operational issues: Latch-up damage



- Digital power current increase
- Sensor data corruption
- Hotspots in sensor digital section
- Correlated with *latch-up* events
- Limited with operational methods





Latch-up tests at BASE facility (LBL) to measure latch-up cross-section and reproduce damage

- 50 μm & 700 μm thick, low and high resistivity sensors; PXL ladders
- Irradiation with heavy-ions and protons

Latch-up phenomenon:

- Self feeding short circuit caused by single event upset
- Can only be stopped by removing the power



Results and observations

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- Current limited latch-up states observed (typically ~300 mA)
- Damage reproduced only with HI on PXL 50 μ m thinned sensors
- Latch-up protection at 80 mA above operating current

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Periodic detector reset to clear SEU

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Latch-up test damage analysis

Hot spot showing damage to sensor #2 on run 14 ladder



50 um thinned silicon Temperatures from 55-100 C

- Full thickness sensors were tested for LU during development: measured cross section consistent with LU events recorded on the detector
- Damage cross section is too low to easily measure with individual sensors based testing

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Hotspots tend to favor particular structures (isolated buffers with specific structure pitch)





PXL sensor layers deconstructed (plasma etching technique) and viewed with SEM (@BNL Instrumentation Division)

The layers appear to be melted



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Latch-Up Damage evolution

Run	Good sensors on Inner Layer		Good sensors on Outer Layer		Comment
	installation	end of run	installation	end of run	
2014	100%	82%	100%	95%	LU damage, most of it in the first 15 days of operations
2015	99 %	94%	98%	96% (93%)*	* = Lost control of an outer ladder (10 good sensors off)
2016	100%	95% (87%)+	99 %	98%	⁺ = Current instability on inner ladder (8 good sensors off)

Good sensor = sensor with >95% active channels and uniform efficiency

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Software/Firmware issues

Reconstruction software issue - 2014 data production

- A bug in the **reconstruction** software led to an **efficiency loss** in the reconstructed 2014 Run data, affecting the preliminary STAR results
- After fixing the bug, the new data reconstruction and analysis showed a significant improvement in the tracking performance which now matches the simulation → ~4x Significance



- Readout firmware issue 2015 data, matching inefficiency
 - A subtle bug introduced by a change in the **PXL RDO firmware** led to an efficiency loss in the 2015 Run p+p data
 - Feedback and data QA tools:
 - The extensive tests with pattern data and the calibration were inadequate
 - A fast-offline tracking QA was put in place only after the 2015 Run
 - **Fix:** A post-run investigation based on external **sensor illumination with LED** allowed for firmware debugging and fixing

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HFT Performance from 2014 data



Alignment

Residuals distribution after alignment shows $\sigma \leq 25 \ \mu m$





- $\Lambda_{c}^{\pm} \rightarrow p^{\pm} K^{\mp} \pi^{\pm} c\tau \sim 60 \mu m BR = 5 \%$
- Experimentally challenging to measure in heavy-ion collisions
 - → Combinatorial background is greatly suppressed
- Significance: $S/\sqrt{S+B} \sim 5.2$ (10-60% centrality, p_T : 3–6 GeV/)
- Λ_c/D^0 ratio compatible with baryon-to-meson ratios of light hadrons

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STAR PXL Project: Strengths and Weaknesses

Strengths

- MAPS technology features
- Sensor and Readout System developments strictly coupled
- Engineering run, crucial for the program
- ~Full control on the production



Weaknesses

- The technology was new for a collider environment
- Short (3-years) physics program
- Sensor integration time too long to access the bottom domain

----> Future: ALICE ITS Upgrade, sPHENIX MVTX





Evolution of MAPS-based Vertex Detector

2014-2016

2021+



Integration time: **186** μ s Thickness first layer: 0.4%X₀

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Integration time: <20 μ s Thickness first layer: 0.3%X₀

Next generation MAPS detector used for ALICE ITS Upgrade and proposed for sPHENIX MVTX: Thin MAPS detector with much shorter integration time -> Significantly reduced background hits -> Much improved tracking efficiency

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@LHC: ALICE ITS Upgrade from HybridPixels/Drifts/Strips to MAPS



 \rightarrow see A. Alici on the Current ITS (this workshop)



Upgraded ITS Performance

Performance of new ITS (MC simulations)





Impact parameter resolution

Tracking efficiency (ITS standalone)

Existing ITS: **ITS Upgrade:**

Hybrid pixels, drift, strips All layers are MAPS sensors

 $X/X_0 \ge 1\%$ /layer ~120 µm @ 500MeV/c X/X₀ ~0.4% /layer ~40 µm @ 500MeV/c

Physics Goals:

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Improve charm meson study - Access charm baryons, bottom hadrons in Pb-Pb collisions

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CMOS Pixel Sensor using TowerJazz 0.18 μ m CMOS Imaging Process



 \rightarrow see also R.Tieulent on the ALICE MFT (this workshop)

ALPIDE sensor (developed at CERN)

- ~28 μm pitch
- Integration time: < 20 μ s
- Trigger rate: 100 kHz
- Read out up to 1.2 Gbit/s
- Power: 40 mW/cm²
- Priority encoder sparsified readout
- Rad. Tolerant: 700krad -10¹⁴ IMeV n_{eq}/cm²
- High-resistivity (> $1k\Omega$ cm) p-type epitaxial layer (20μ m 40μ m thick) on p-type substrate
- Small n-well diode (2-3 μ m diameter), ~100 times smaller than pixel => low capacitance
- Application of (moderate) reverse bias voltage to substrate can be used to increase depletion zone around NWELL collection diode
- Quadruple well process: deep PWELL shields NWELL of PMOS transistors, allowing for full CMOS circuitry within active area

New ITS Layout - Inner Barrel Stave

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QRHIC: MAPS Vertex Detector (MVTX) for **PH**^{*}ENIX

sPHENIX: next-generation heavy-ion experiment on jets and Upsilons at RHIC - detailed in NSAC long range plan 2015

- received first approval in Sept. 2016, inner tracker detectors not included in the baseline

MVTX brings new **heavy flavor** physics program to sPHENIX - open bottom production at mid-rapidity over a broad momentum at RHIC

Physics-driven Detector Requirements

Physics goal: Access and study open bottom physics at RHIC

Design goals: Reduce background hits, improve tracking efficiency

ltem	Requirements
Acceptance	Vertex $ z < 10$ cm, $ \eta < 1$, full azimuthal coverage
Event rate	Matching the sPHENIX DAQ rate of 15 kHz event rate
DCA resolution	< 50 μ m for charged pions at p_T =1 GeV/c
Tracking efficiency	> 60% efficiency for charged pions at p _T = I GeV/c in central Au+Au collisions

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sPHENIX MVTX Proposal

A Monolithic Active Pixel Sensor Detector for the sPHENIX Experiment

• Technology choice: **MAPS**

- ALPIDE sensor meets the requirements for MVTX
- Int. time $<20\mu$ s, $\sim28\mu$ m pitch, pow. diss. 40mW/cm²
- Detector layout based on: ITS Inner Barrel

• Leverage the ITS Upgrade R&D for:

- Sensor design and production
- Inner Barrel and Mechanics layout
- Stave production & test
- Power system design
- Readout Units design

Specific R&D - Fabrication - Assembly for MVTX

- Develop data aggregation/formatting/DAQ interface
- Adapt and integrate carbon fiber structures design, and fabricate
- Adapt and fabricate Power System and Readout Units
- Assemble the detector and integrate in sPHENIX

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Proposed MVTX Tasks and Timeline

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Conclusions

- STAR PXL, first generation MAPS-based detector at a collider experiment, successfully completed the 3-year physics program at RHIC
 - Performance met design requirement, access open charm physics
 - > 2013 Engineering Run, short duration program
- MAPS technology proved to be suitable for vertex detector applications
- Next-generation MAPS sensor: ALPIDE
 - Shorter (x10) integration time
 - Higher radiation tolerance
- Next-generation MAPS-based vertex detectors:
 - ALICE ITS Upgrade @LHC (now entering the production phase)
 - sPHENIX MVTX @RHIC (recently proposed)
 - \blacktriangleright Reduced background hits, improved tracking efficiency \rightarrow open bottom physics

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Thank you for your attention!

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Backup slides

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PXL Material Budget

• Carbon fiber supports

- I 25 μm stiffener
- 250 μm sector tube
- 0.193% X₀

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- Cooling
 - Air cooling: negligible contribution

Total material budget on inner layer: 0.388% X₀

(0.492% X_0 for the Cu conductor version)

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HFT DCA pointing resolution: (10 \oplus 24/p) μ m

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PXL Position Control

Vibration at air cooling full flow: $\sim 5 \,\mu m RMS$

 \rightarrow Global hit position resolution: ~ 6.2 µm

Stable displacement at full air flow: \sim 30 μ m

Stable displacement at power on: $\sim 5 \,\mu m$

Metrology survey

- 3D pixel positions on sector are measured with touch probe and related to tooling balls
- Sector tooling ball positions related to kinematic mounts
- \rightarrow Detector-half is fully mapped

HFT DCA pointing resolution: (10 \oplus 24/p) μ m

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Position stability

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PXL Detector Powering and Readout Chain

2013 Engineering Run

• PXL Engineering Run assembly crucial to deal with a number of unexpected issues

Sensor IR picture

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Flawed ladder dissection: searching for shorts

- Shorts between power and gnd, or LVDS outputs
- Adhesive layer extended in both dimensions to increase the portion coming out from underneath the sensors
- Insulating solder mask added to low mass cables

- Mechanical interference in the driver boards on the existing design.
- The sector tube and inner ladder driver board have been redesigned to give a reasonable clearance fit
- ► Inner layer design modification: ~ 2.8 cm inner radius

Inner layer design

- Limited capability to remotely control power and current limits
- After the engineering run added functionality to the Mass Termination Board:
 - remote setting of LU threshold and ladder power supply voltage + current and voltage monitoring

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ALPIDE Pixel Architecture

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ALPIDE performance

Detection Efficiency and Fake-Hit Rate

- Big operational margin with only 10 masked pixels (0.002%)
- Chip-to-chip fluctuations negligible
- Non-irradiated and NIEL/TID chips show similar performance
- Sufficient operational margin after 10x lifetime NIEL dose

From ITS Upgrade Talk @ QuarkMatter I 7, February 'I 7

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ALPIDE Architecture

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ITS Outer Barrel

- Nr. Chips/layer: 6048 (ML), 17740(OL)
- Power density $< 100 \text{ mW} / \text{cm}^2$

Length (mm): 900 (ML), 1500 (OL) Nr. modules/stave: 4 (ML), 7 (OL) Material thickness: ~ 1% X_0 Throughput (@100kHz): < 3Mb/s × cm⁻²

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