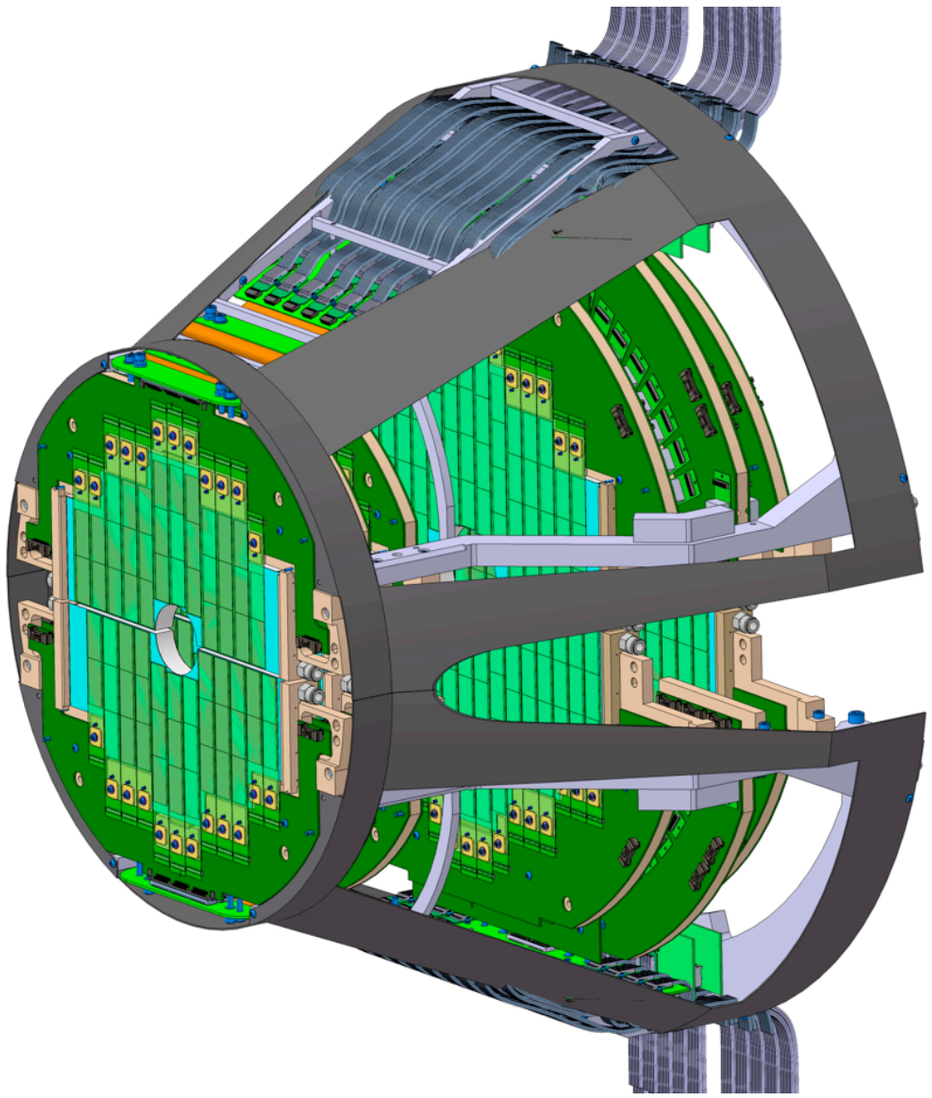
The Muon Forward Tracker
Upgrade of the ALICE experiment



Raphaël Tieulent

Institut de Physique Nucléaire de Lyon

on behalf of the ALICE collaboration

Outline

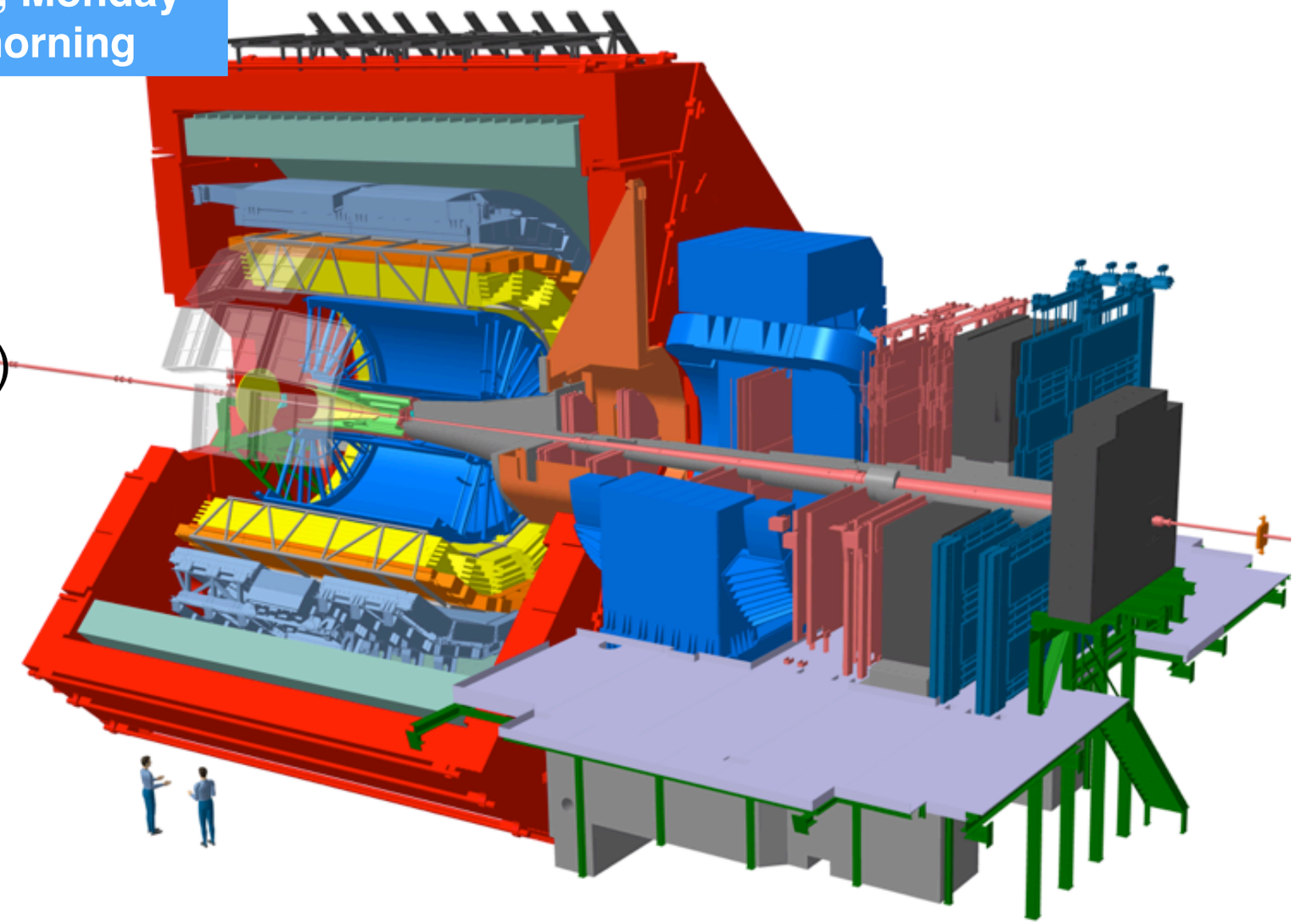
- ALICE detector and its upgrade strategy during LS2
- The Muon Forward Tracker principle
- ALPIDE Chip
- MFT R&D overview
  - Ladder assembly
  - Disk assembly
  - Readout

The ALICE experiment

- LHC experiment dedicated to the study of Heavy Ion collisions
- Detectors designed to identify and reconstruct particles in a large p_T domain (>100 MeV/c)

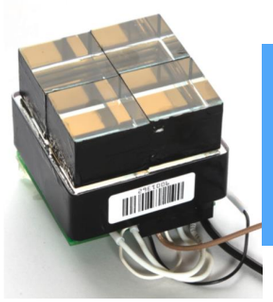
Andrea ALICI talk, Monday morning

- **Central Rapidity (|η|<1)**
  - Tracking (ITS, TPC)
  - PID (TOF, TRD)
  - Calorimetry (EMCAL, PHOS)



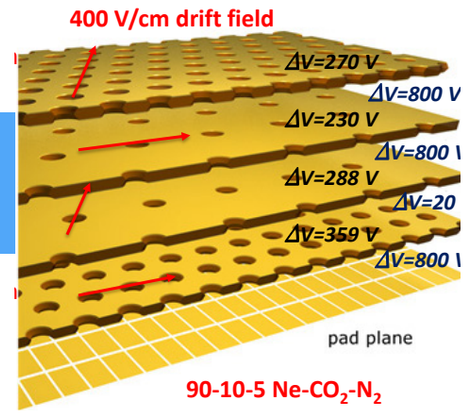
- **Forward Rapidity, muon spectrometer (2.5<η<4)**
  - PID (Muon absorber)
  - Tracking (MWPC)
  - Trigger (RPC)

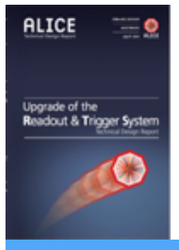
Upgrade strategy for LS2



New Minimum Biais trigger detector

New TPC GEM Chambers

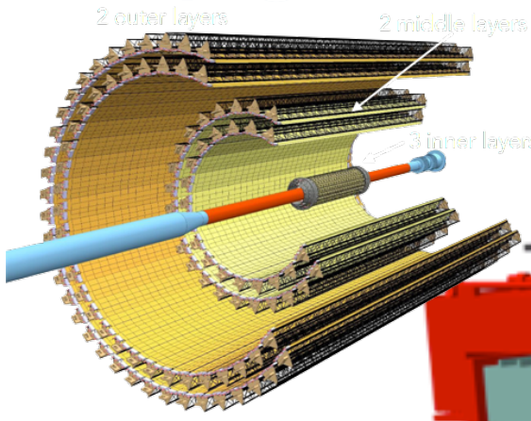




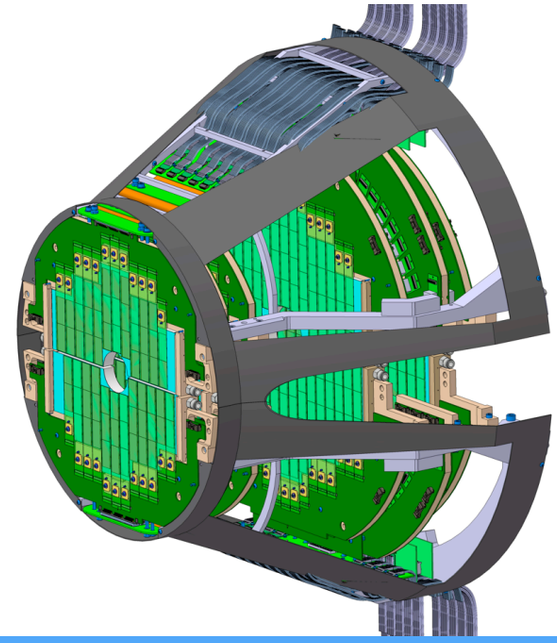
New Readout system

New Online/ Offline Computing

Upgrade strategy for LS2

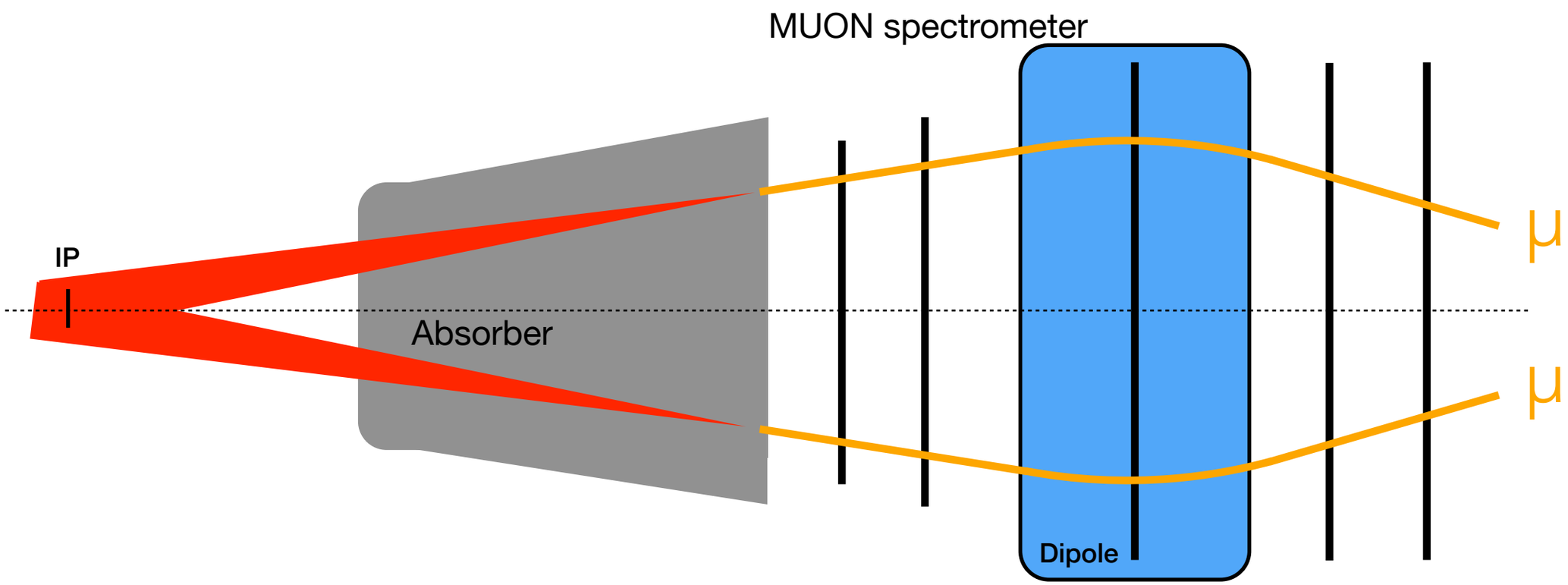


New Central Inner Tracking System
High resolution ; low material budget



New Muon forward Tracker
High resolution ; low material budget

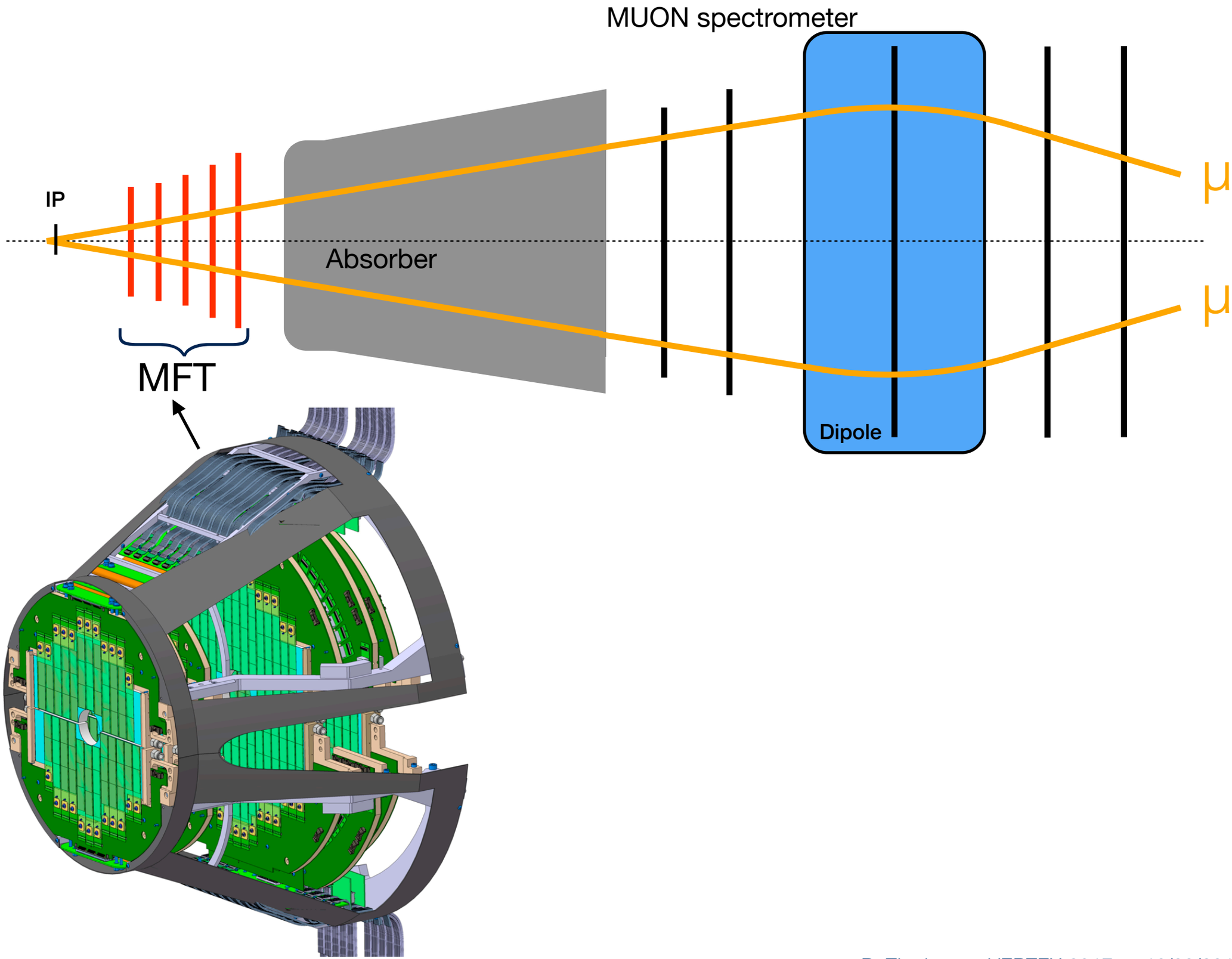
The Muon Forward Tracker



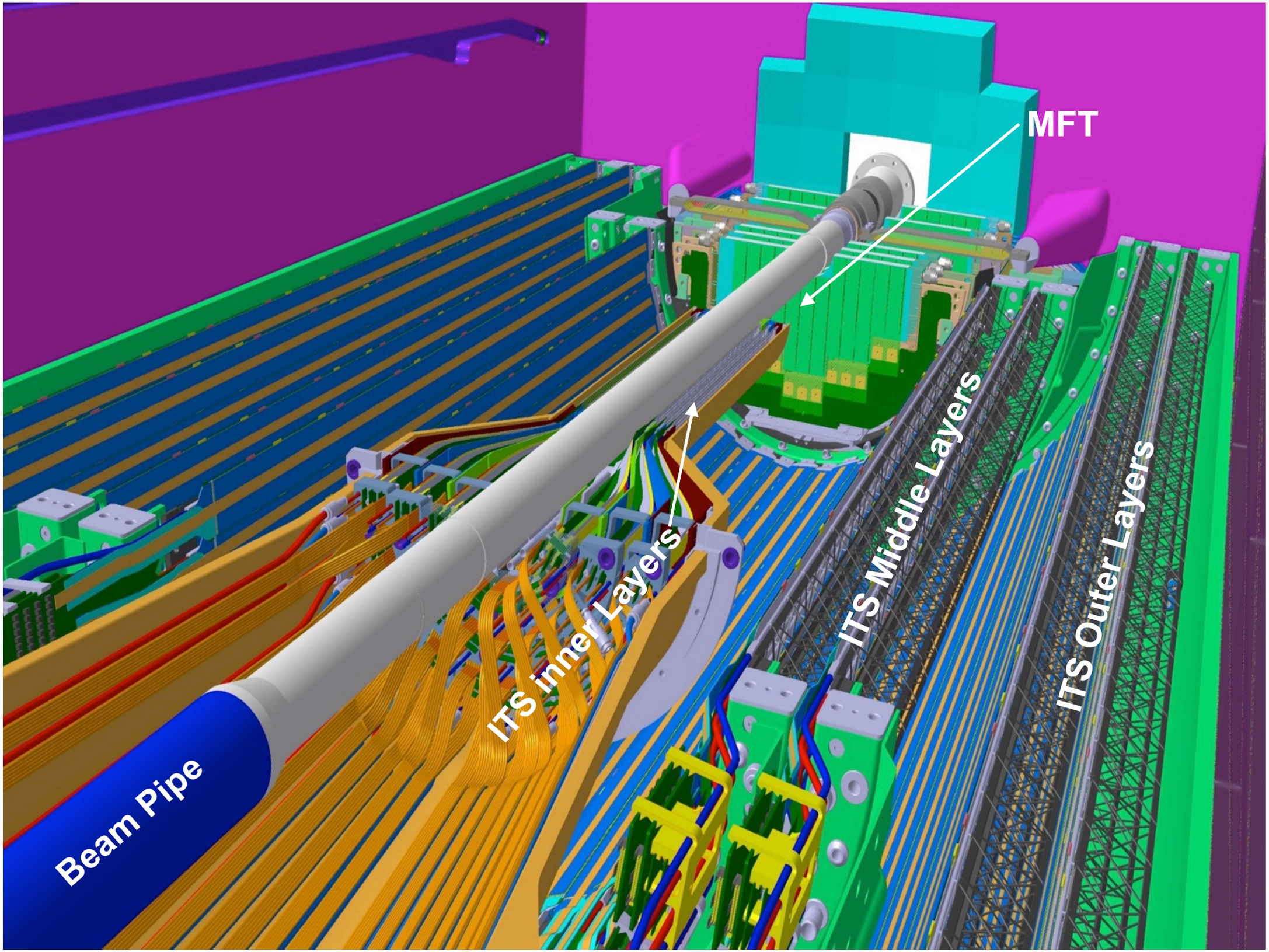
Present MUON spectrometer blurred in muon track extrapolation

- No constraint in the primary vertex region (no charm/beauty separation)

The Muon Forward Tracker



The ALICE inner trackers



MFT design goals

Vertexing for the Muon Spectrometer at forward rapidity

- 5 detection disks with detection on both side, O(5 μm) spatial resolution
- 0.7% of X_0 per disk
- $-3.6 < \eta < -2.45$
- Disk#0 at z = -460 mm, R_{in} = 25 mm (limited by the beam-pipe radius)

Good matching efficiency between MFT and Muon Spectrometer

- Disk#4 at z = -768 mm (limited by the frontal absorber).

Fast electronics read-out

- Pb-Pb interaction rate ~50 kHz, pp interactions ~200 kHz
- Integration time and dead-time < 20 μs

MFT Layout

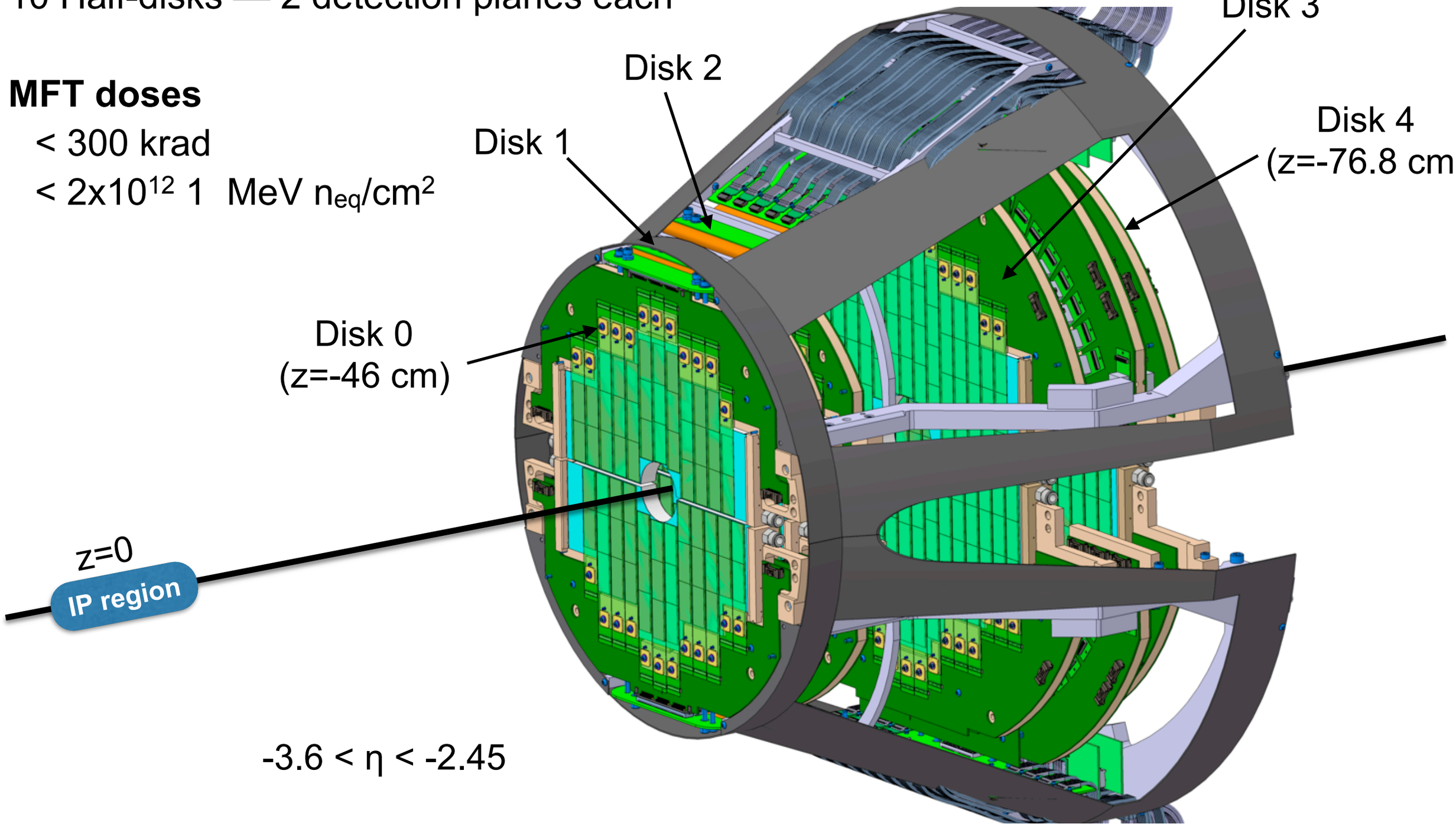
920 silicon pixel sensors (0.4 m^2) on 280 ladders of 2 to 5 sensors each

10 Half-disks — 2 detection planes each

MFT doses

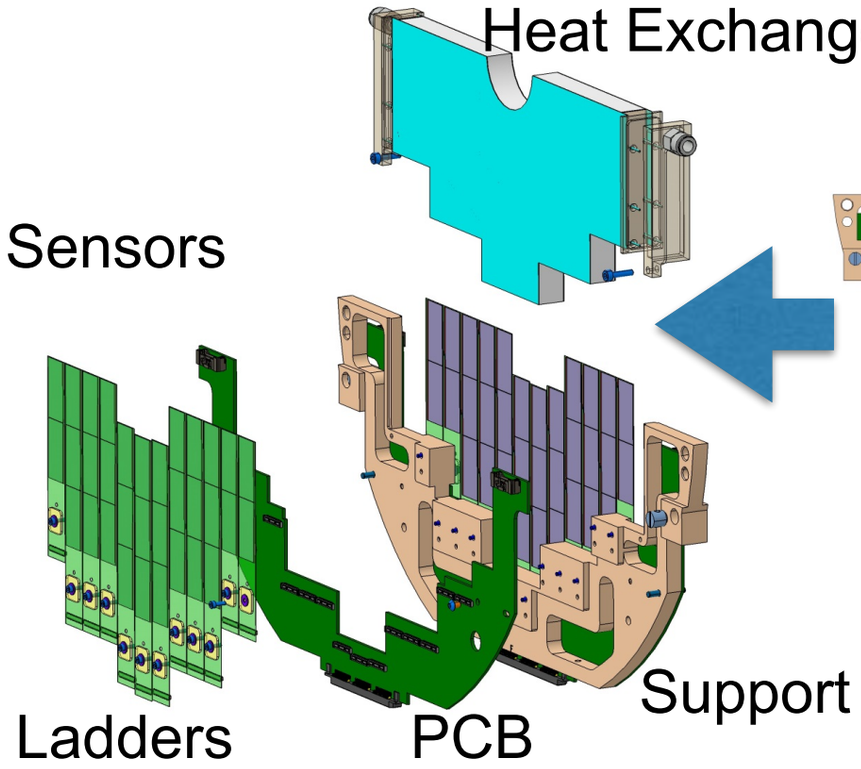
< 300 krad

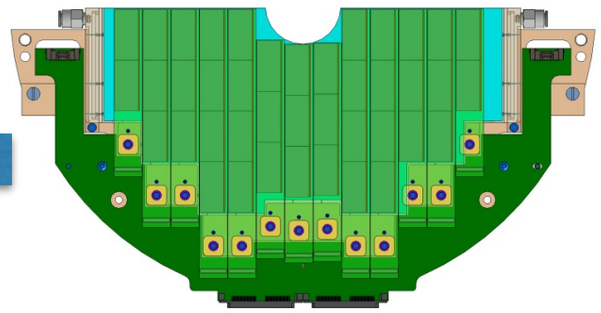
< 2x10^{12} 1 MeV n_{eq}/cm^2

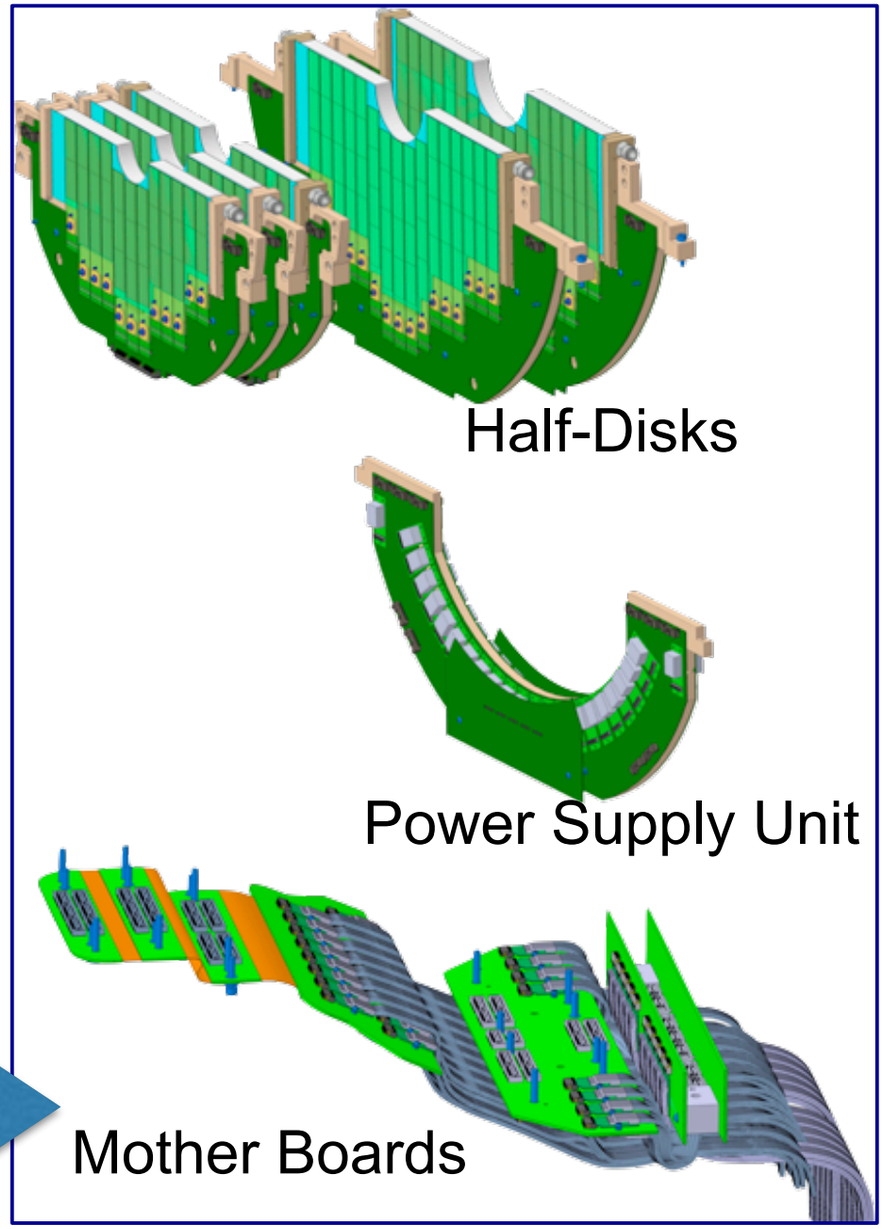


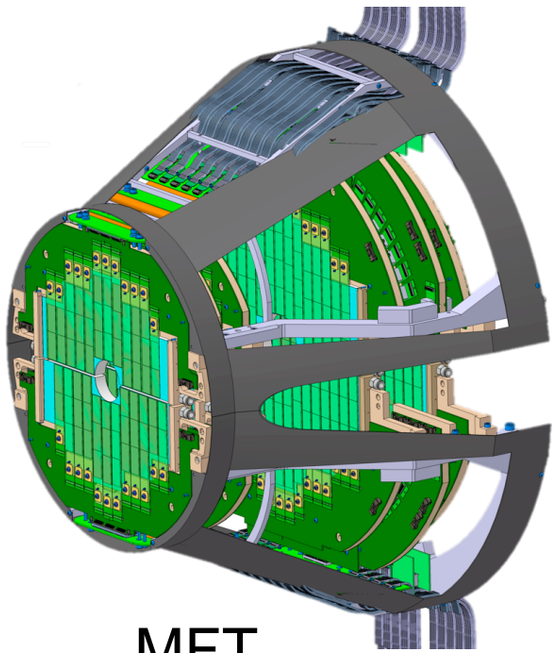
-3.6 < η < -2.45

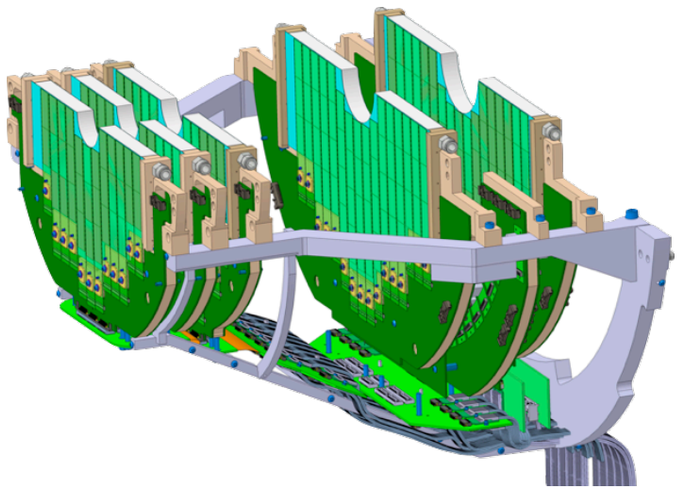
MFT Layout



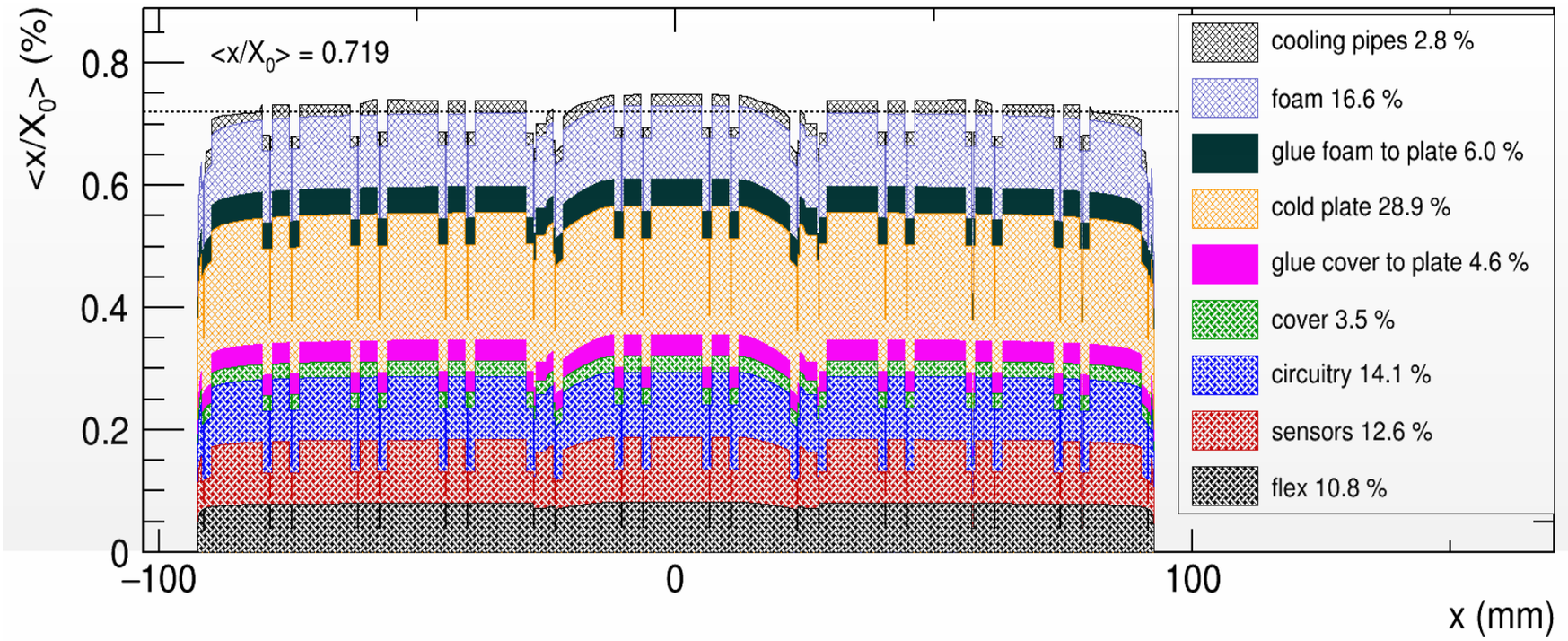

Half-Disk




MFT


Half-MFT cone

Material Budget



Ladder contribution (two sides): 0.3%

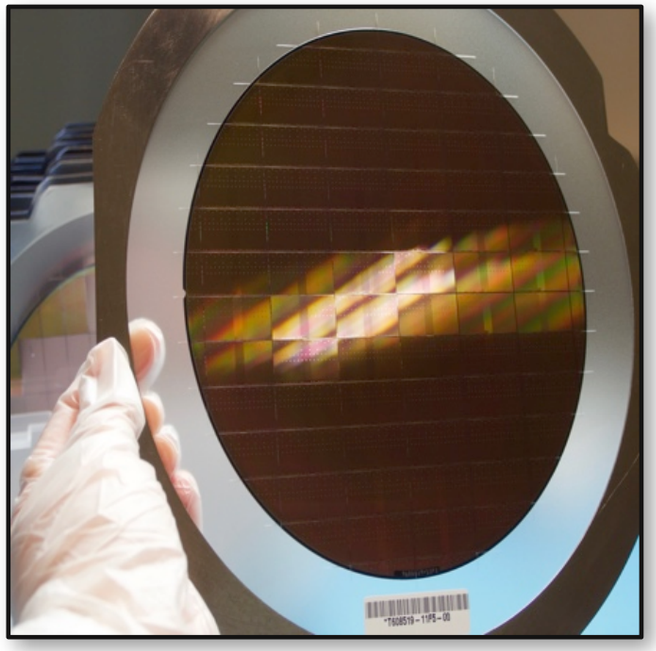
- Sensor: 0.09%
- Flex substrate: 0.08%
- Al circuitry: 0.1%

Total Disk: 0.7% of X_0

ALPIDE pixel sensor characteristics

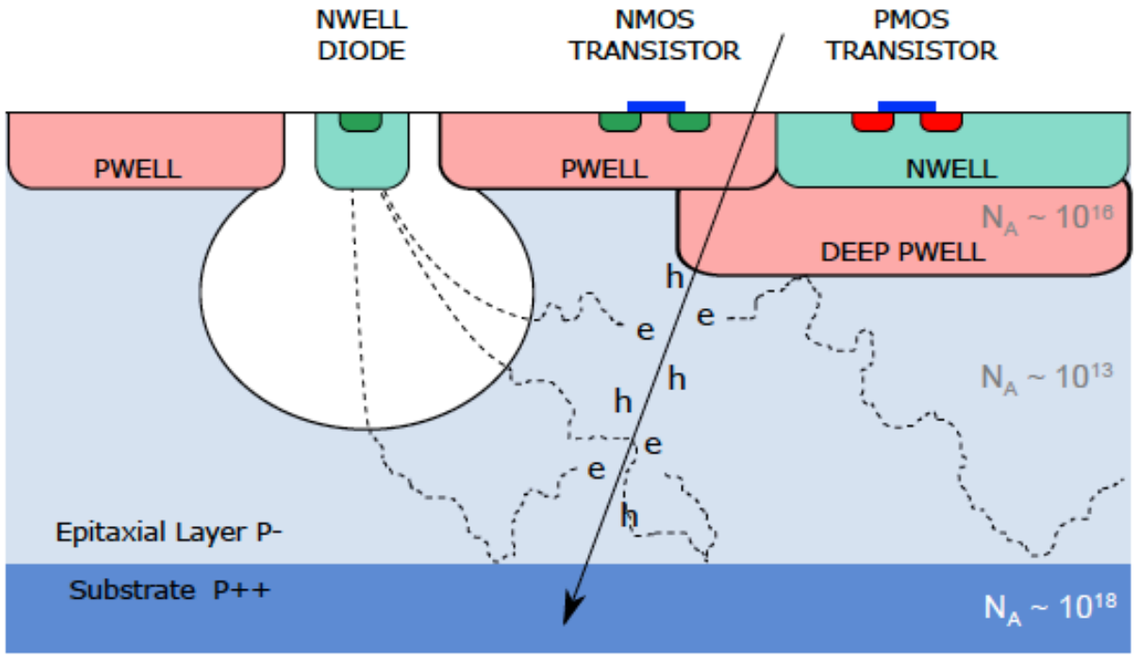
CMOS Monolithic Active Sensors (MAPS), TowerJazz 0.18 µm technology

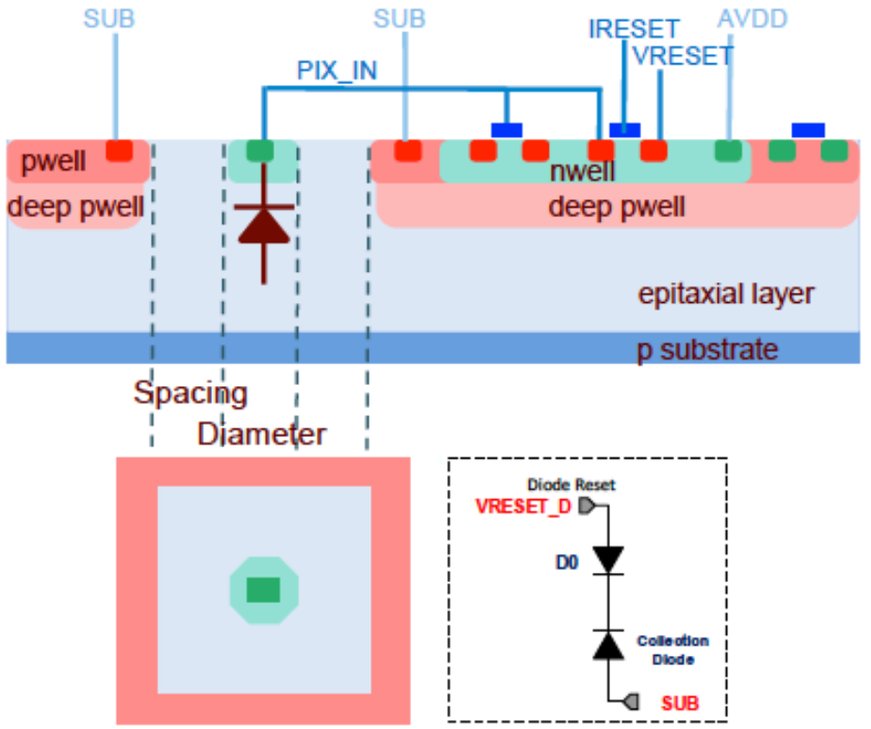
- Sensor Thickness 50 µm
- Sensor Size 15 mm x 30 mm. Pixel pitch 29 µm x 27 µm
- Spatial Resolution 5-6 µm
- Event time resolution ~ 2 µs
- Low power consumption ~40 mW/cm^2
- Expected radiation load in ALICE Run3 and Run4 <300 krad, <2.0x10^{12} 1 MeV n_{eq}/cm^2
- In-pixel amplification/discrimination/multi-event buffering
- In-matrix zero suppression
- Triggered or continuous acquisition
- High speed serial data output up to 1.2 Gb/s



ALPIDE Production started December 2016

ALPIDE Technology

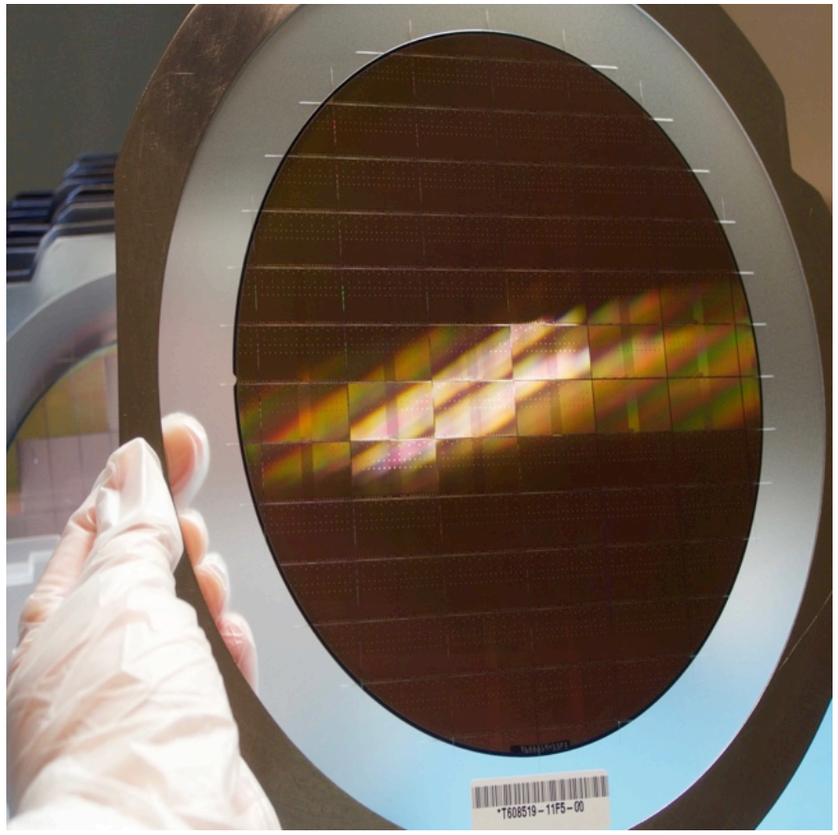


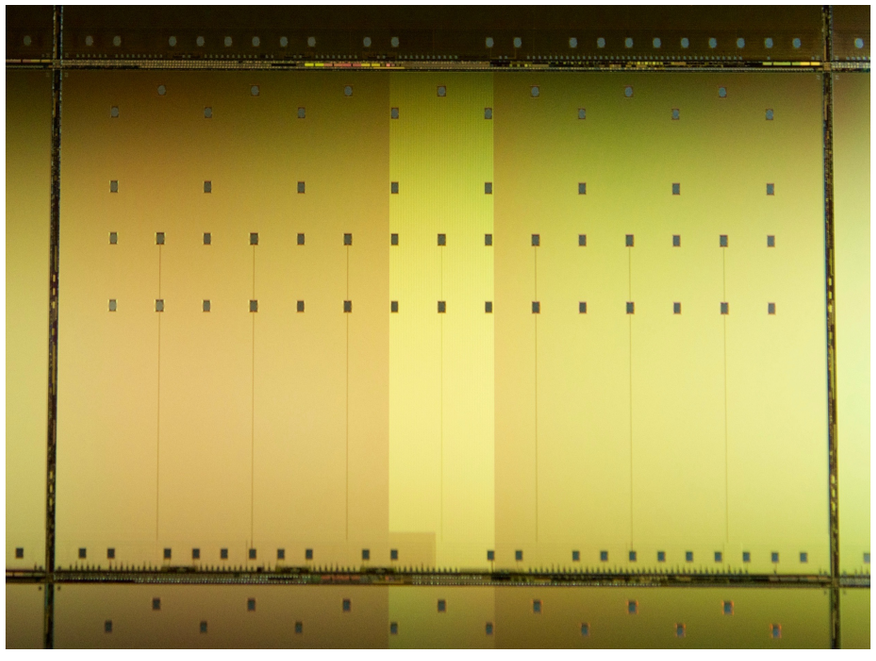


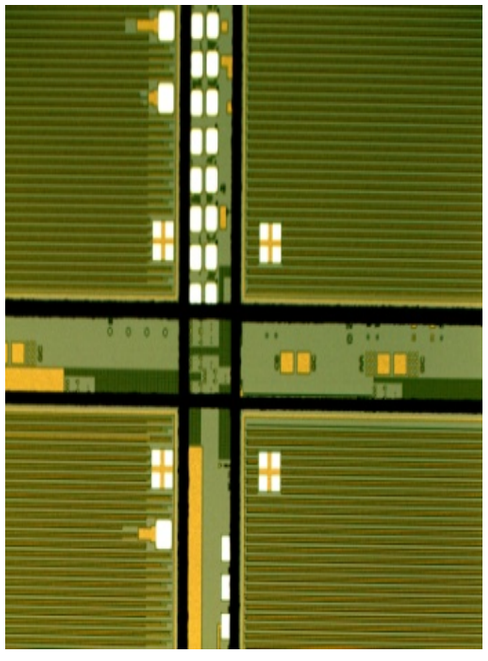
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25µm) on p-type substrate
- Small n-well diode (2 µm diameter), ~100 times smaller than pixel => low capacitance (~fF)
- Reverse bias voltage (-6V < V_{BB} < 0V) to substrate (contact from the top) to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors (full CMOS circuitry within active area)

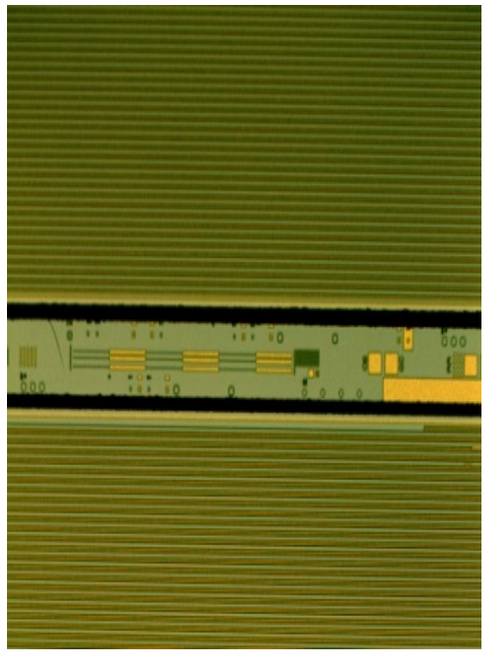
ALPIDE production

- ALPIDE production started December 2016
- Wafers are delivered on tape, mounted on a dicing frame
- Double cuts to separate the chips from their neighbors

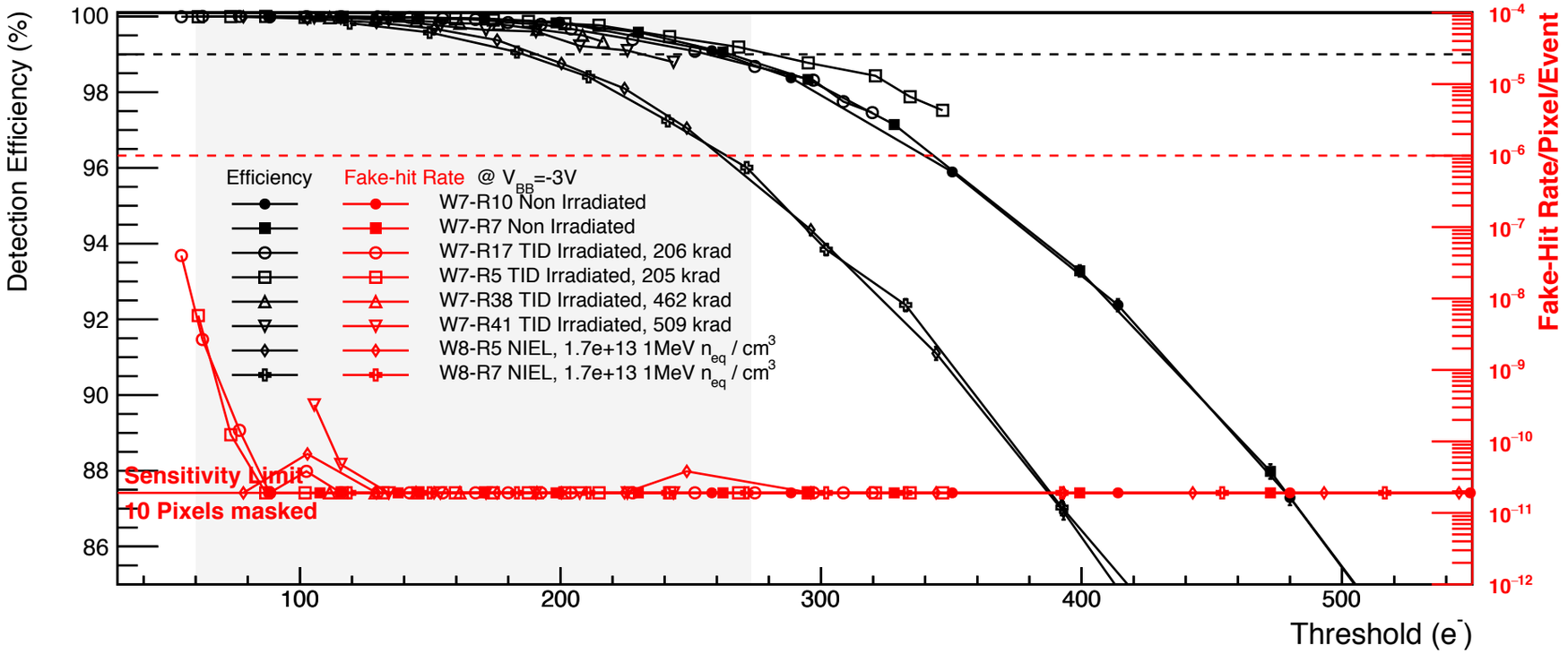




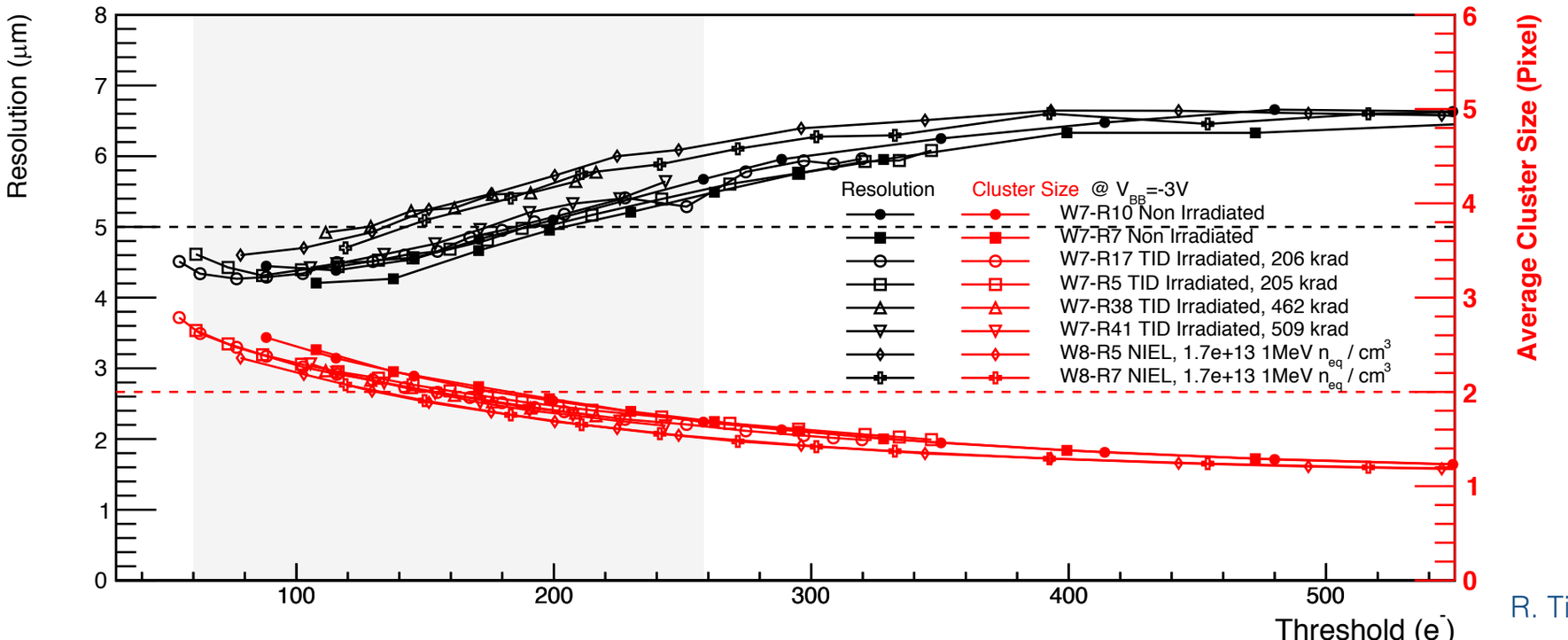




ALPIDE test beam results



- High detection efficiency > 99%
- Very low fake hit rate

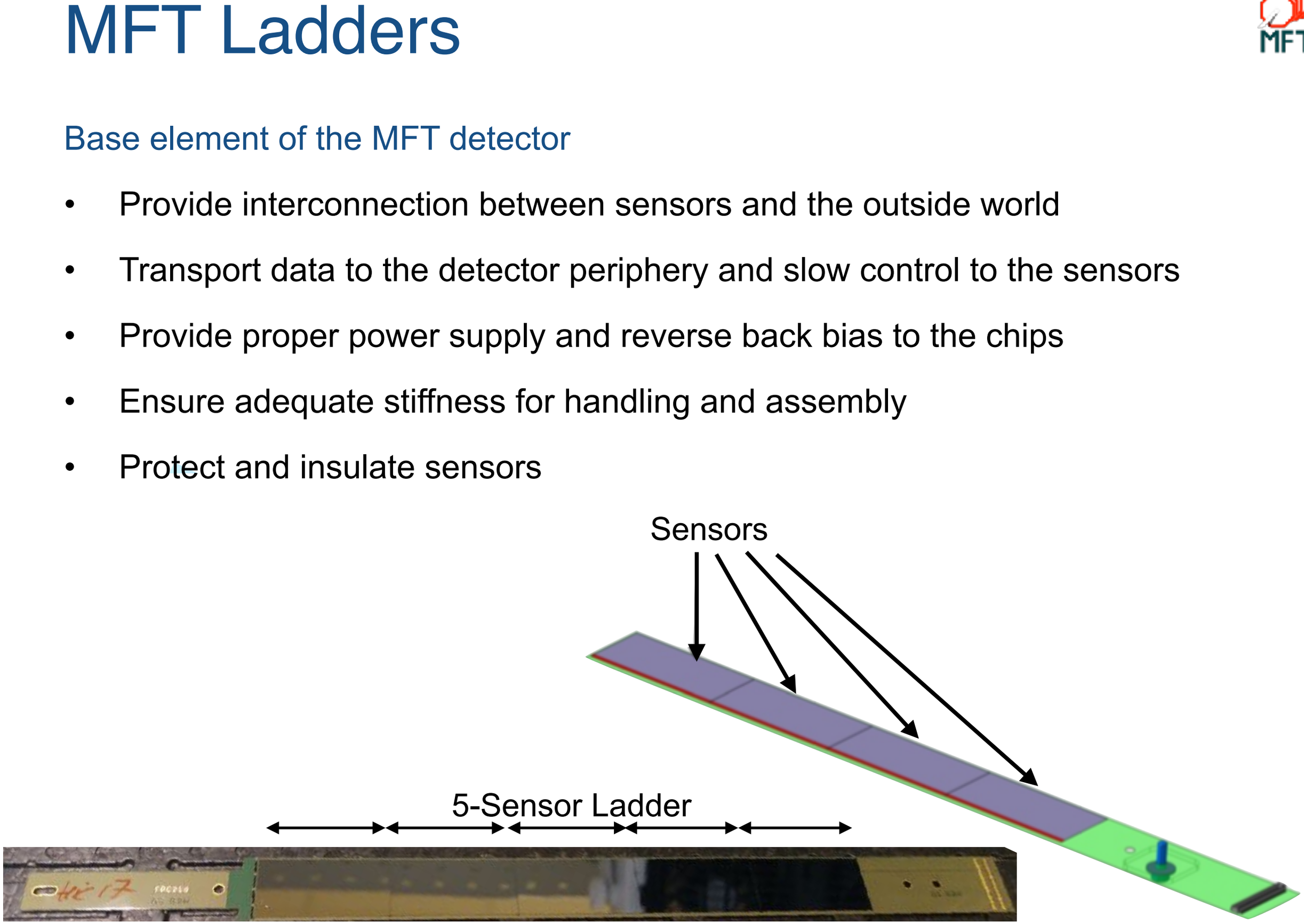


- Spacial resolution ~5-6μm
- Cluster size ~1-2 pix

MFT Ladders

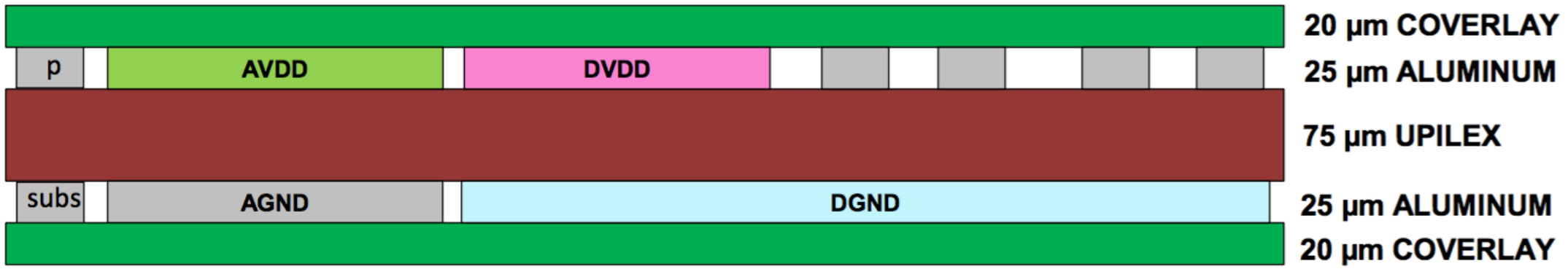
Base element of the MFT detector

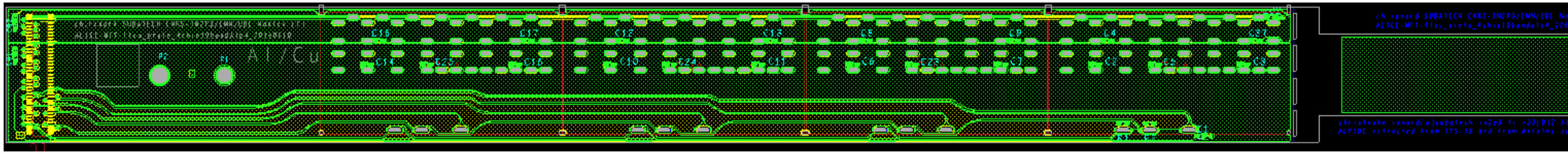
- Provide interconnection between sensors and the outside world
- Transport data to the detector periphery and slow control to the sensors
- Provide proper power supply and reverse back bias to the chips
- Ensure adequate stiffness for handling and assembly
- Protect and insulate sensors



Flex Printed Circuit

Sensors are interconnected to a Aluminum Flexible Printed Circuit (FPC)





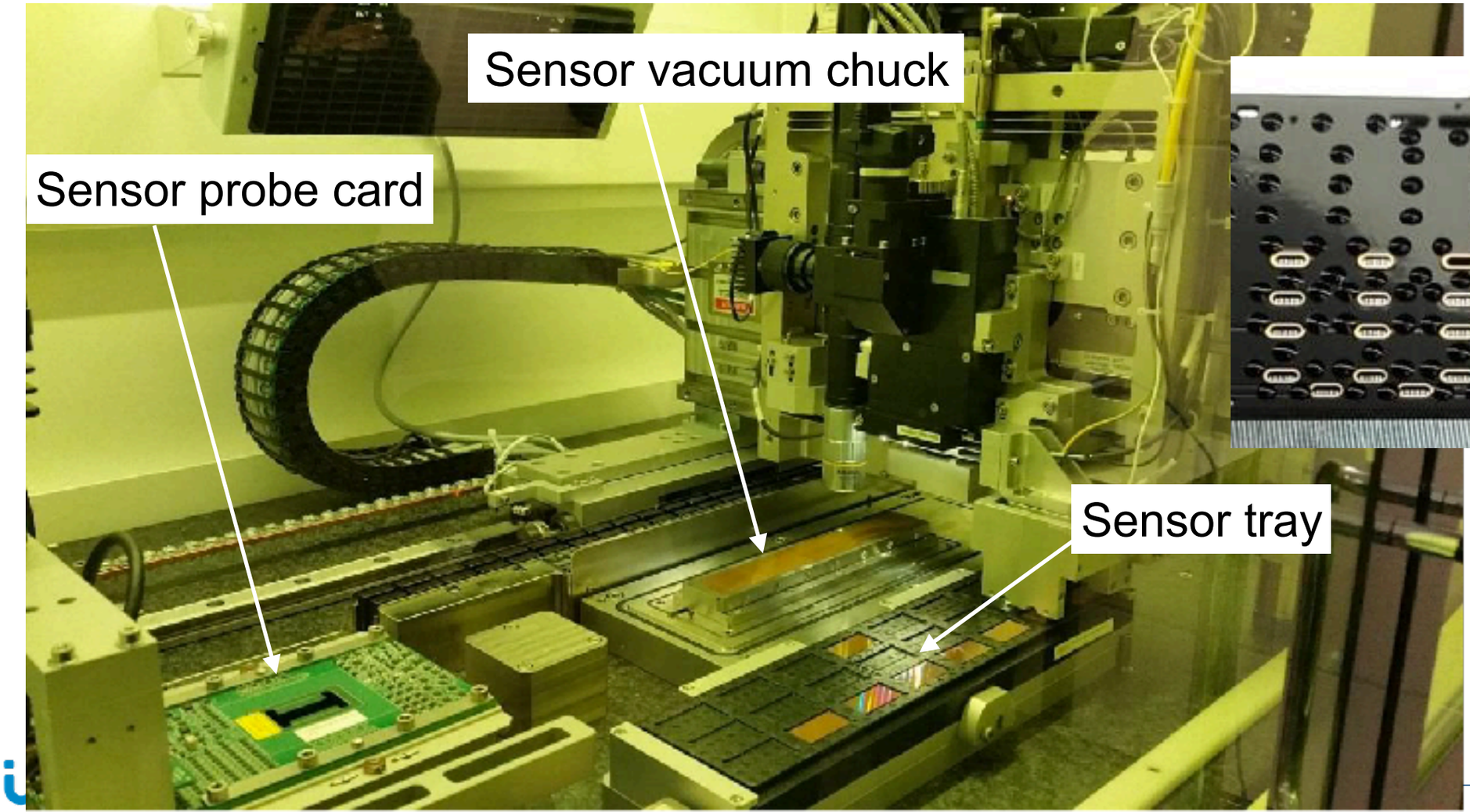
Connector to Disk | Sensor 0 | Sensor 1 | Sensor 2 | Sensor 3

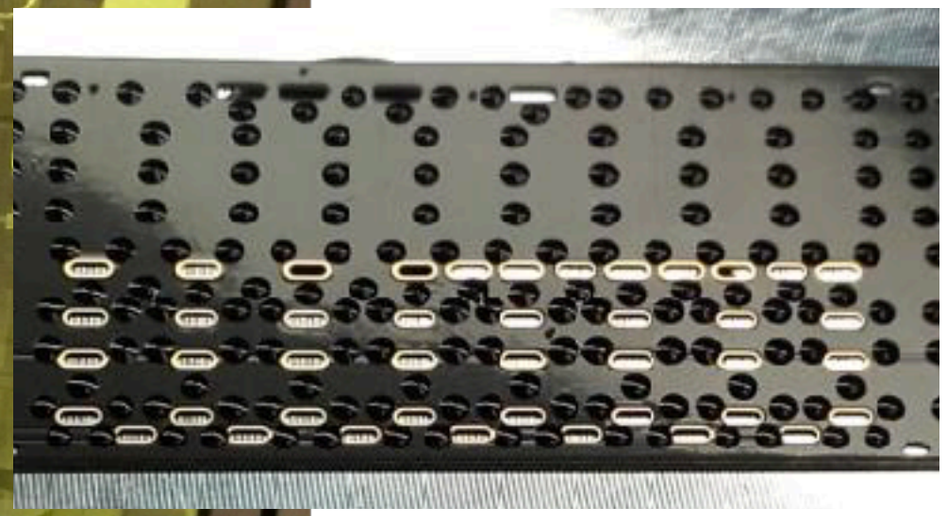
- Ensure data, slow control, reverse back bias and power supply from/to the sensors
- Choice of Al and thickness: minimize material budget and voltage drop (impedance 100 Ω)

Ladder assembly - Chip Gluing

Automatic sensor positioning/gluing on FPC using a Module Assembly Machine

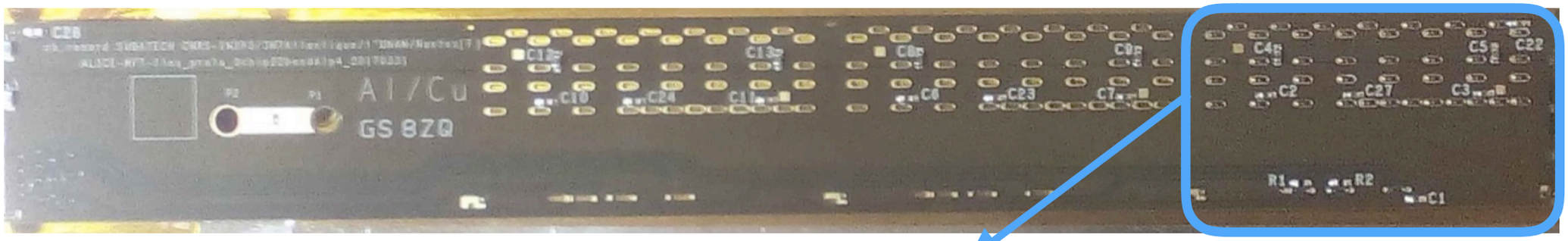
- Automatic chip picking from the tray
- Precise (5 µm) and automatic alignment on the chip vacuum chuck
- If needed, electrical test of the chip (probe card station available)
- Visual inspection of chip quality (edges,…) and alignment correction

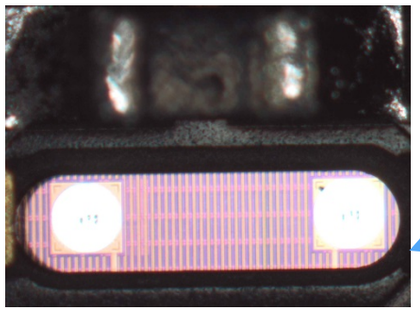




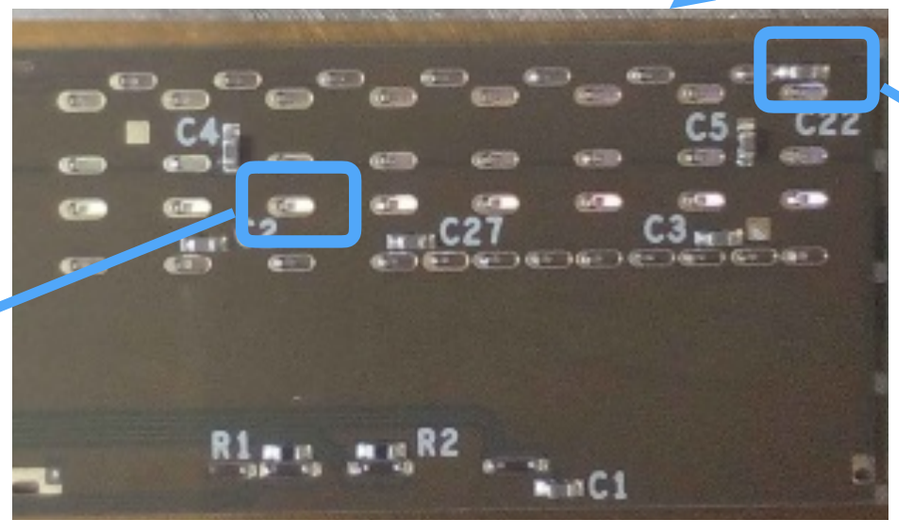
Glue dots deposition using a mask

Ladder assembly - Wire Bonding

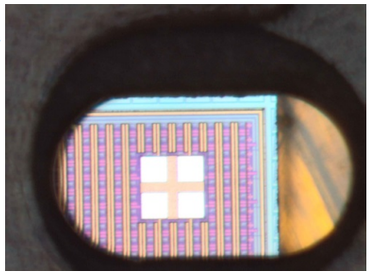




Chip bonding pads

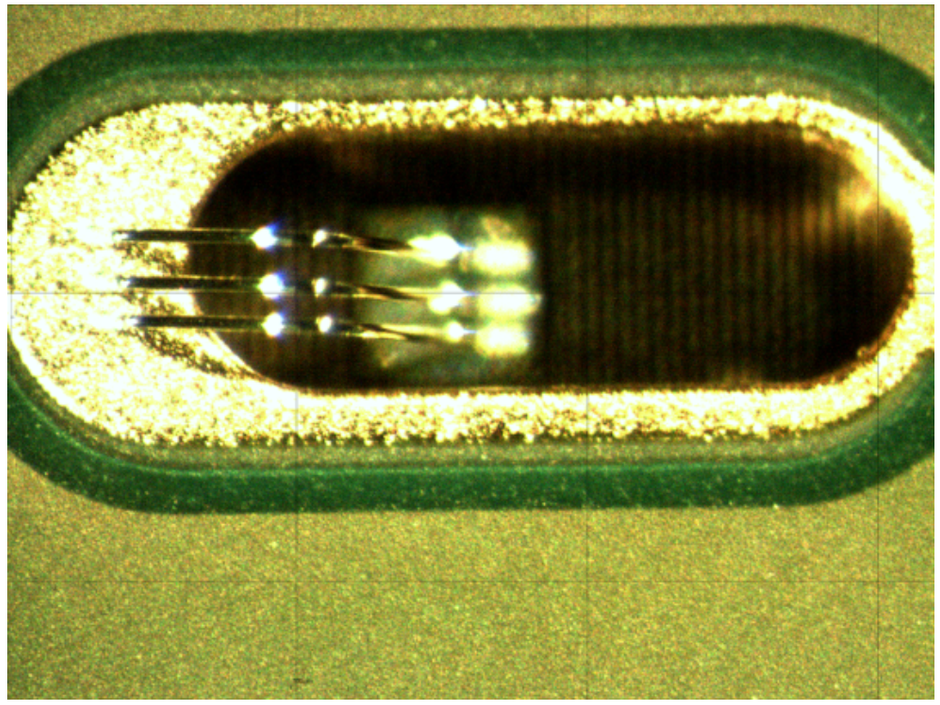


Positioning target on the chip



Bonding performed at CERN bonding lab

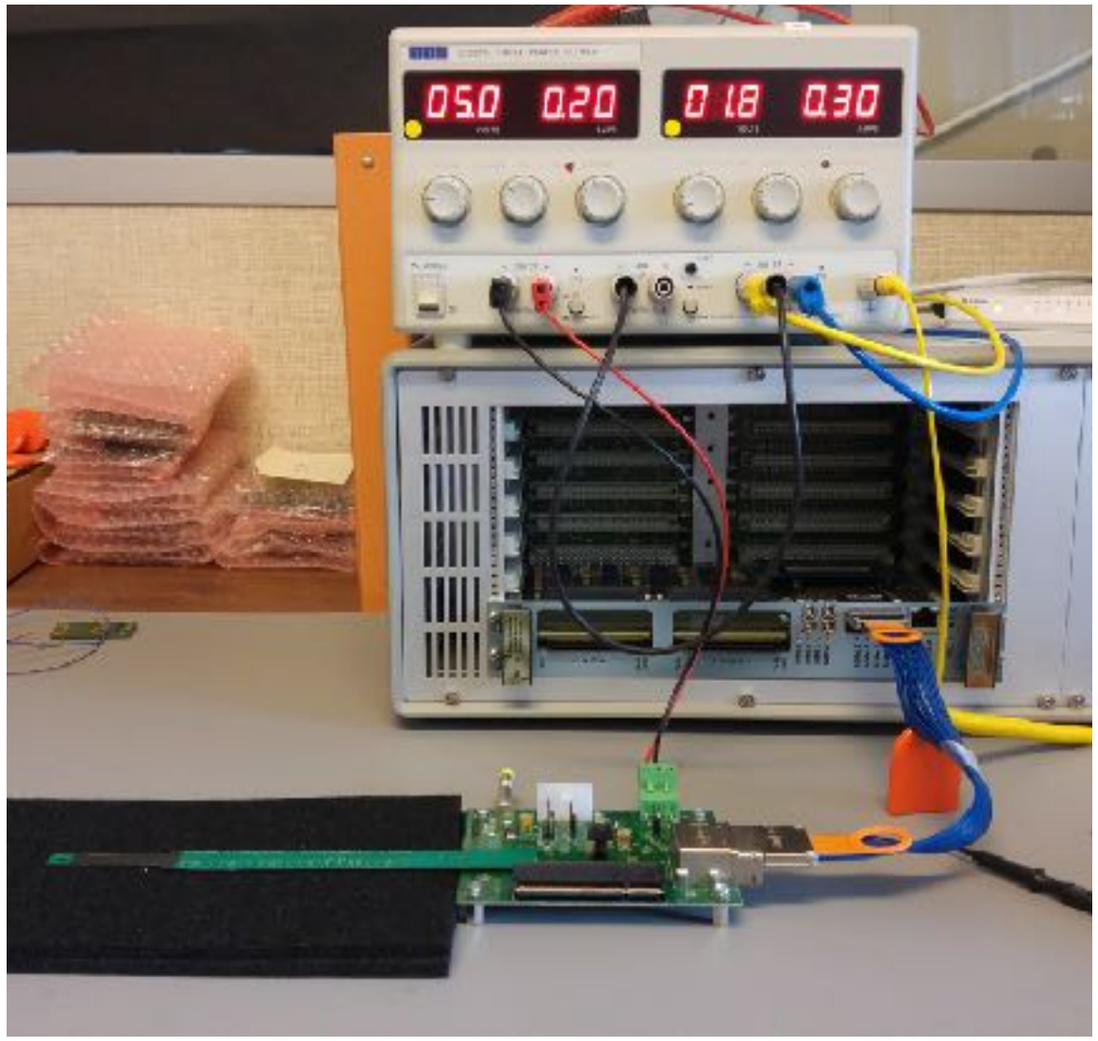
- Prototype production on-going, process optimization
- Production Readiness Review scheduled Oct'18

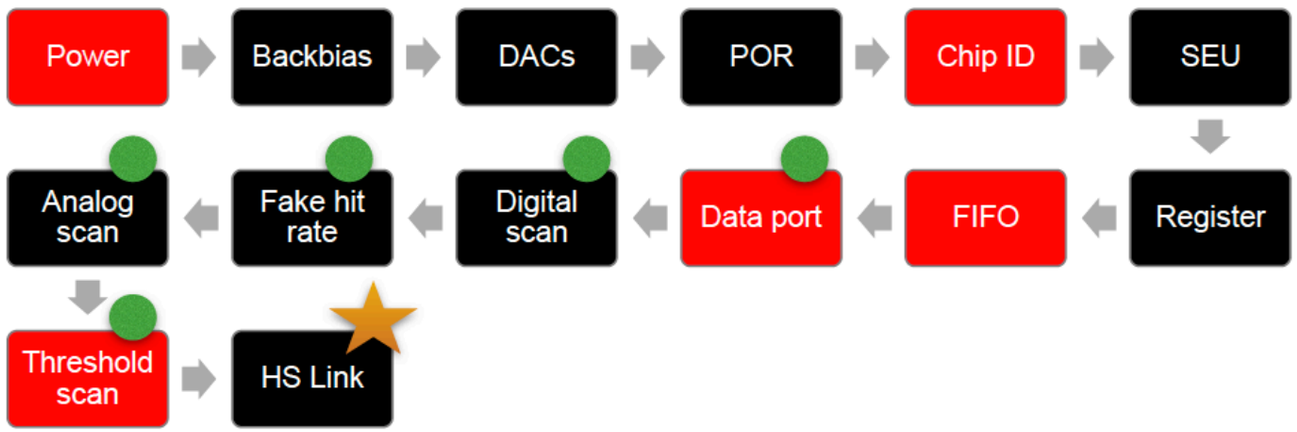


MFT Ladder qualification

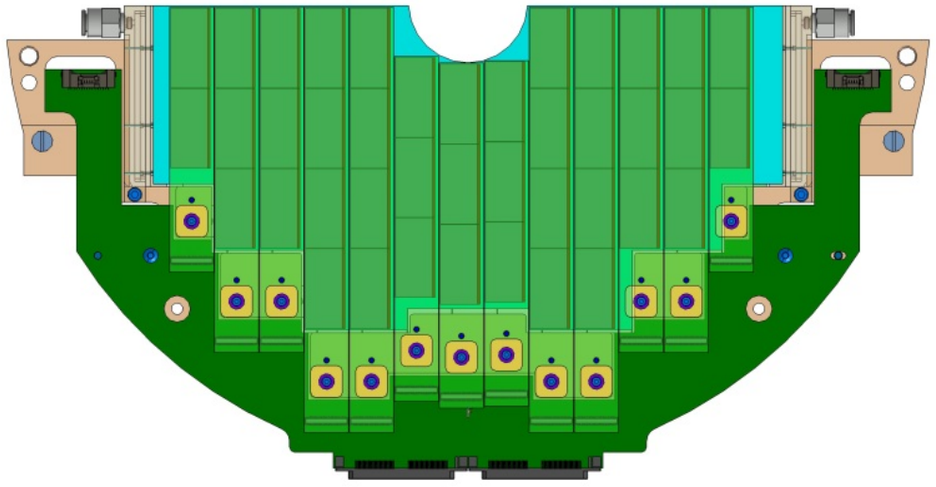
Ladder test bench fully operational

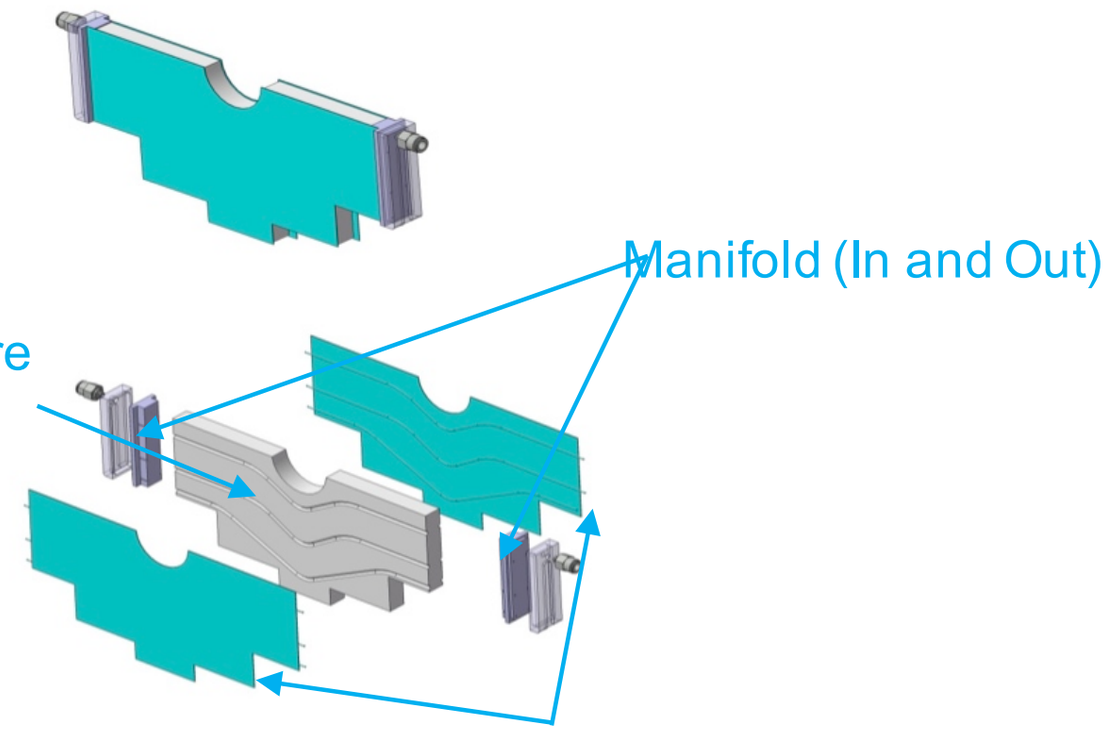
- Definition of the mass qualification process on-going
  - Definition of tested parameters
  - Operational threshold and margins definition
  - Automatic filling of QA database





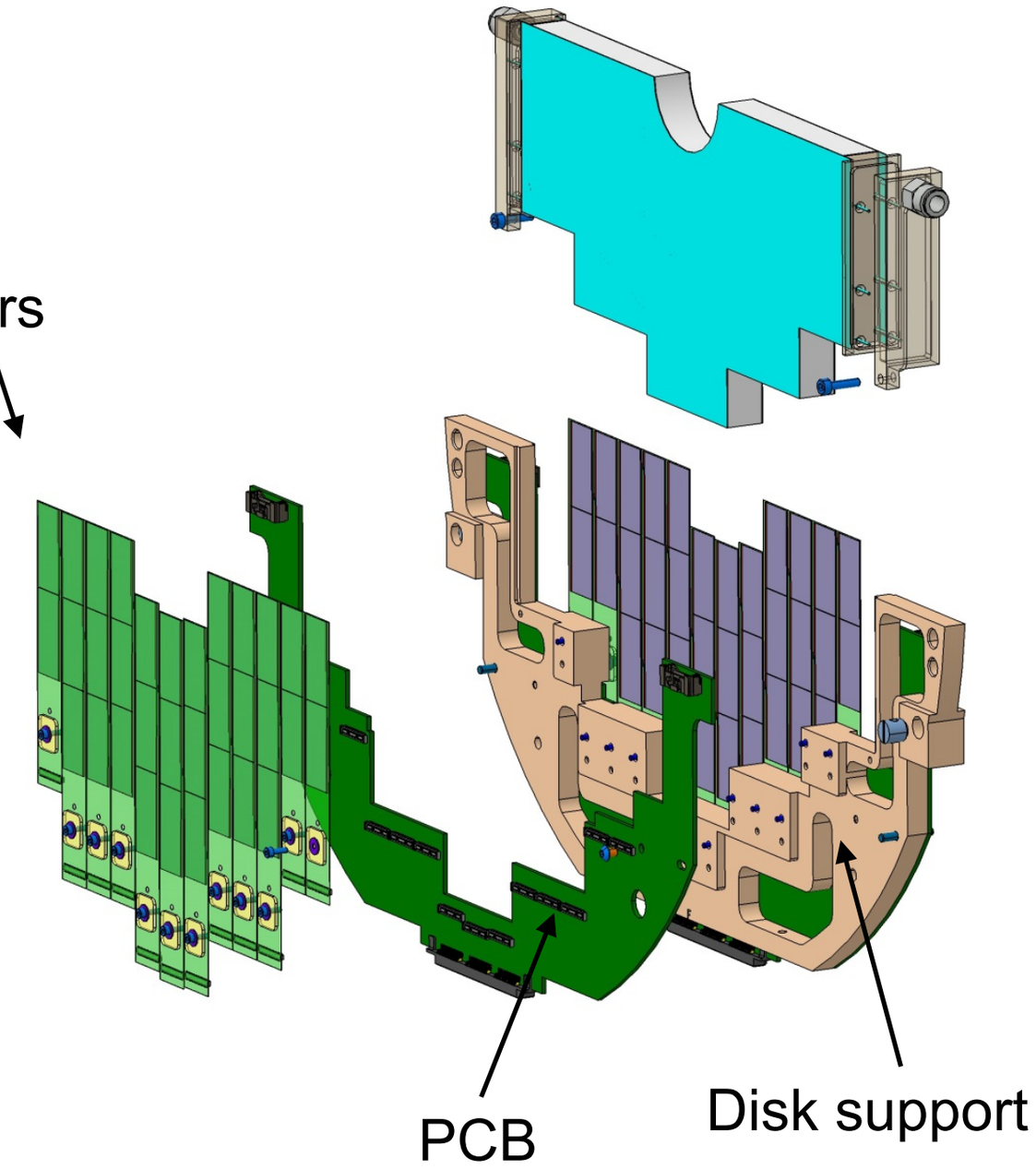
MFT Disk Structure





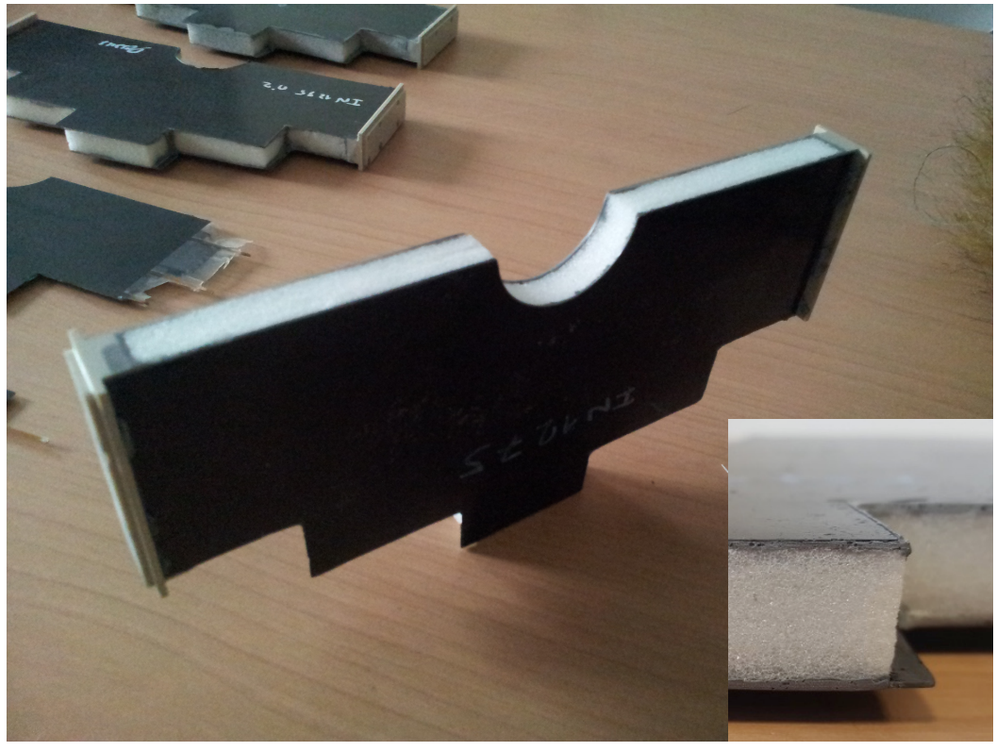
Heat exchanger

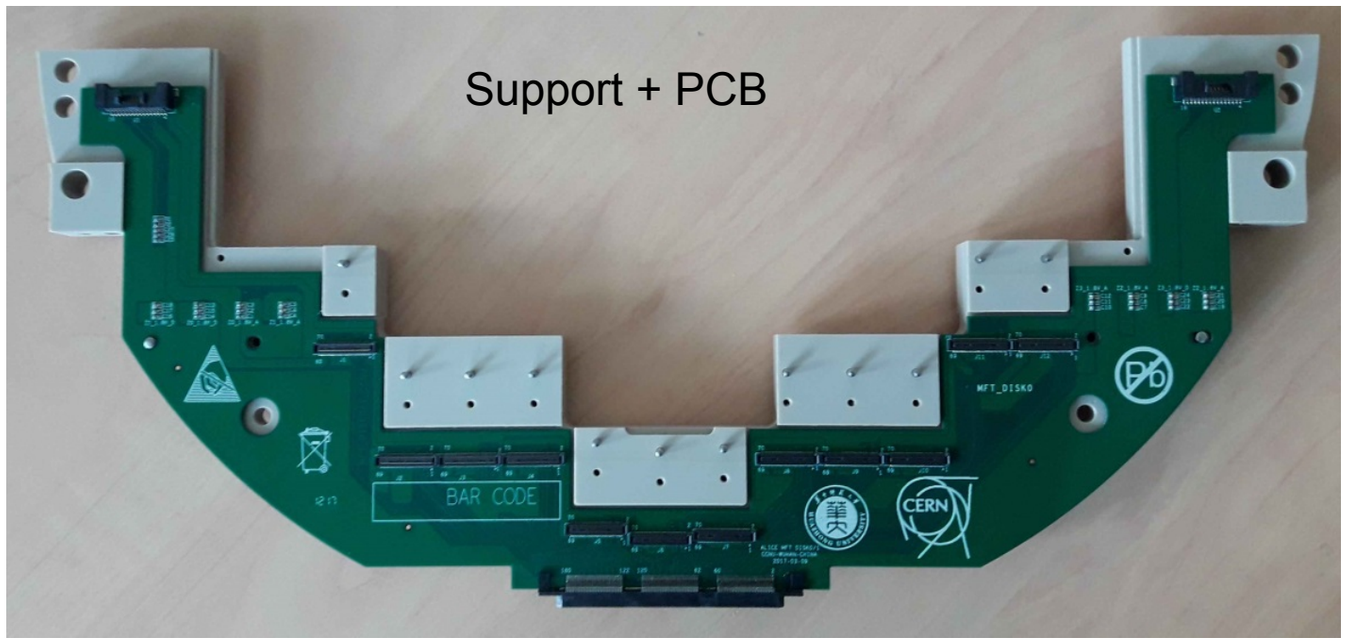
Ladders

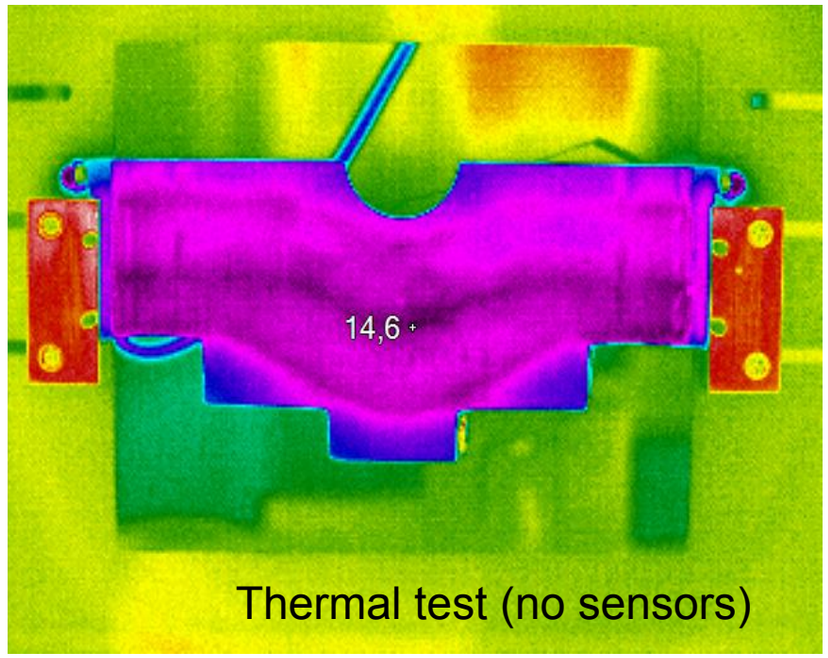


Disk Prototyping and tests

- Disk Prototyping performed
- Results from thermal test bench positive
- Disk Production Readiness Review scheduled Dec' 17







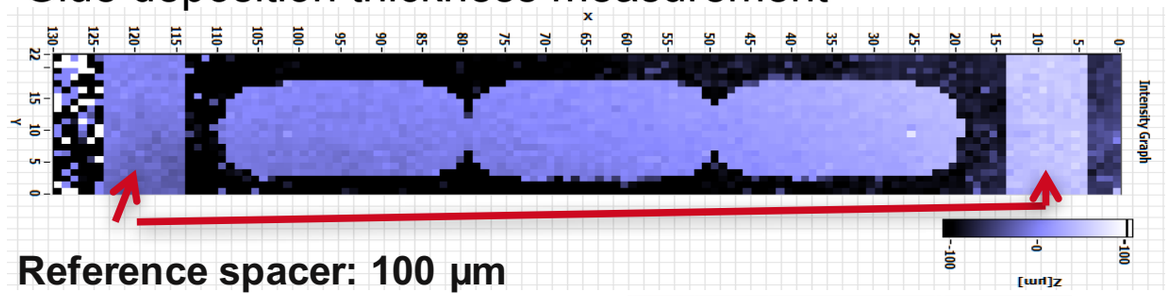
MFT Half-Disk Assembly

Automatic glue deposition by the robot

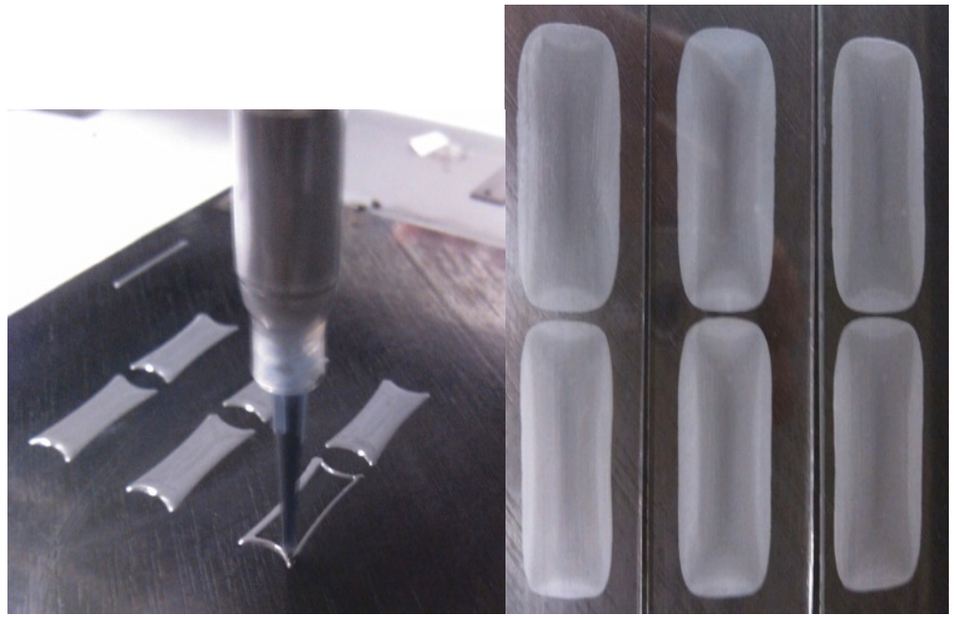
Ladder are glued on heat-exchanger
(Dow Corning SE4445 CV Thermally Conductive)

Finalization of the assembly process

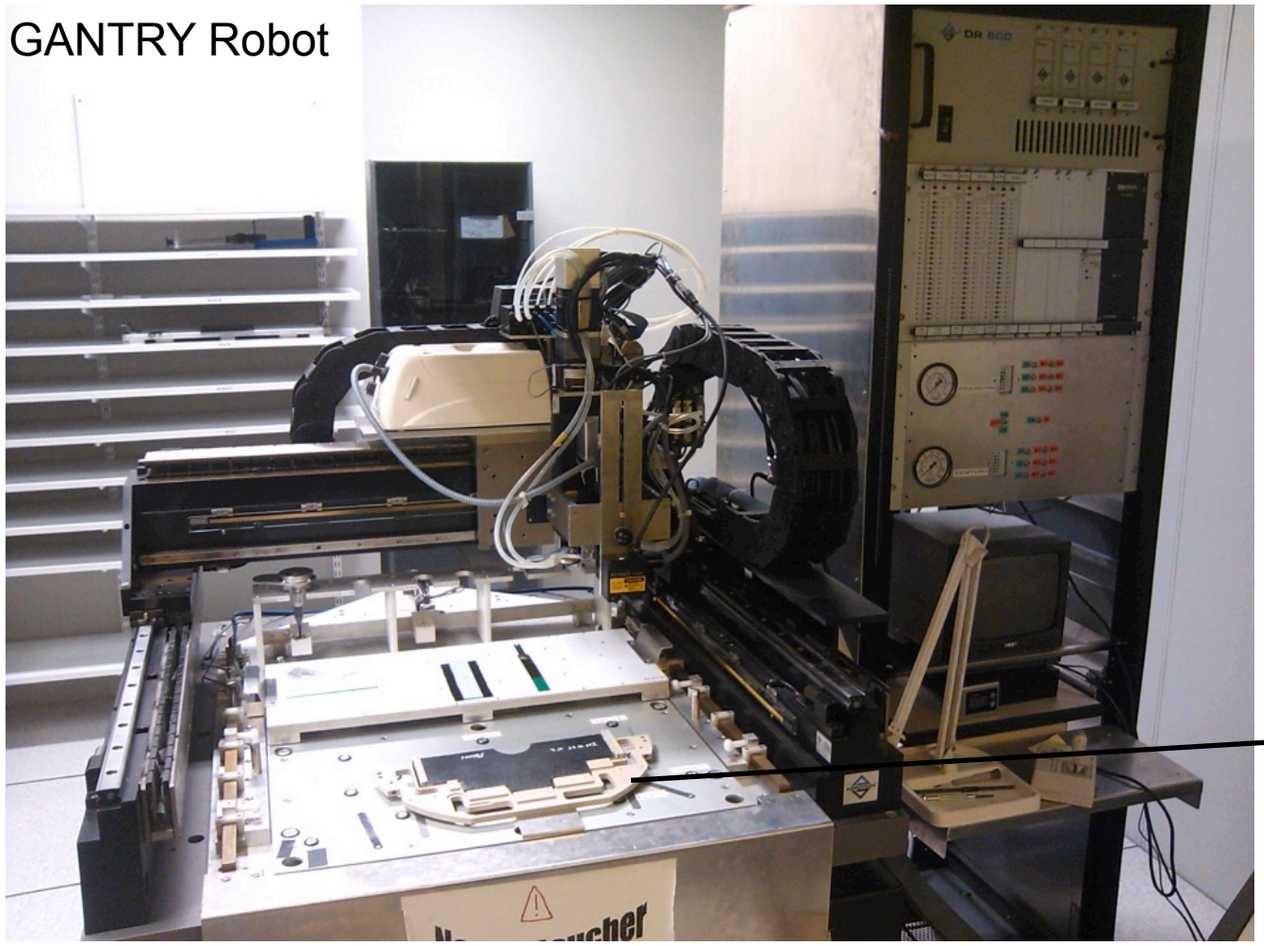
Glue deposition thickness measurement

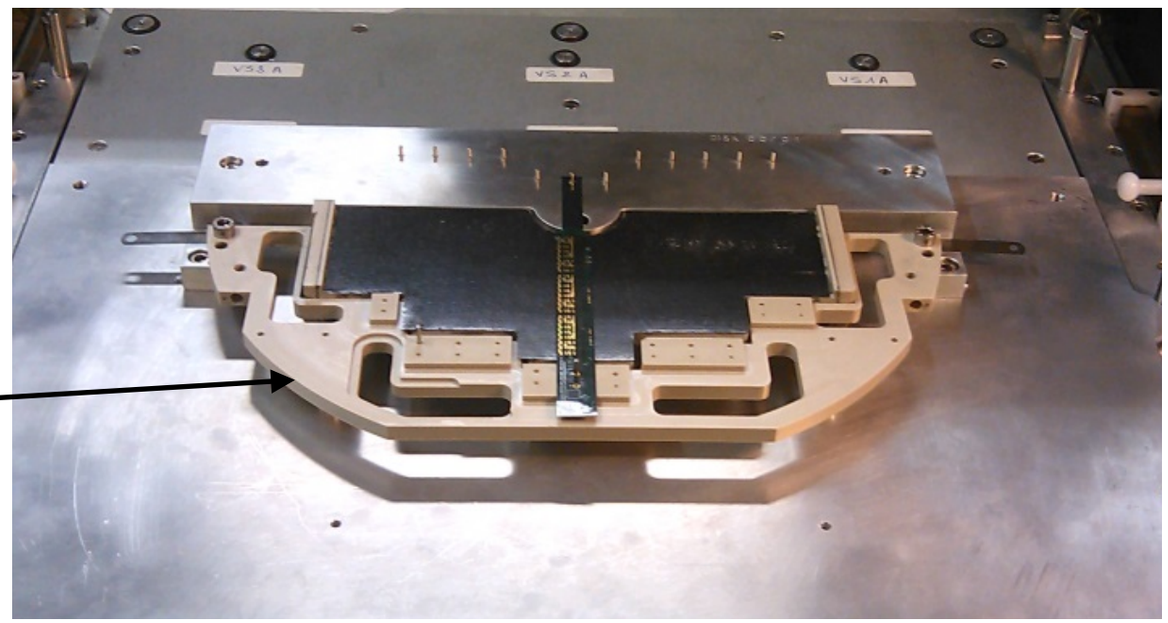


Reference spacer: 100 µm

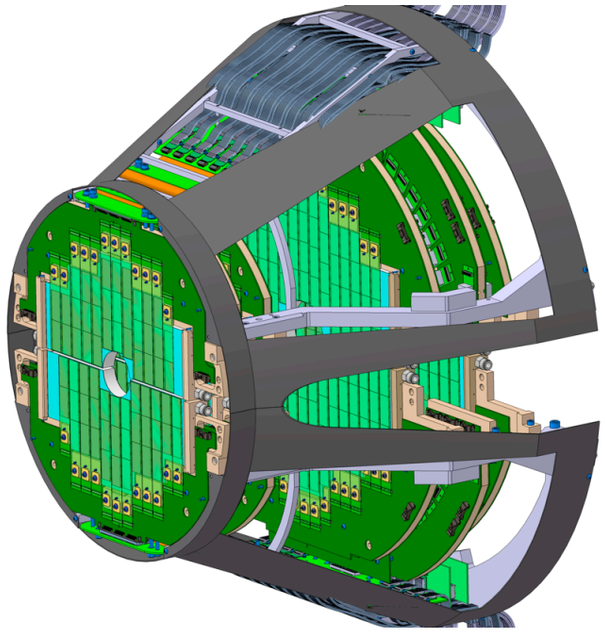


GANTRY Robot





MFT Readout



Copper links

1.2 Gb/s high speed data

80 Mb/s clock and control

Central Trigger Processor

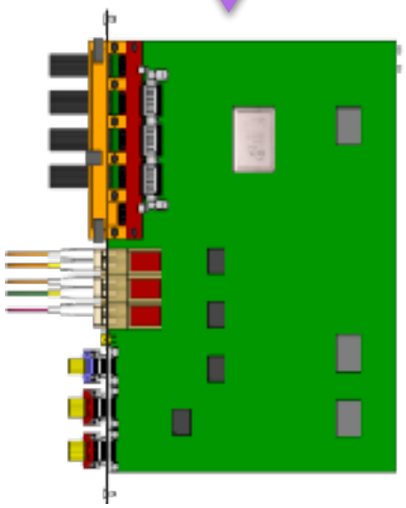
GBT optical

Trigger

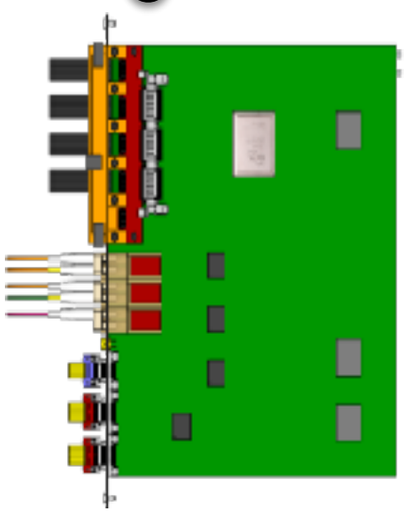
Clock

Control

Data



x80 Readout Units



GBT optical

Control

Data

Control

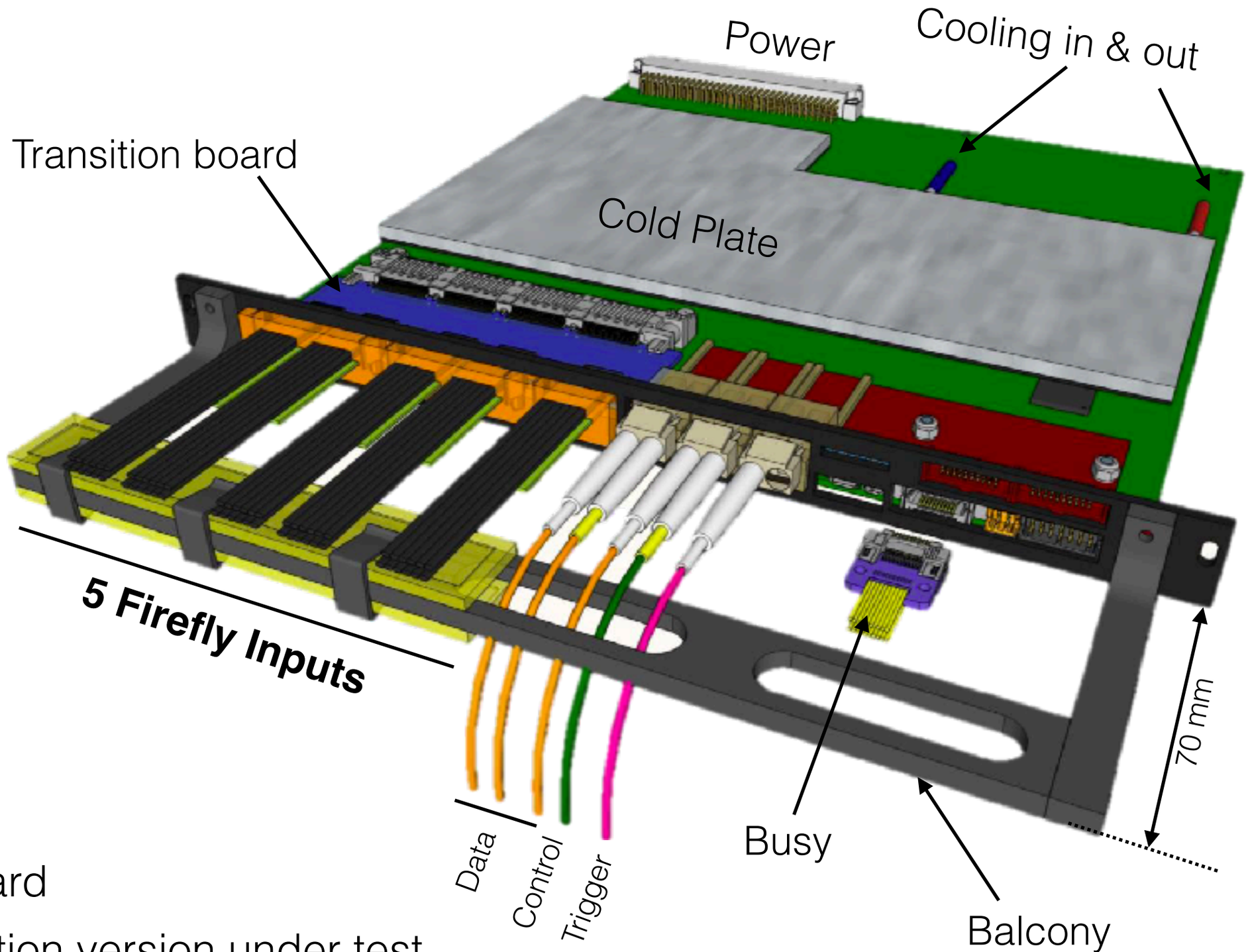
Data

GBT optical

Data Acquisition and Detector Control System (Common Readout Unit)

Readout Unit

Readout Unit Common to ITS upgrade and MFT



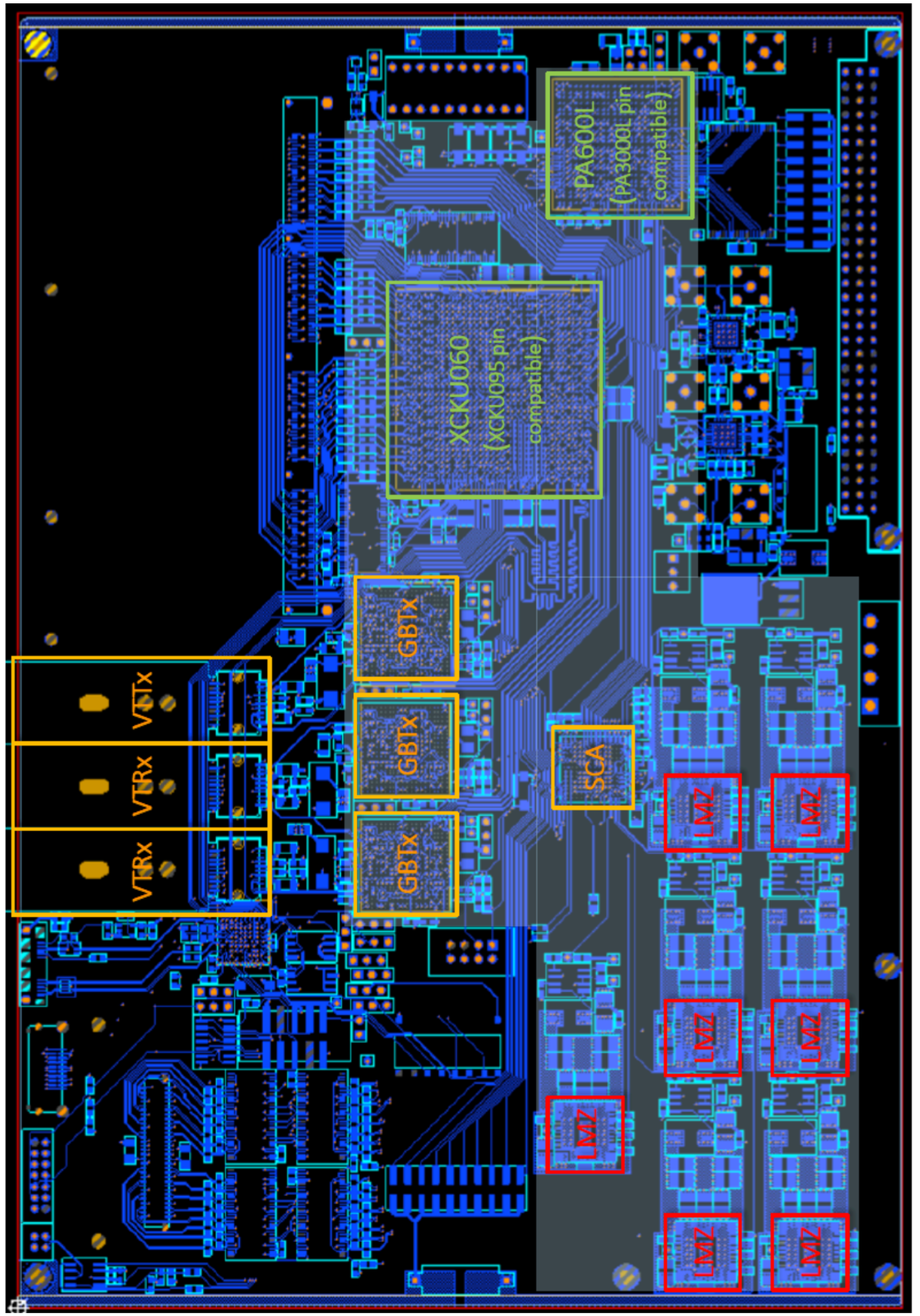
6U size board

Pre-production version under test

Readout Unit

Developed by ITS Upgrade team

- 3 GBTx chip, 1 GBT-SCA chip
- 1 VTRxSM (trigger)
- 1 VTRxMM (data/control)
- 1 VTTxMM (data)
- XCKU060 main FPGA (upgradable to XCKU095)
- PA600L scrubbing FPGA (upgradable to PA3000L)
- 7 LMZ31710RVQ DCDC (10A, rad and mag 1T tsd)
- J1 back connection for power supply (non VME)
- SEU hardening specific solution (triplicated FPGA IOs)



Marcus Johannes Rossewij

Summary

- ALPIDE chip under production
- Most of the R&D finalized — no showstopper found
- All Engineering Design Review successfully passed
- Ladder production will start fall 2017
- Disk production in 2018
- Ready for commissioning on surface fall 2019