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SI LAB Silizium Labor Bonn

ATLAS EXPERIMENT

Upgrade of ATLAS ITk Pixel Detector

26th International Workshop on Vertex Detectors

Las Caldas, Asturias, Spain

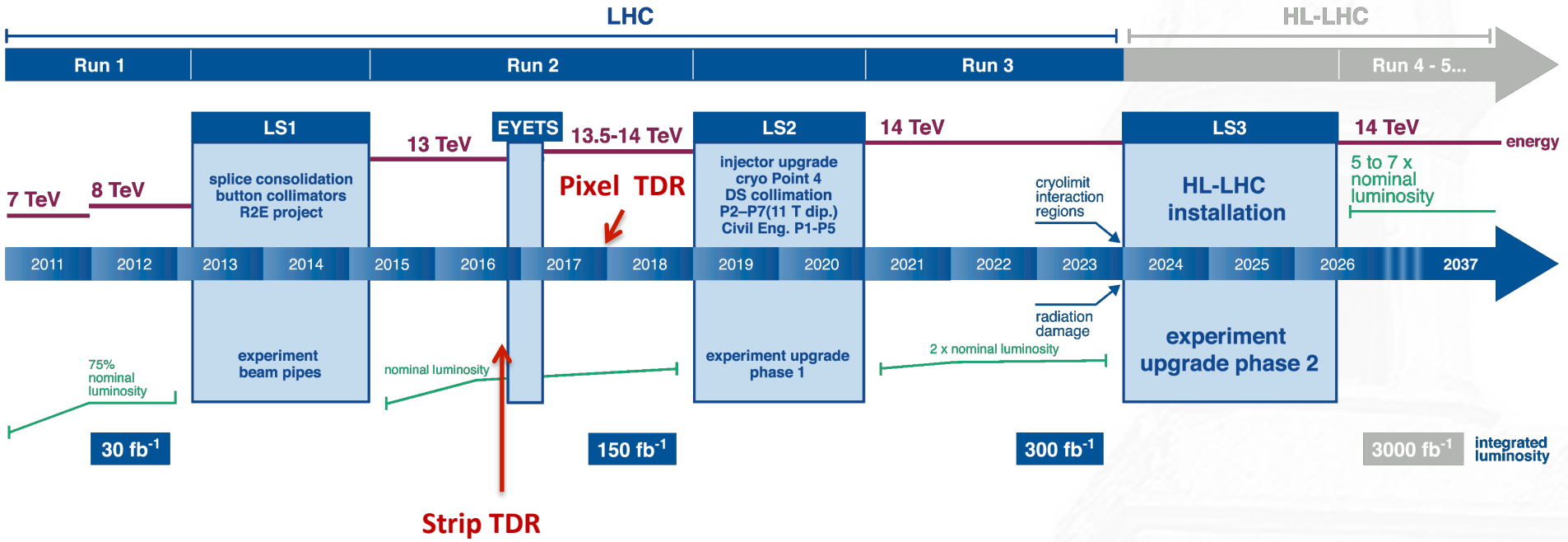
Fabian Hügging, University of Bonn

on behalf of the ATLAS Collaboration

Outline

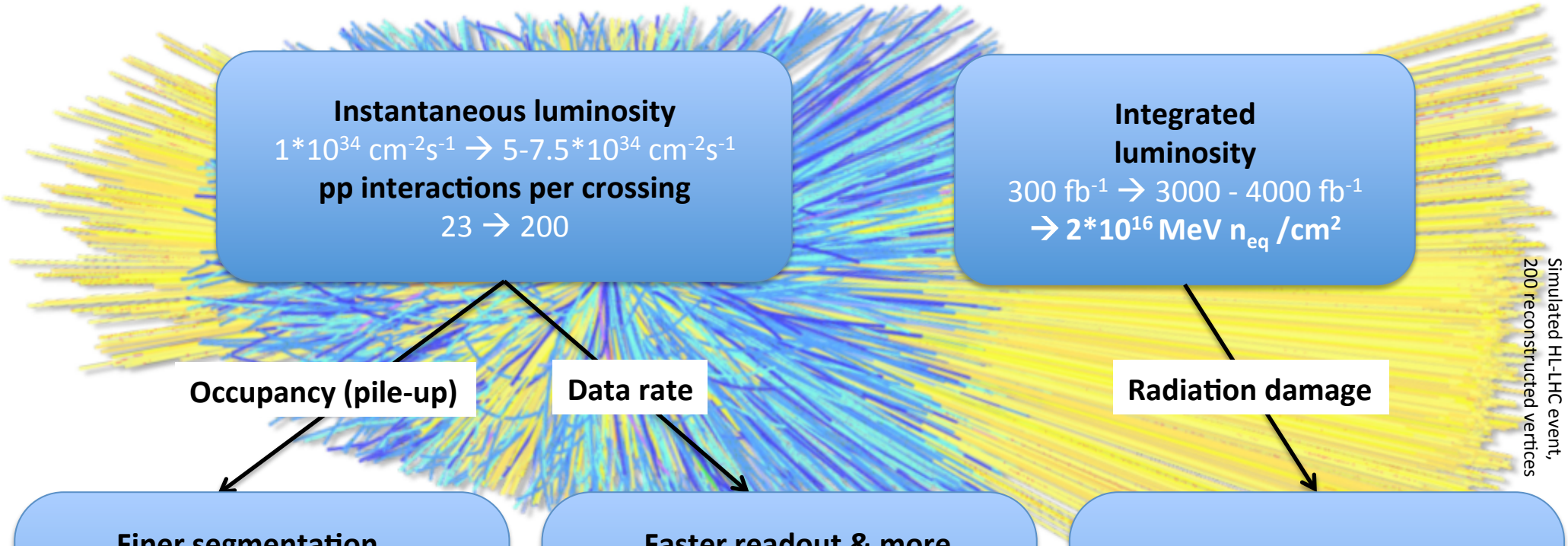
- Introduction
  - HL-LHC schedule
  - Requirements
  - Layout of the Phase 2 ATLAS Pixel Detector
- The ATLAS ITk Pixel Detector for HL-LHC
  - Mechanics: Support structures
  - Pixel Modules
  - Pixel Sensors: Planar, 3D and CMOS
  - FE-electronics: RD53
  - Bump bonding and assembly
  - System Design: Readout Concepts and powering scheme
  - System tests
- Conclusions

HL-LHC schedule



- The LHC will be upgraded to the High Luminosity-LHC (HL-LHC) to produce up to 4000 fb^{-1} of integrated luminosity until 2035
  - benefits precision measurements in many physics channels
  - allows studies of rare processes

Why a new Inner Tracker (ITk) for ATLAS?



Instantaneous luminosity
$1*10^{34}$ $cm^{-2}s^{-1}$ → 5-7.5*10^{34} $cm^{-2}s^{-1}$
pp interactions per crossing
23 → 200

Integrated luminosity
300 fb^{-1} → 3000 - 4000 fb^{-1}
→ **2*10^{16} MeV n_{eq} /cm^2**

Simulated HL-LHC event, 200 reconstructed vertices

Occupancy (pile-up)

Data rate

Radiation damage

Finer segmentation

- Smaller channels
- More channels
  → All silicon inner tracker with strips and pixels

Faster readout & more storage

- Upgraded readout (ASICs & Detector)
- Enhance data purity
  → Track trigger

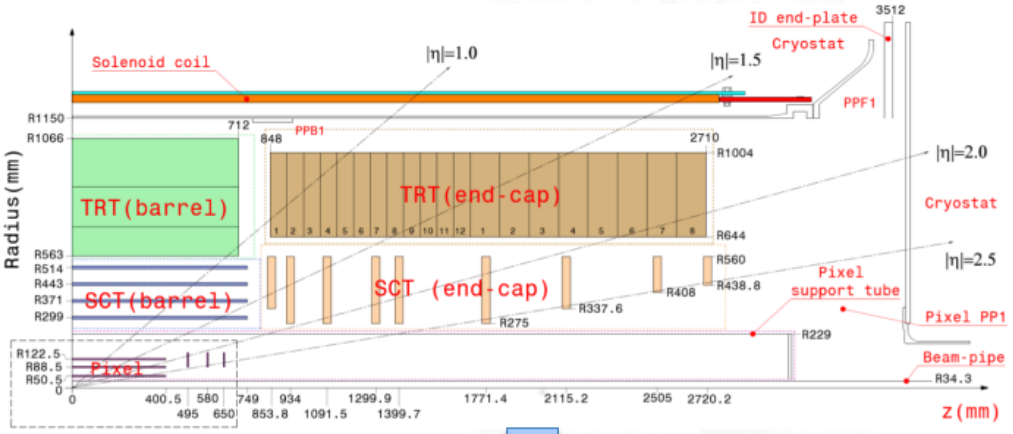
Increase radiation hardness

- New sensor & FE designs
- Exchangeable detector layers
- New CMOS technologies and designs

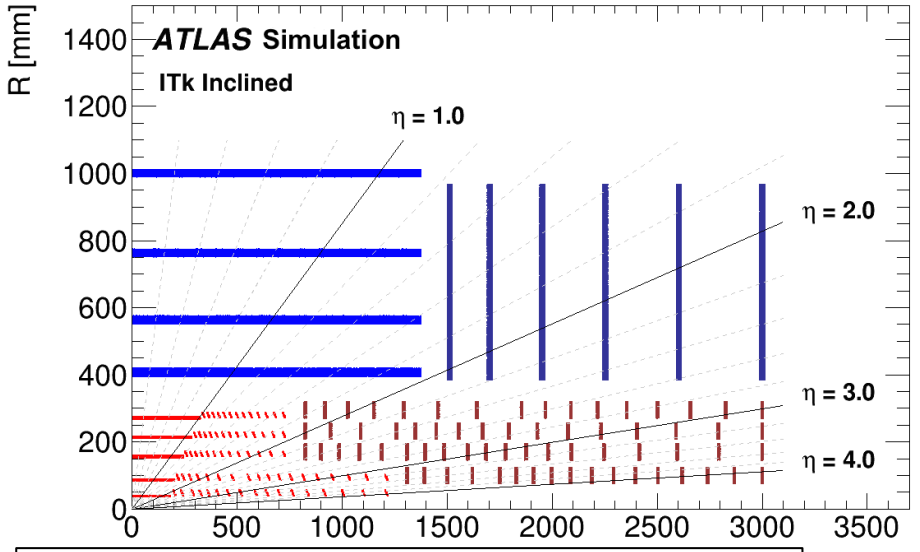
ITk Pixel Detector layout

Design goal:

- ITk should provide the same performance as the current detector, but in harsher environment of the HL-LHC

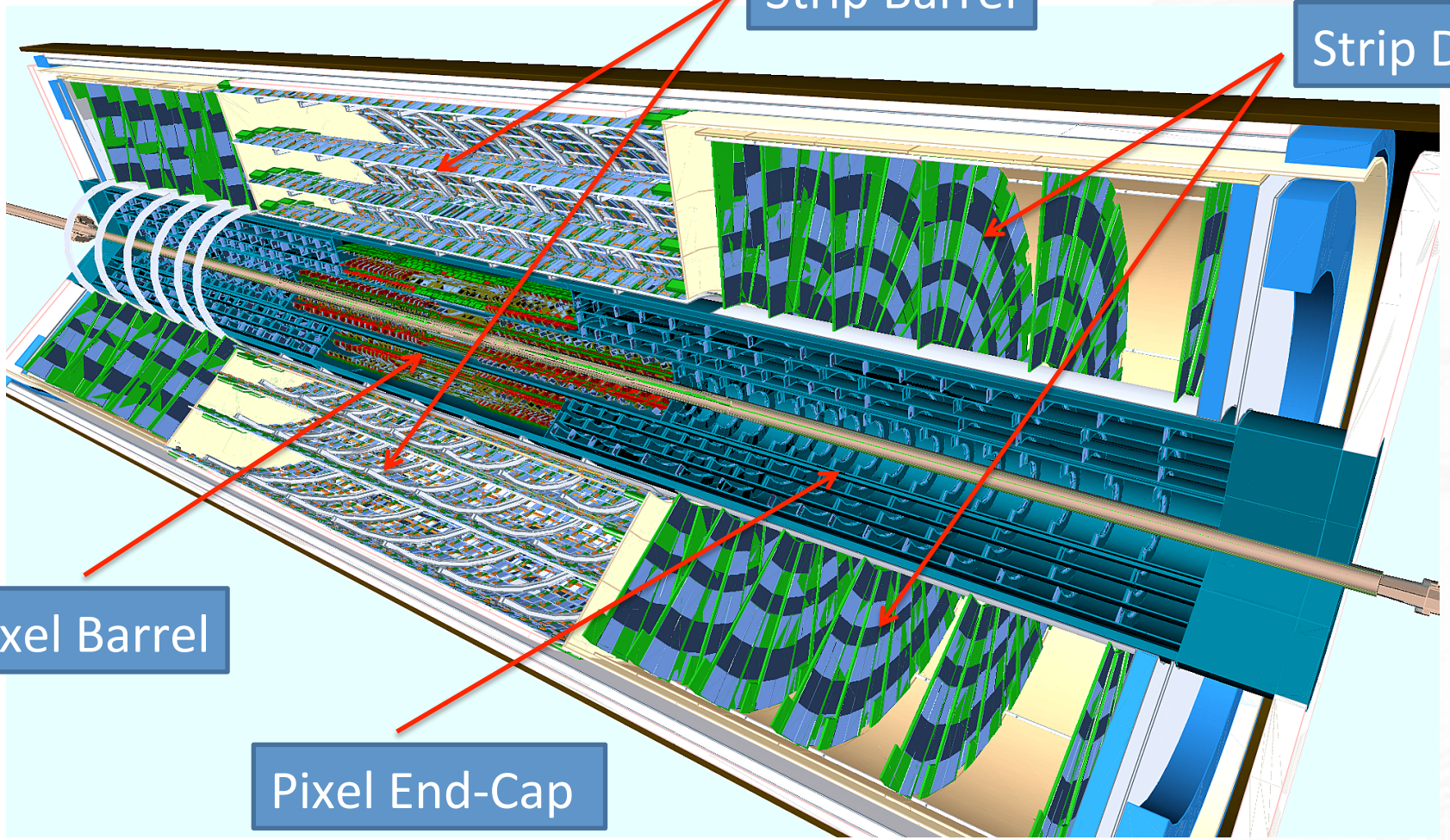


- All silicon design
- η coverage increased from 2.5 to 4
- 5 pixel barrel layers and 5 pixel rings
- 10,000 modules with 12 -14 m^2 of pixel detectors
- Design of the pixel part is being finalized: inclined layout optimization



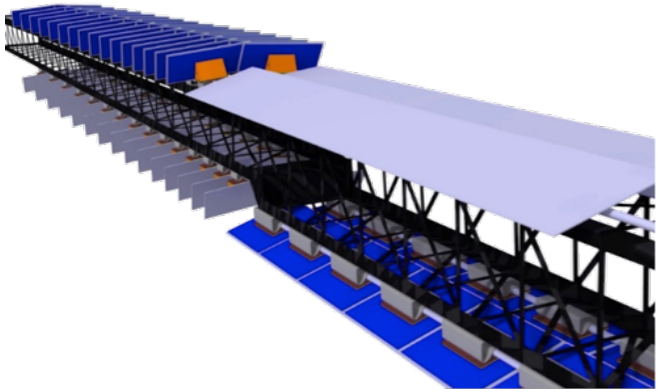
Technical Design Report for the ATLAS Inner Tracker Strip Detector
CERN-LHCC-2017-004. ATLAS-TDR-025, April 2017

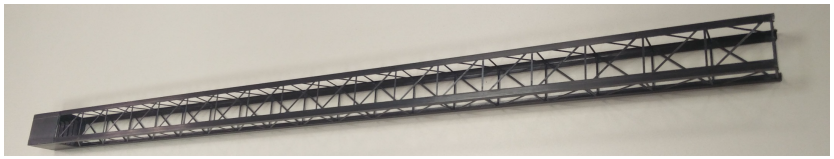
Pixel Mechanics

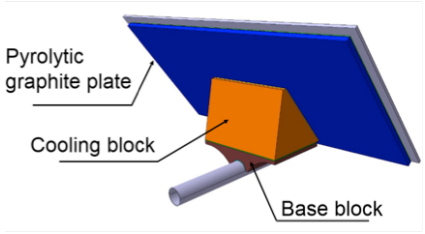


Pixel Mechanics

Pixel Barrel



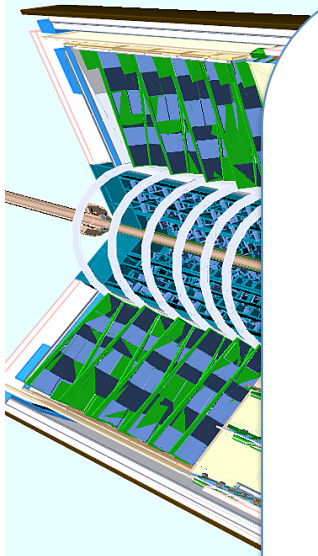


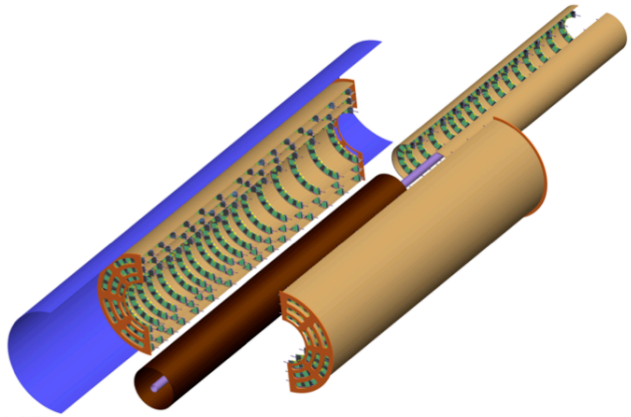


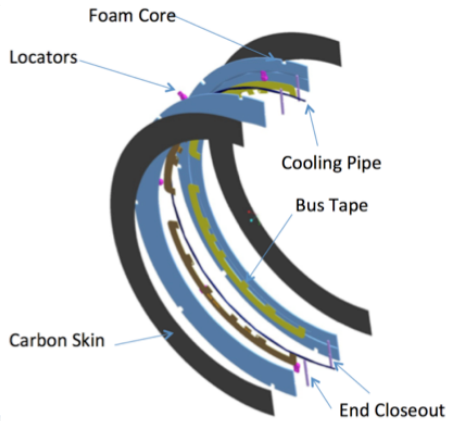
Truss prototype for Longeron design outer barrel layers
Flat section in the middle part of the Longeron
Inclined modules mounted on pyrolitic graphite plate (PGP)
connected to cooling pipe via cooling block
Inner layers could have slightly different design

Pixel Mechanics

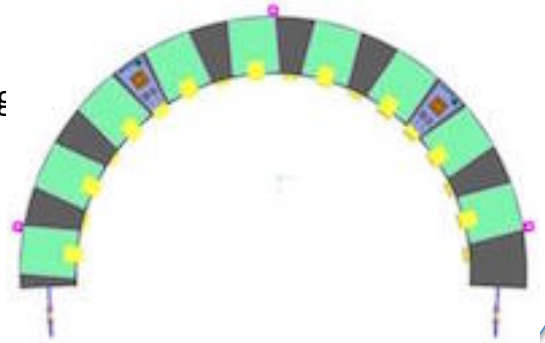
Pixel End-Cap





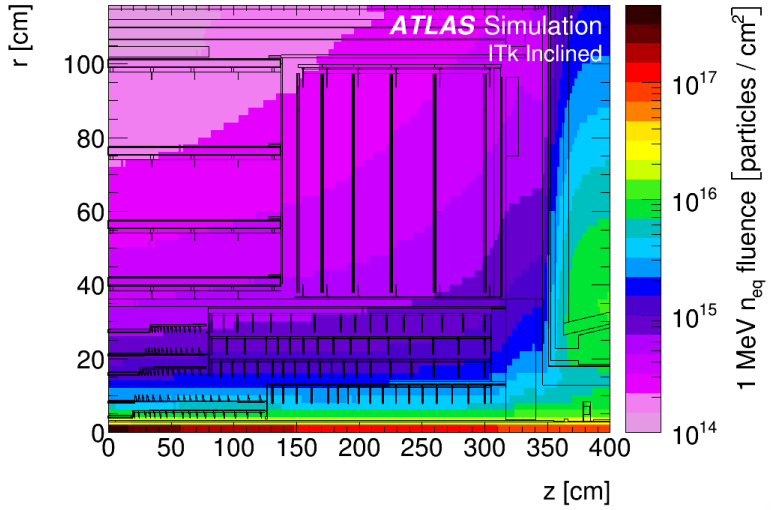


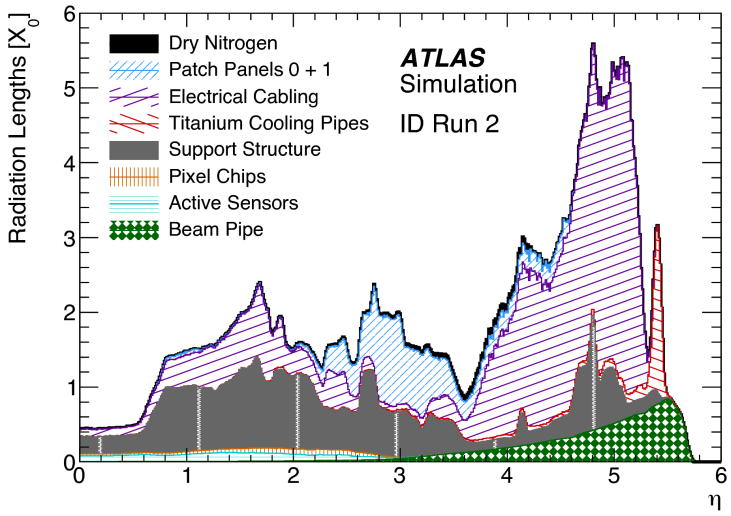
Half cylindrical shells supporting quad modules:
Designed to minimize mass of ring system reducing particle background reaching forward calorimeter and to improve tracking at high eta

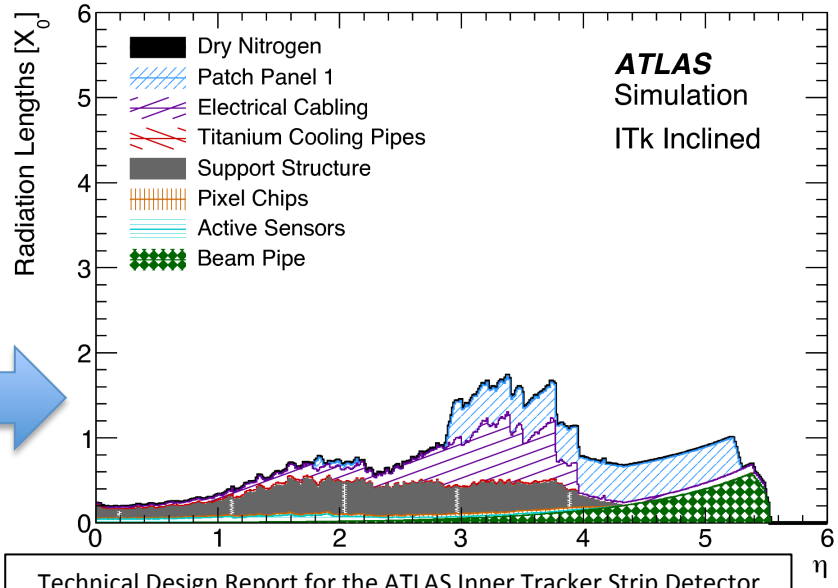


Material distribution

- Material reduction is crucial for good tracking and it helps reduces the fluence
- For the Phase 2 ITk the total material budget is around 30% lower as compared to the current Run 2 inner detector







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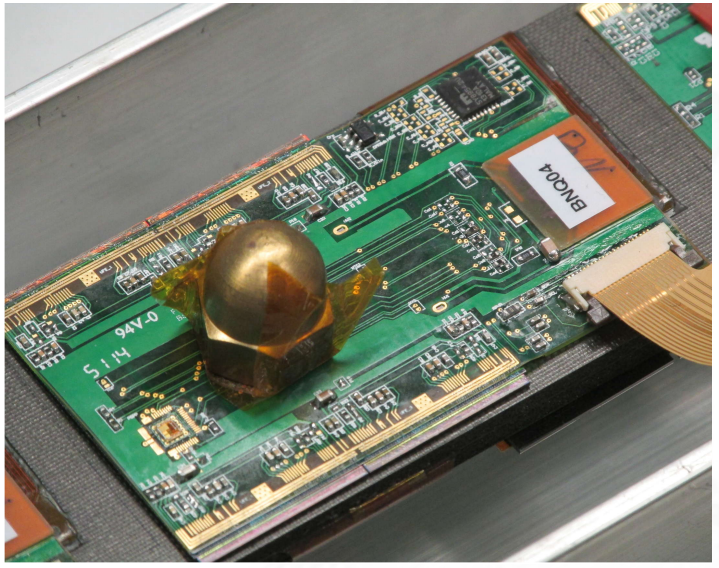
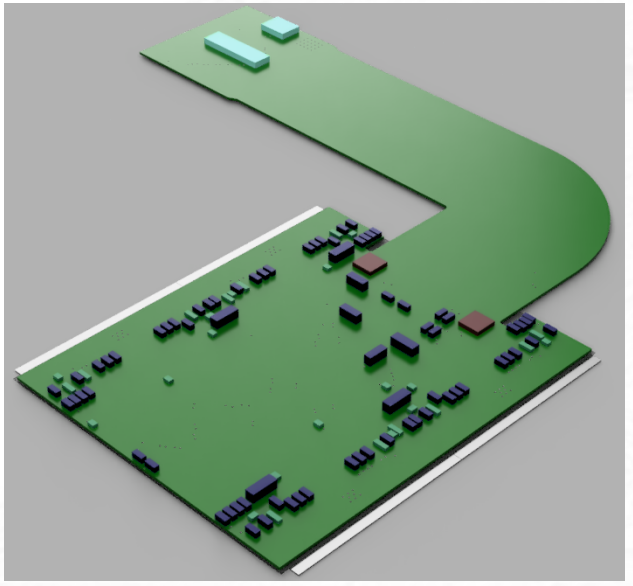
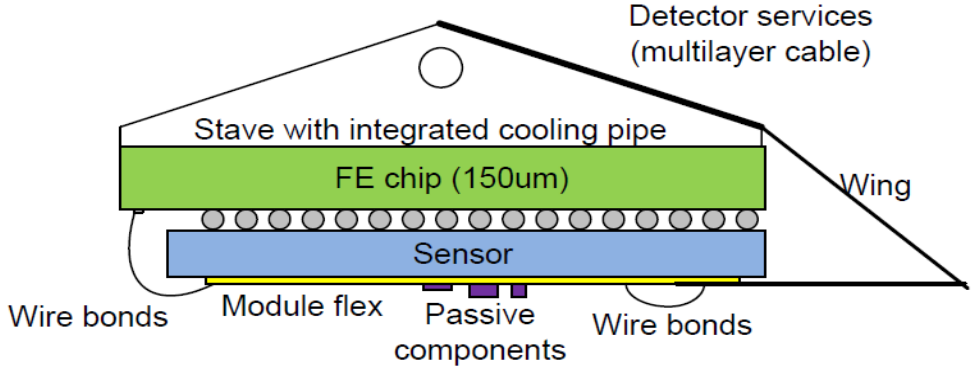
Pixel Module Assembly

- Basic building block is the pixel module:
  - bare module assembly consisting of sensor and FE-chip(s)
  - flex hybrid for interconnection of data power line to the local support services
  - Connection between FE, sensors and flex is done via wire-bonds
- For ITk about 10,000 modules are needed (quad-, double and single chip modules)

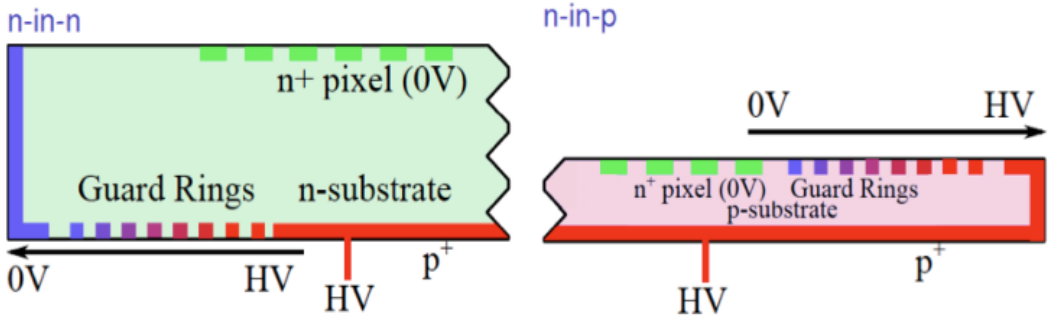


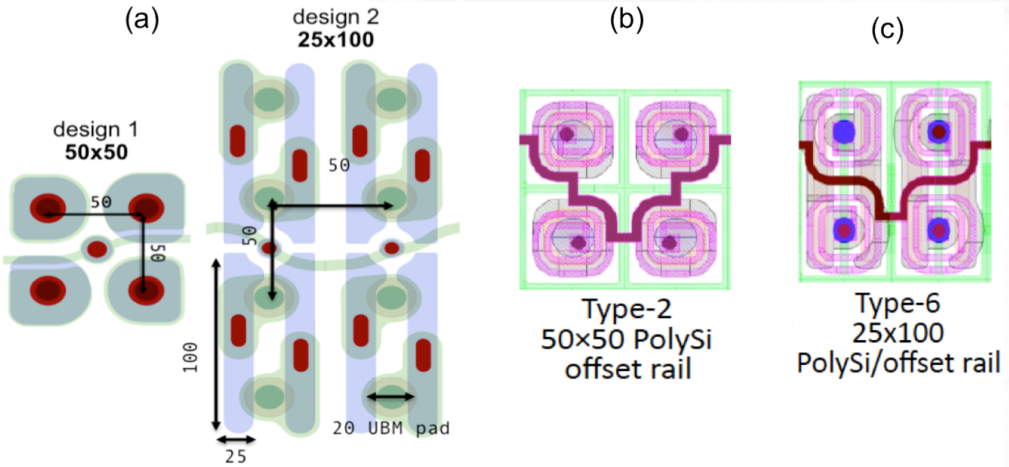




Planar pixel sensors

- Planar sensor technology
  - well understood and proven
  - n-in-p compared to current n-in-n → HV insulation on sensor or chip needed
  - for large areas: outer layers and quad assemblies → high yields and low costs
  - pixel size of 50x50 µm² or 25x100 µm² → mitigate effects of charge losses due to PT bias grid
  - thinner sensors with 100 – 150 µm → dealing with lower signals after high radiation fluences

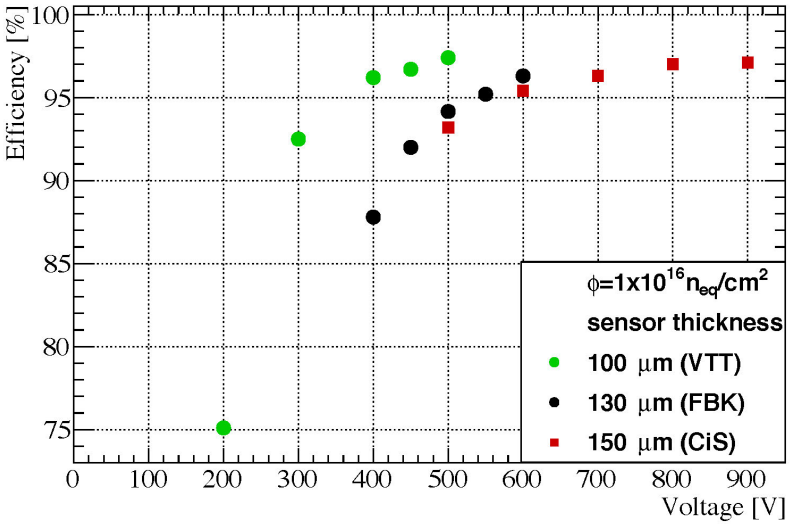


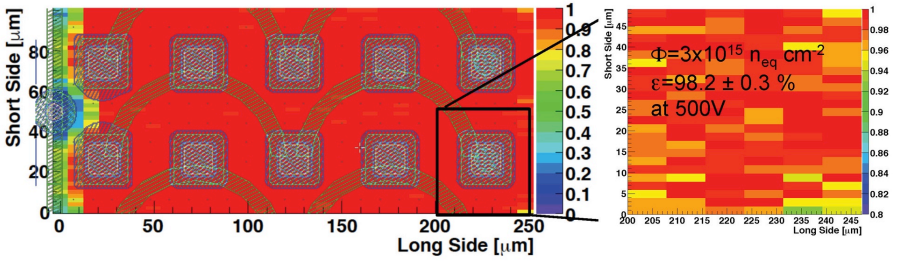


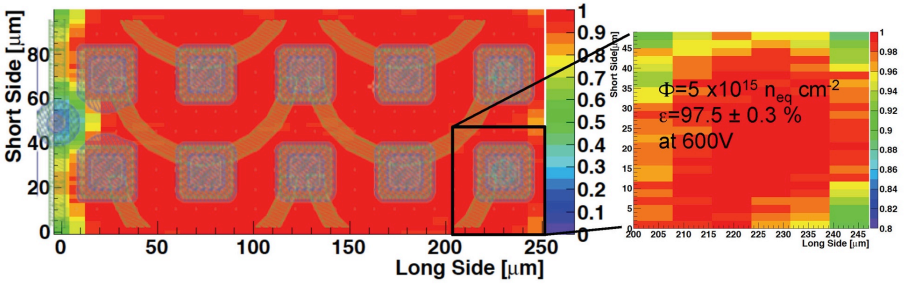
Planar pixel sensors

- Test of hit efficiency with FE-I4 compatible sensors of different vendors and thickness at 10^{16} MeV n_{eq}/cm^2:
  - 97% hit efficiency can be achieved
  - for thinner sensors this efficiency is reached at lower bias voltages between 400 - 500 V

- 50x50 μm^2 pixel cells has been tested with a modified sensor design w/o bias structures to extrapolate the performance expected with RD53

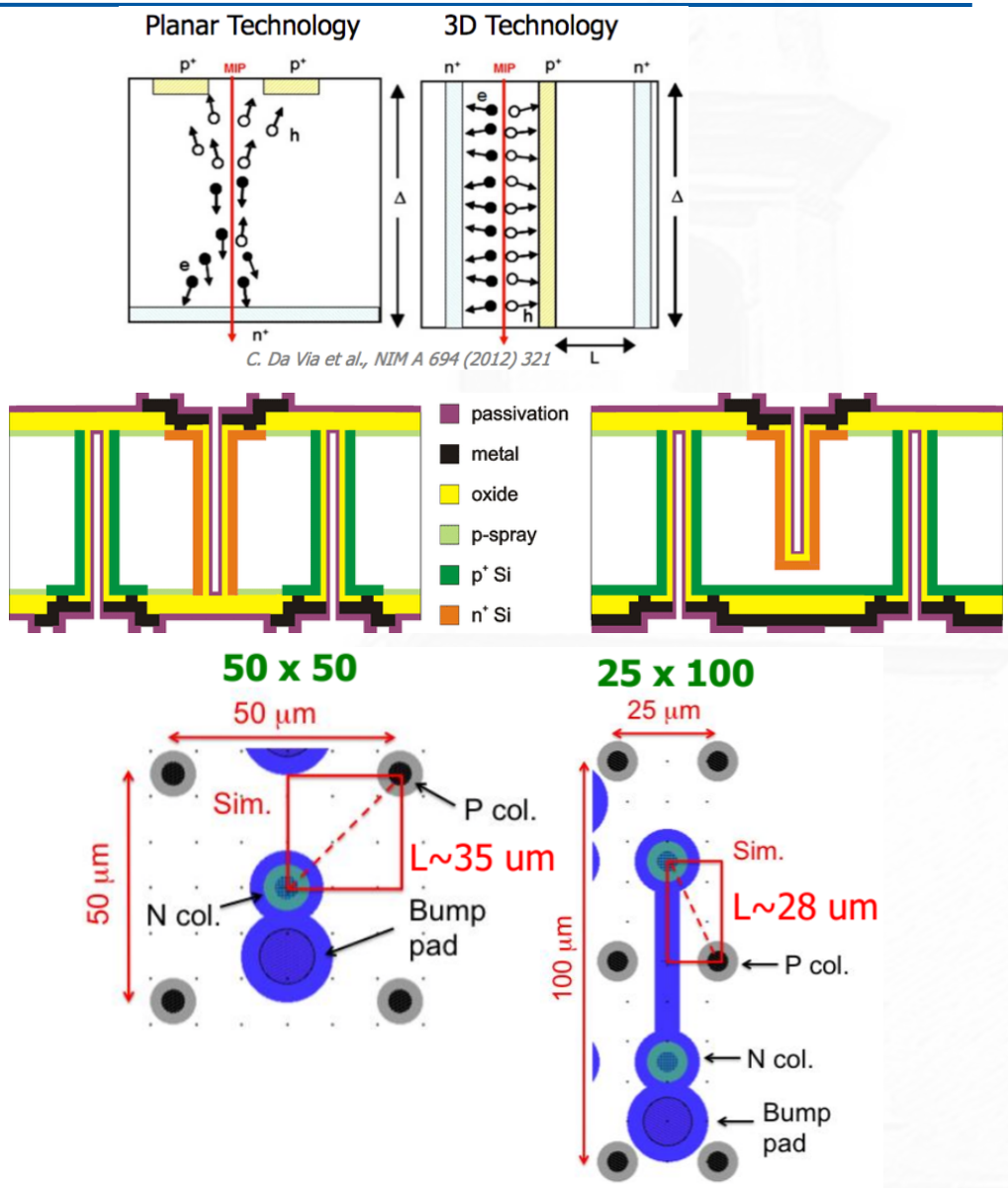




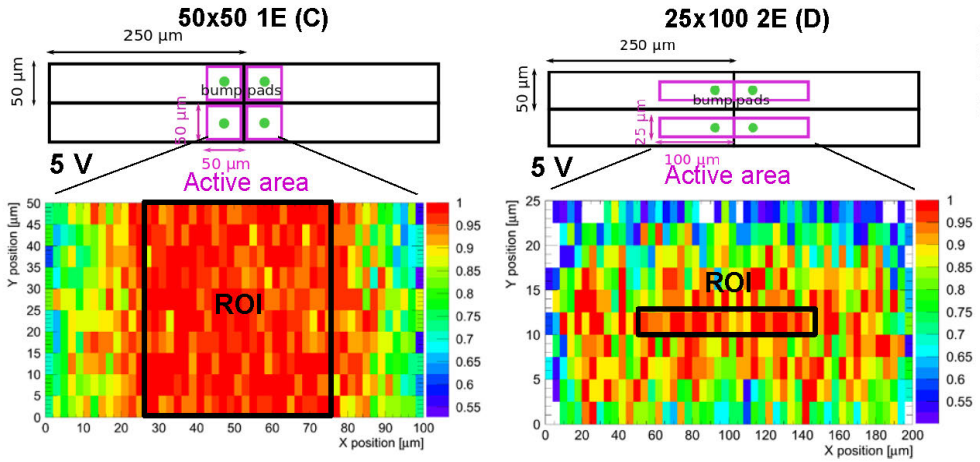


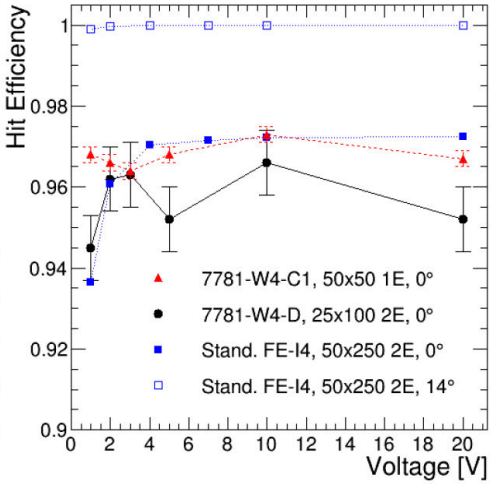
3D pixel sensors

- 3D sensor technology is the prime candidate for the inner layers due to the advantages in radiation tolerance
- 3D sensors are successfully used inside the ATLAS IBL
- Main challenges for the usage inside ATLAS ITk:
  - smaller pixel (50x50 or 25x100 μm^2) are more demanding with the column electrodes
  - yield improvements
  - thinner sensors to optimize signals and hits per track

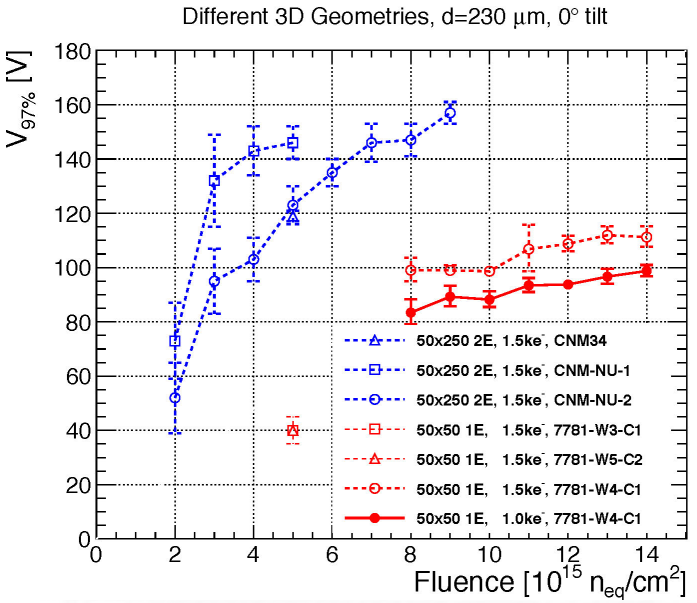


3D pixel sensors



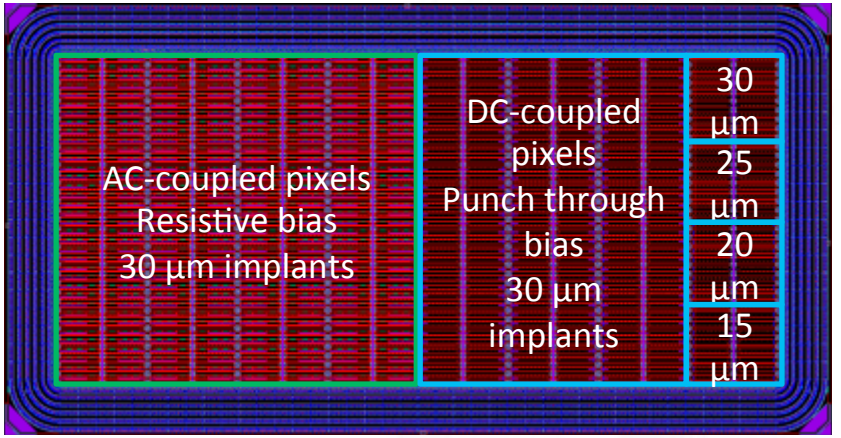


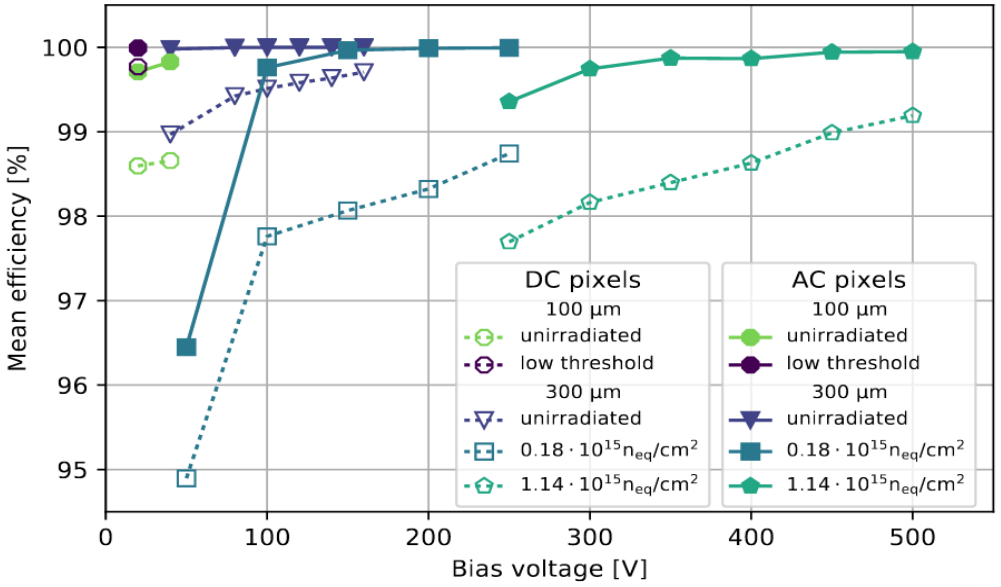
- Small pitch sensors are investigated with FE-I4 chip before and after irradiation:
  - hit efficiencies of 97% could be achieved at moderate bias up $1.4*10^{16}$ MeV n_{eq}/cm^2
  - good uniformities inside the pixel for both pixel sizes
  - $50x50\mu m^2$ pixel size is preferred



Passive CMOS sensor performance

- LFoundry 150 nm CMOS technology
- 2kΩcm p-type material, CZ 8’’
- Passive pixel, i.e collecting node w/o electronic
- 100/300µm thick, backside processed
- Bump bonded to ATLAS FE-I4
- Pixel size: 50 µm x 250 µm
- Matrix size: 16 x 36 (1.8 x 4 mm^2)





D. Pohl (Bonn)

113 of 114 measured sensors have identical parameters

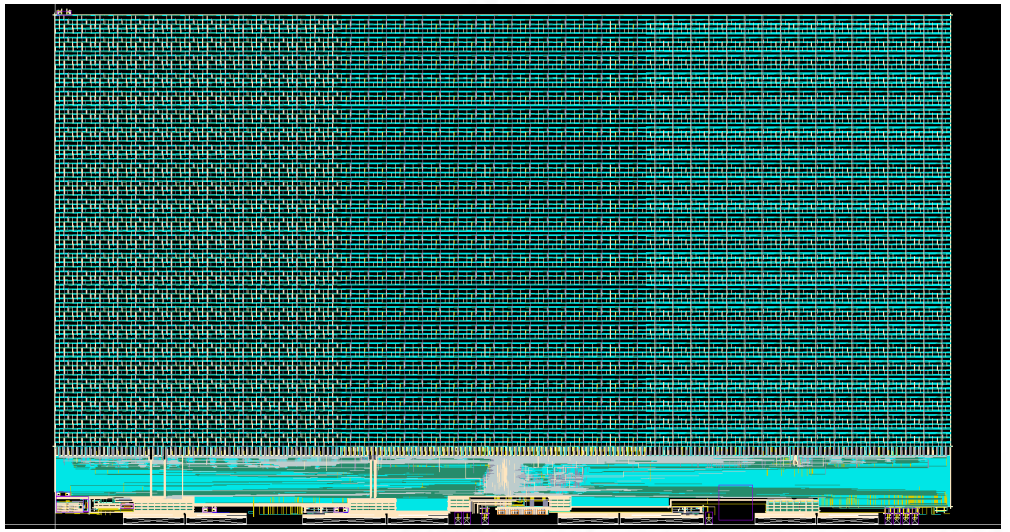
CMOS foundries can do good planar sensors (8”)

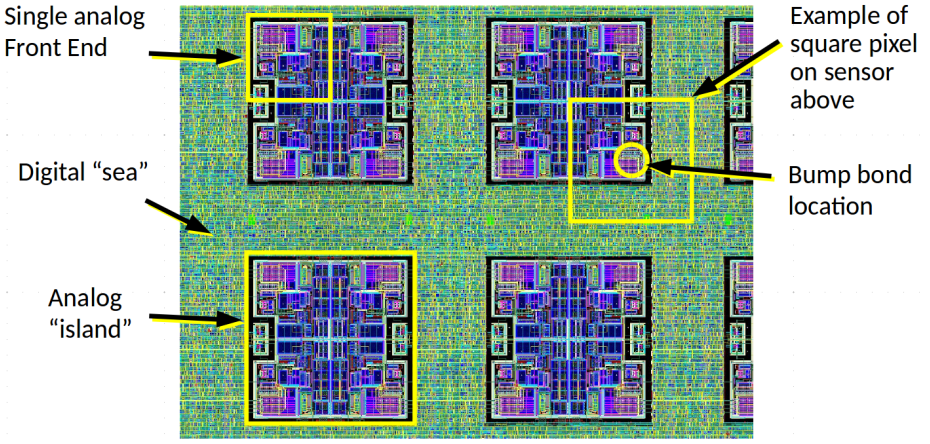
Development is ongoing as planar sensor option for the ATLAS ITk hybrid pixel detector

More about active CMOS sensors in T. Hemperek presentation on Tuesday and M. Benoit on Thursday

Pixel FE chip

- Format & power similar to FEI4
- “New” CMOS node and vendor
  - 65 nm with TSMC
- Joint development ATLAS & CMS
  - RD53 – share resources
  - Several prototypes fabricated and tested
- Radiation tolerance challenge
  - Damage mechanism empirically characterized
  - Can produce design spec for required 1 GRad target or at least 500 MRad
- Pixel layout
  - 50x50 µm^2 with 4-pixel analogue section
  - Surrounded by synthesized Digital sea
  - 50 µm minimum pitch to allow “standard” flip-chip
- Timescale
  - first large prototype (20 x 12 mm) RD53A chip in late 2017





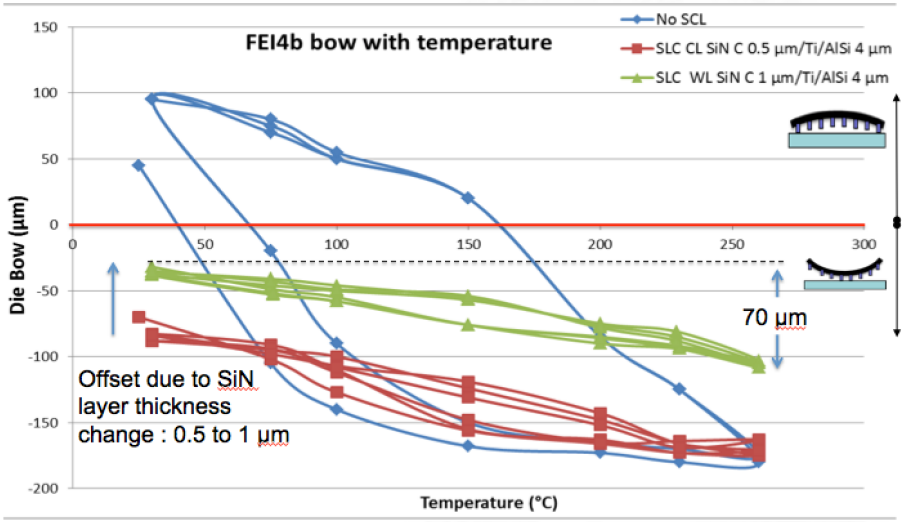
RD53A Specifications

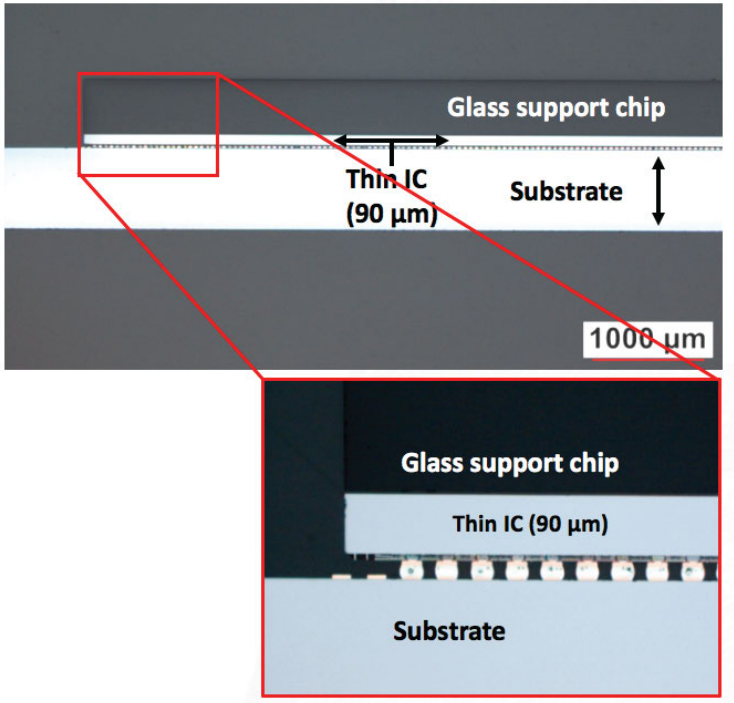
Technology	65nm CMOS
Pixel size	**50x50 um²**
Pixels	192x400 = 76800 (50% of production chip)
Detector capacitance	< 100fF (200fF for edge pixels)
Detector leakage	< 10nA (20nA for edge pixels)
Detection threshold	<600e-
In -time threshold	**<1200e-**
Noise hits	< 10^{-6}
Hit rate	**< 3GHz/cm²** (75 kHz avg. pixel hit rate)
Trigger rate	Max 1MHz
Digital buffer	12.5 us
Hit loss at max hit rate (in-pixel pile-up)	≤1%
Charge resolution	≥ 4 bits ToT (Time over Threshold)
Readout data rate	**1-4 links @ 1.28Gbits/s = max 5.12 Gbits/s**
Radiation tolerance	**500Mrad at -15°C**
SEU affecting whole chip	< 0.05 /hr/chip at 1.5GHz/cm² particle flux
Power consumption at max hit/trigger rate	**< 1W/cm² including SLDO losses**
Pixel analog/digital current	4uA/4uA
Temperature range	-40°C ÷ 40°C

More about RD53A read-out chip in R. Beccerle presentation on Wednesday morning

Pixel Modules: Bump Bonding

- Technology and requirements similar to ATLAS IBL, but
  - huge increase in volume → high production rate required
  - 12,000 modules in two years yield in peak flip-chip rate of 50 modules/day
  - Share the load: progress with several vendors (SnAg or In)
- Technical challenges:
  - assembly of thin devices:
    - sensor as thin as 100µm
    - FE chip 150µm or below → chip bow during reflow
  - Wafer sizes: 300mm FE, 150… 200mm sensors
  - bump denisty of 400 bump per cm^2 at 50µm pitch
  - smaller inter-chip spacing

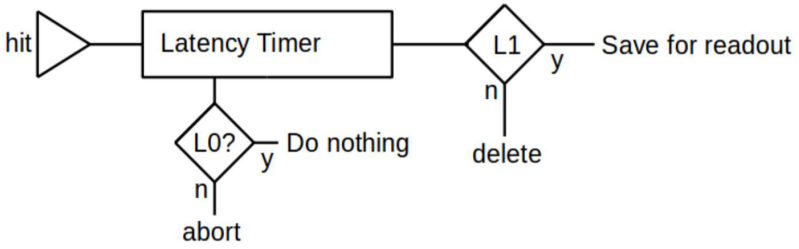


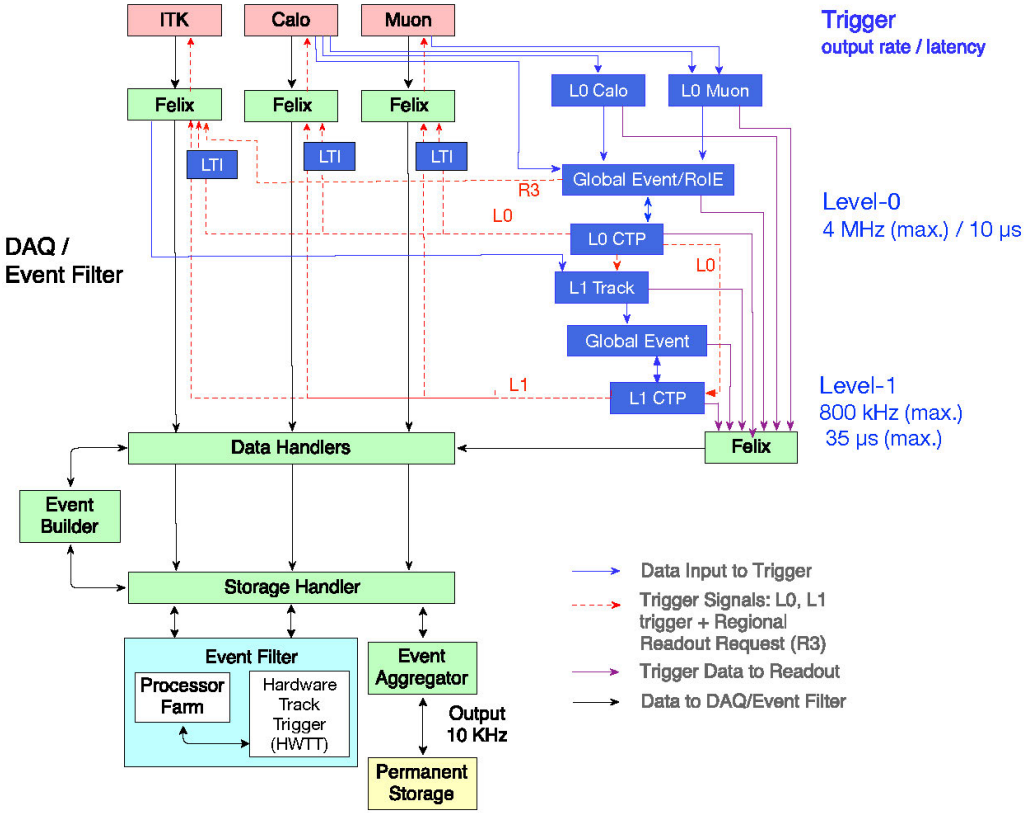


Readout Strategy: Trigger concept

- Complete ITk readout on L0 with 1 MHz rate and 10 µs latency or
- Partial ITk readout on L0 with 4 MHz/10 µs and full readout at L1 with 800 kHz/35 µs
  - outer pixel layers can provide full data on L0
  - inner layers can't due to bandwidth limitation of 5 Gb/s

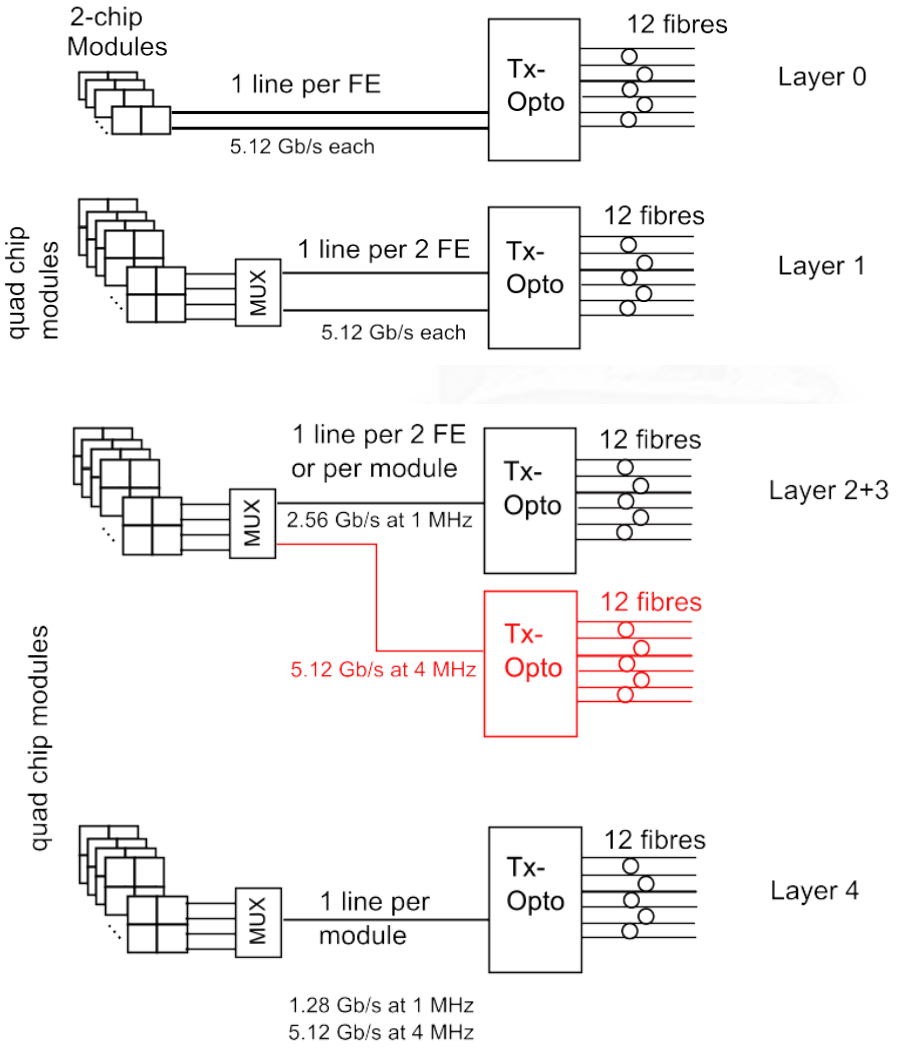
→ fast clear on L0, wait for L1



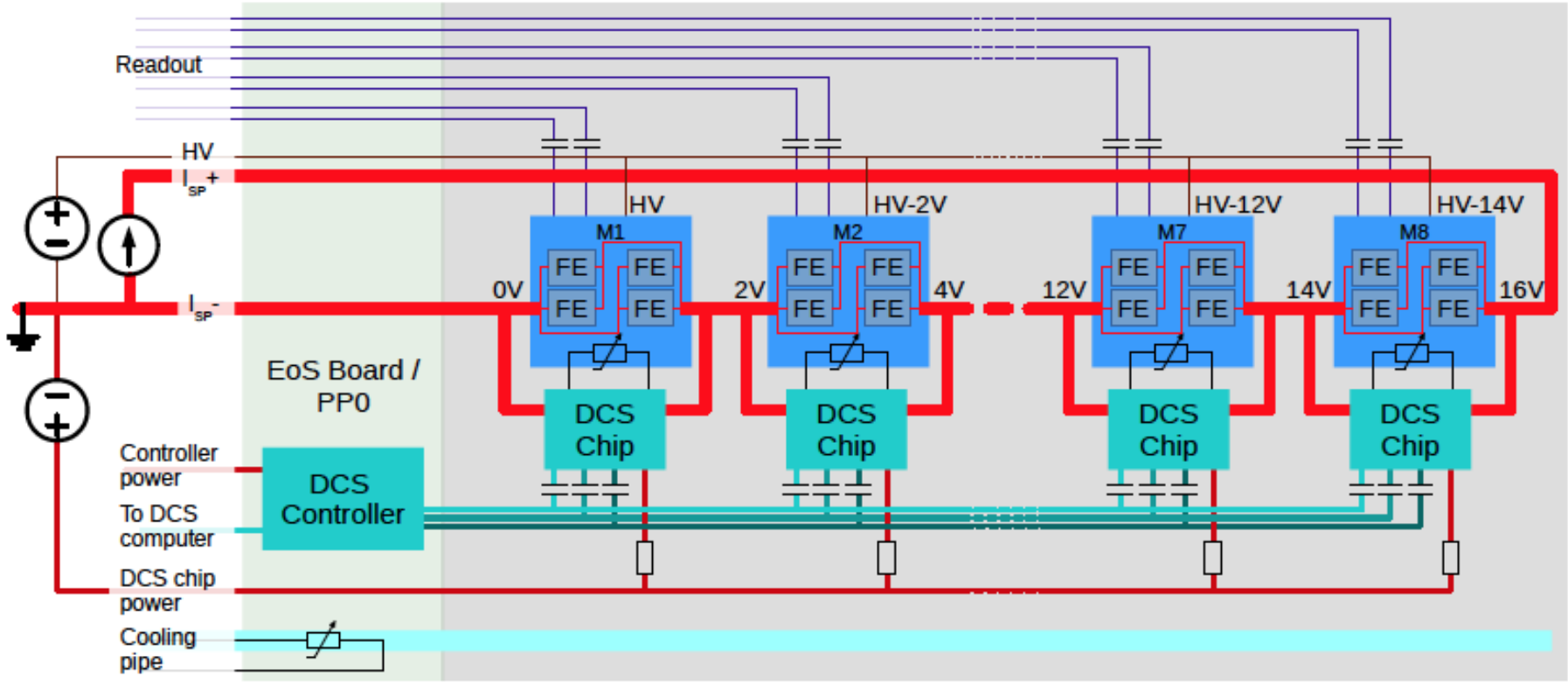


Readout strategy: Rates and bandwidths

- Rates and bandwidths vary:
  - inner layer: 1 cable per FE
  - outer layer: combines links to make use of bandwidth
- For Command/Clock (TTC):
  - use GBT
  - 160 Mb/s between GBT and FE for all chips per module



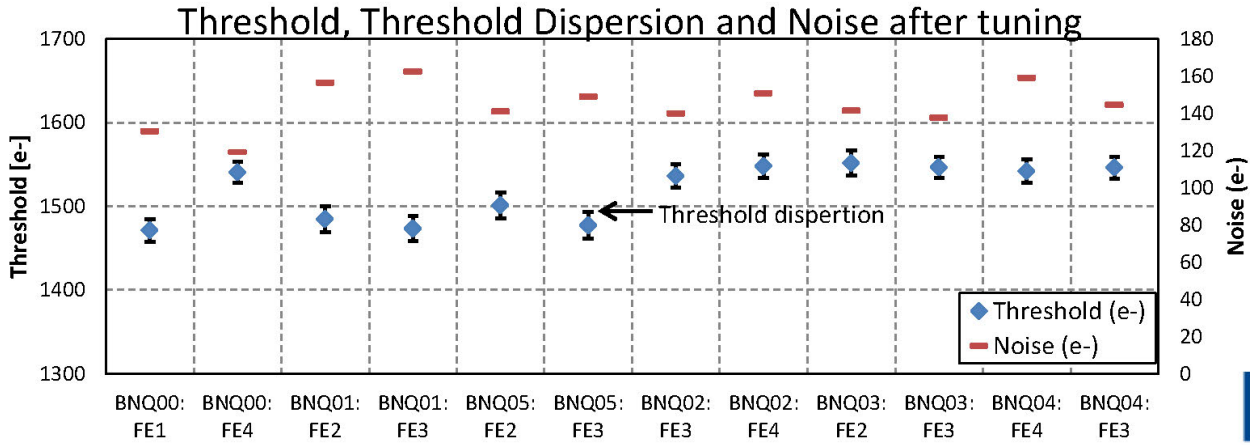
Pixel powering scheme

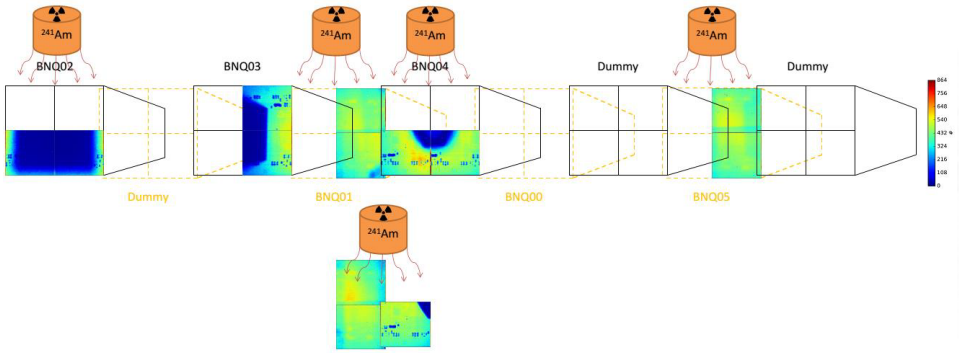


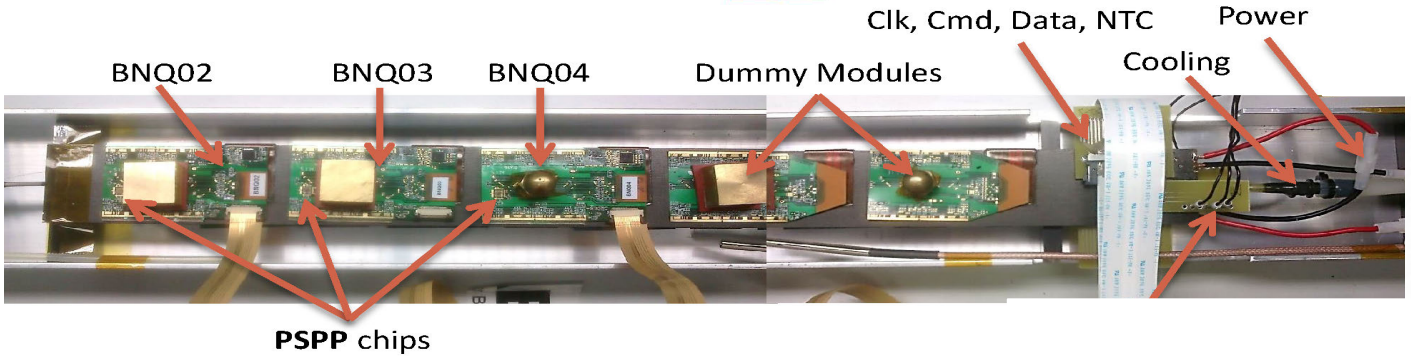
- Serial powering of pixel modules with up 12 (16) modules per chain
- DCS functionality integrated in concept
  - DCS chip: monitor and control of module (bypassing)
  - Independent power and communication lines for the DCS

Serial Powering Prototype

- Prototype with 6 FE-I4 quad modules mounted stave prototype
- 3 with on-flex DCS chip (PSPP)
- 6 modules tuned in parallel with no performance degradation w.r.t parallel powering
- Source scans with parallel readout of all modules



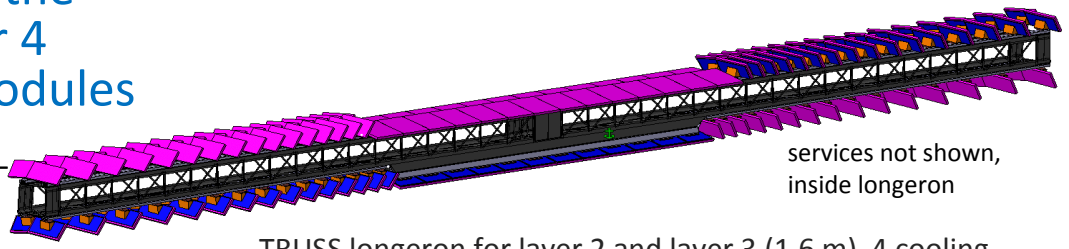




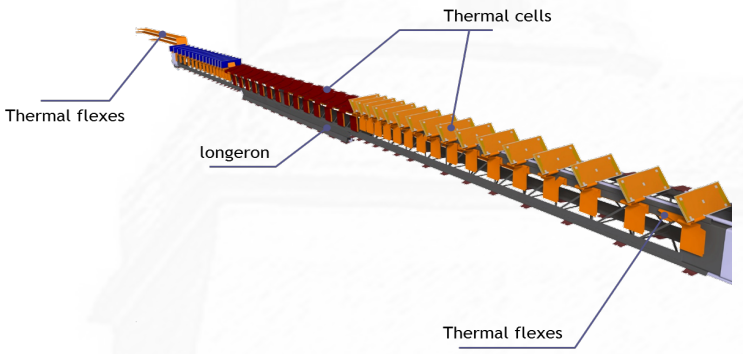
Prototyping outer barrel - Demonstrator programme

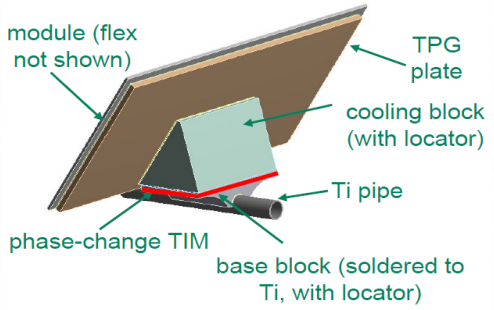
- Programme to evaluate and validate the SLIM concept: longeron coupling 3 or 4 cooling lines with flat and inclined modules
  - Prototypes for thermo-fluidic, thermal, thermo-mechanical, loading and full system tests
  - Deploy electrical (FE-i4) and heater modules, serially powered, services routed inside longeron
  - Exercise integration, development of tooling and share of many tasks and components between several institutes

  → Evaluation and validation of a full system
- Install and commission system setup including CO_2 cooling, DCS, interlock, powering
- Shared effort



TRUSS longeron for layer 2 and layer 3 (1.6 m) 4 cooling lines
52 flat quad and 124 inclined double modules



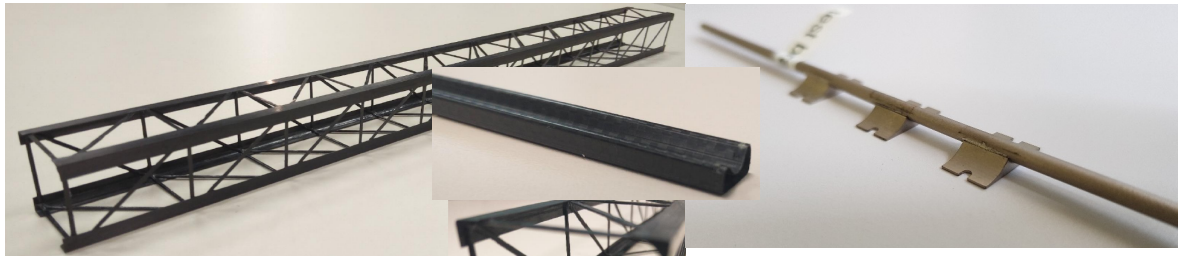


Inclined module on cell

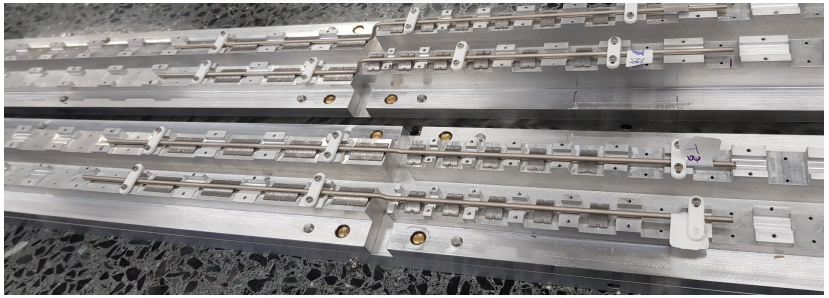
Demonstrator programme: status

- Components are getting ready:

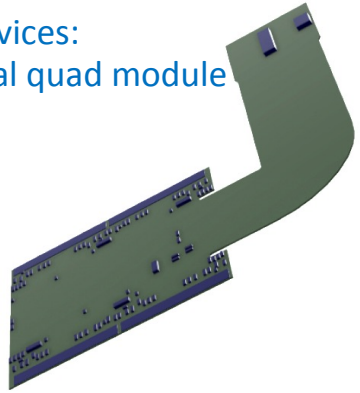
Functional longeron:
TRUSS and bend cooling pipes



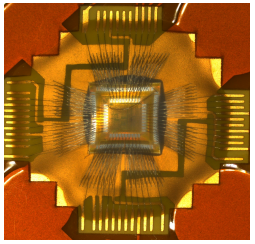
Assembly jig



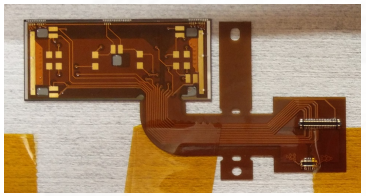
Flex services:
Electrical quad module flex



DCS serial powering
control chip on stave flex:



Heater dummy module



- Next: Assembly and integration, Pre-testing of partly integrated demonstrator components, commissioning of system setup
- Winter 17: Assembly and integration of demonstrator and evaluation

Conclusions

- ATLAS ITk Pixel project is making good progress in a lot areas:
  - Layout is being finalized and optimized
  - New read-out chip prototype RD53A is submitted
  - Sensor technologies are far advanced
  - Read-out with high data rates and electrical transmission
  - New serial powering scheme is established and tested with prototypes
  - Mechanics is getting more mature (thermal aspects, services integration, …)
  - More system aspects will be studied with system tests for barrels and rings
- ATLAS Itk Pixel is currently preparing the TDR
  - TDR submission will take place in December 2017