Contribution ID: **26** Type: **Invited Talk**

RD53A: a Large Scale prototype of a New generation Pixel Readout ASIC for the HL_LHC experiment

Wednesday 13 September 2017 09:30 (25 minutes)

The R&D program for a 65nm CMOS pixel chip of new generation for extremely high rate (3GHz/cm2) and very high radiation levels (1Grad) for ATLAS and CMS phase 2 pixel upgrades has taken place within the RD53 collaboration. Radiation test structures have been realized and characterized; building blocks and analog very front ends have been produced and tested. Small scale demonstrators with 64x64 array of 50x50 um2 pixels containing complex digital architectures have been produced and showed the feasibility of operating at very small noise and in-time thresholds.

Based on the past experience and achievements, the collaboration has designed in the last year a large scale prototype (20mm x 12 mm) called RD53A, that will be submitted for production during summer 2017. It contains a large number of different building blocks (analog front-ends, calibration circuit, Bandgap, DACs, ADC, PLL, serializer, cable driver, serial IO, serial power Shunt-LDO regulator, on-chip monitoring of temperature/radiation/current/voltages, etc.) that have been prototyped and extensively tested, including irradiation, before being finalized and integrated on the RD53A demonstrator.

The main concepts of RD53A are described, explaining how it defines the baseline for the development of the pixel chips for the ATLAS and CMS experiments for HL_LHC

Author: BECCHERLE, Roberto (INFN, Pisa (IT))

Presenter: BECCHERLE, Roberto (INFN, Pisa (IT))

Session Classification: Electronics and System Integration