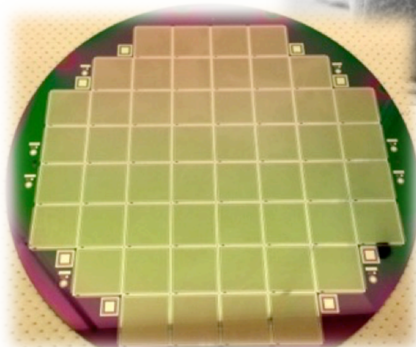
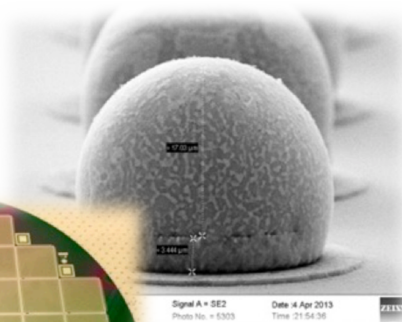
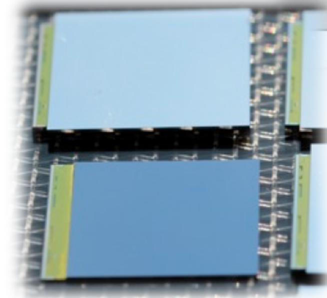
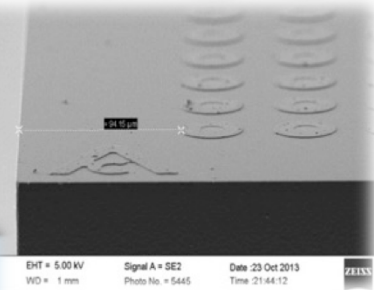
VERTEX/2017

Solutions for flip chip bonding of future pixel detectors



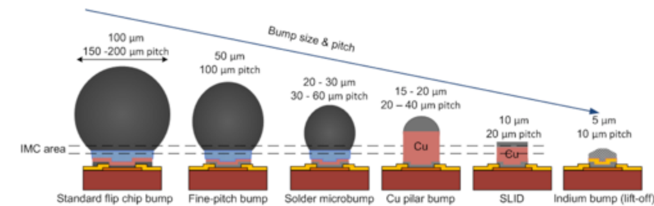


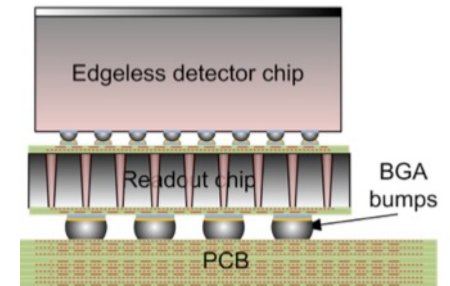


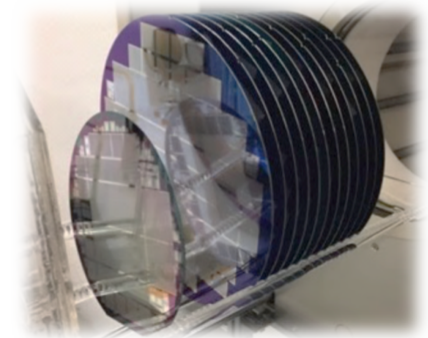


Outline

- Introduction to Advacam
- Ideal pixel detector interconnect structure
- New challenges in the flip chip process
  - 65nm CMOS technology – 300mm wafers
  - Finer pitches requested – going towards 20 um
  - Larger CMOS chips
- Suggested solder bump structures (Cu pillars)
- Flip chip bonding of thin chips
- Modules with Through Silicon Vias (TSV)
- Cost issues & potential solutions
- Summary

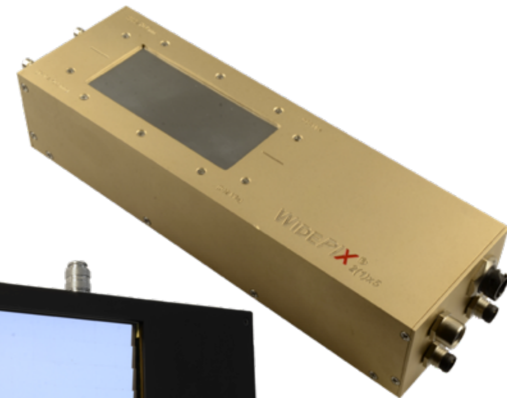


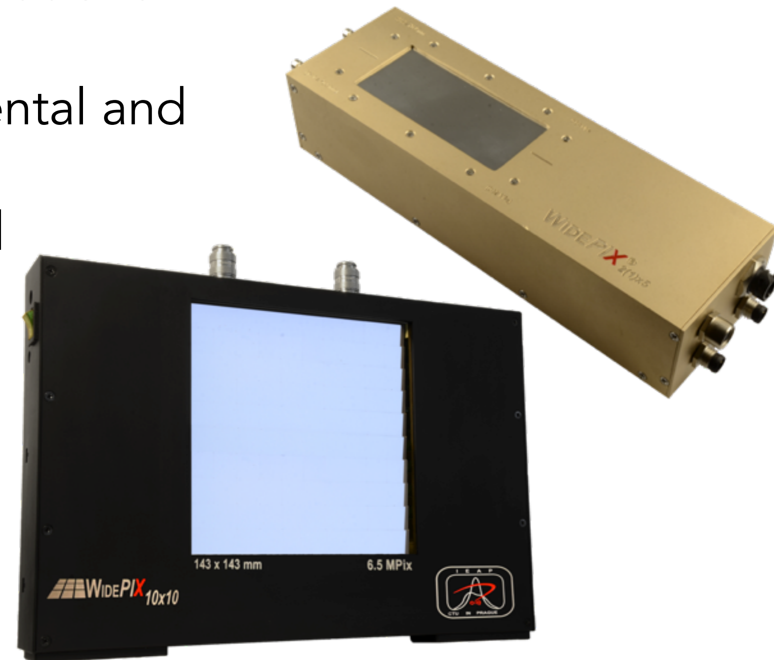




Introduction to Advacam

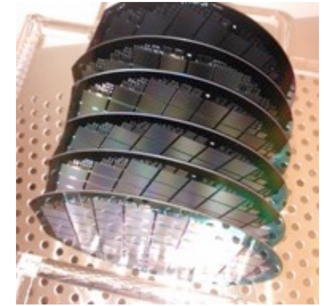
- ADVACAM consists of two units:
  - **Advacam Semiconductors**, Espoo, Finland
    - Sensors & hybrid pixel modules (since 2012)
    - One stop shop for your pixel assemblies
    - Spin-off from VTT Technical Research Centre of Finland
  - **Advacam Cameras**, Prague, Czech Republic
    - Photon counting cameras and solutions (since 2013)
    - Spin-off from Institute of Experimental and Applied Physics, Prague
  - Advacam employs 28 people in total
  - www.advacam.com

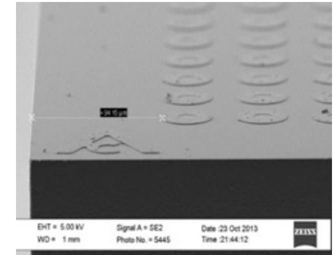


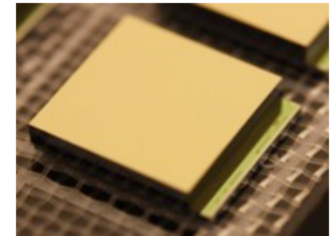


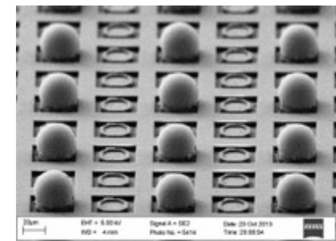
Service Concept of Advacam Semiconductors

- Commercialization of long term research done by VTT
  - Office in Micronova building www.micronova.fi
    - Access to all process tools in VTT's clean room
- Advacam is the "garage" of very challenging fabrication services within radiation pixel detectors
- Unique radiation pixel detector fabrication + flip chip service
  - Planar & edgeless Si sensors
  - Flip chip bonding of compound semiconductor sensors
  - Full value chain covered within the same company
- Services from prototyping to production
- Looking for regular production work with emphasis in gathering more statistics of the process steps, for maintaining quality and investing in new equipment



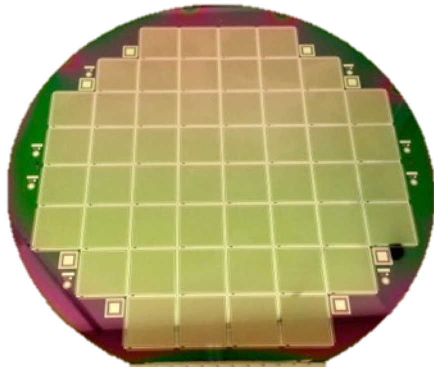


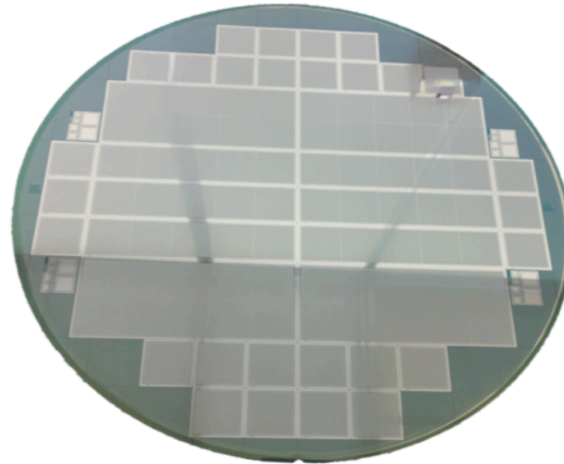


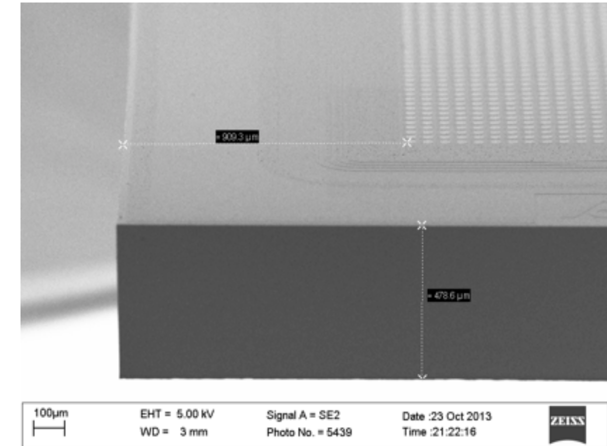


Si Sensor Processing

- Advacam has experience in manufacturing customized “planar” pixel sensor on 6” (8” R&D) wafers ranging from thickness of 100 um to 1 mm.

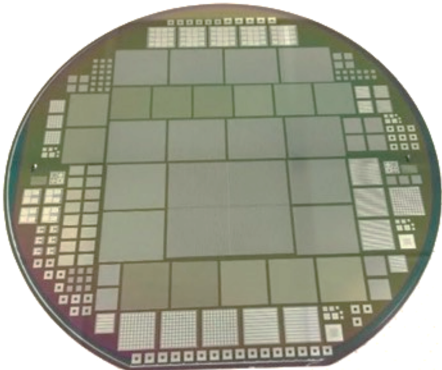


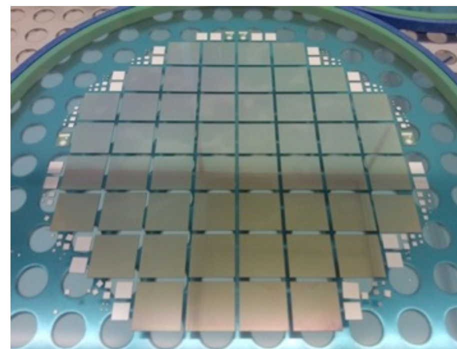


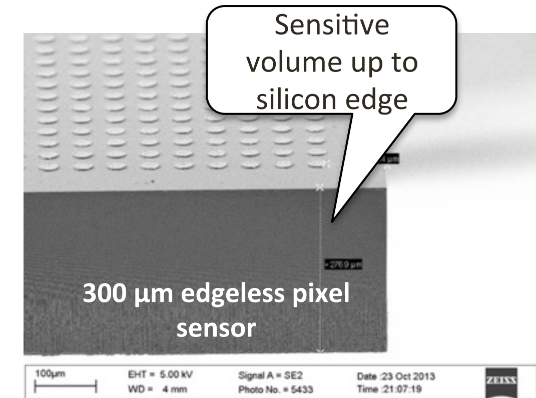


8” (200 mm) wafer

- Advacam has experience in manufacturing “edgeless” and ultra thin sensor 6” wafers ranging from thickness of 5 um to 675 um

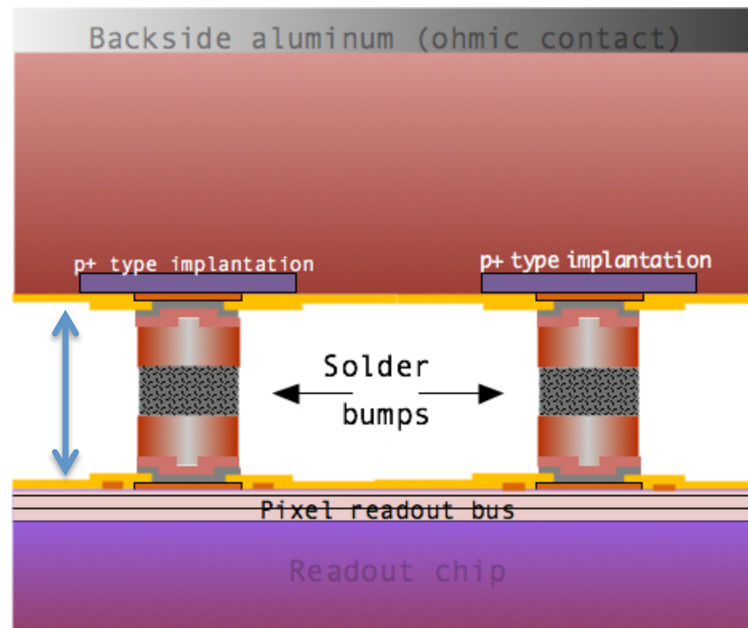






Ideal Pixel Detector Interconnect Structure

- Favorable characteristics:
  - High stand-off height
    - Less sparking
    - Reduced capacitive coupling between sensor and ASIC
    - Improved mechanical reliability



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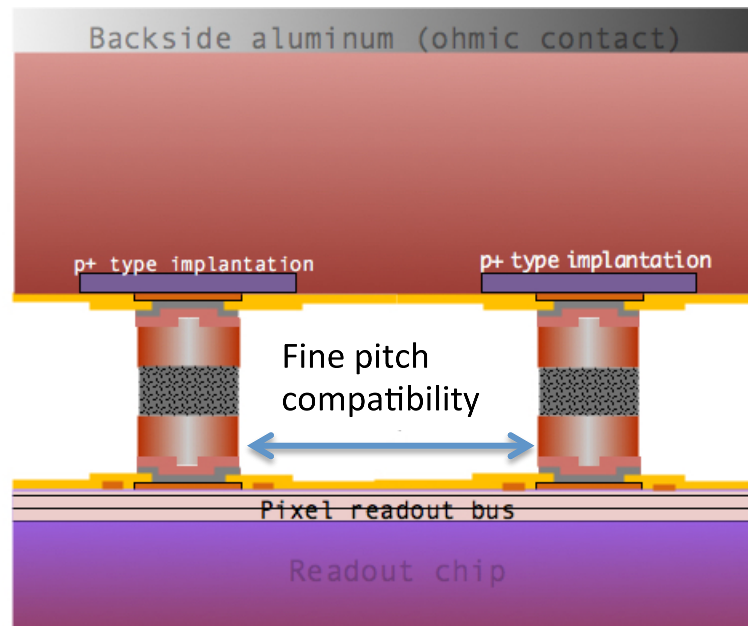
    - Smaller pixel size



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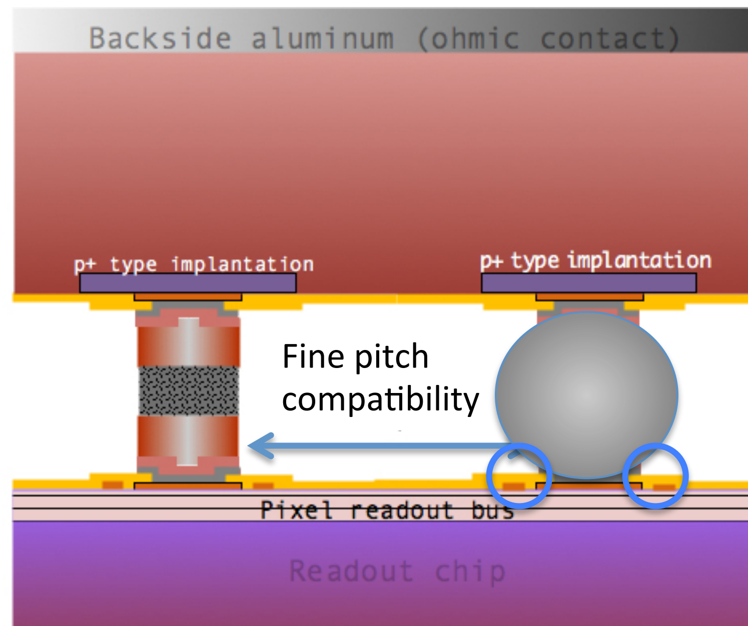
  - Small bump footprint
    - Minimize capacitive coupling to digital circuitry



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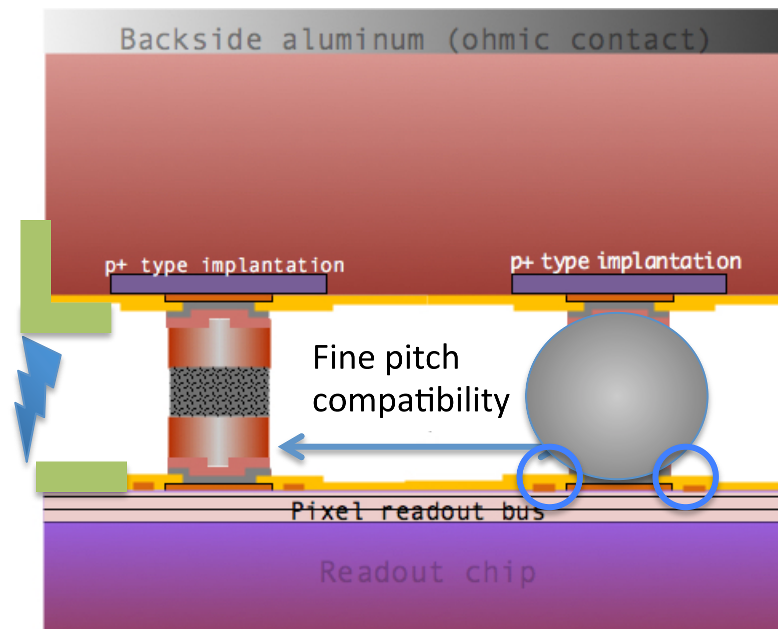
  - Polymer dielectric
    - Coatings to prevent sparking at periphery



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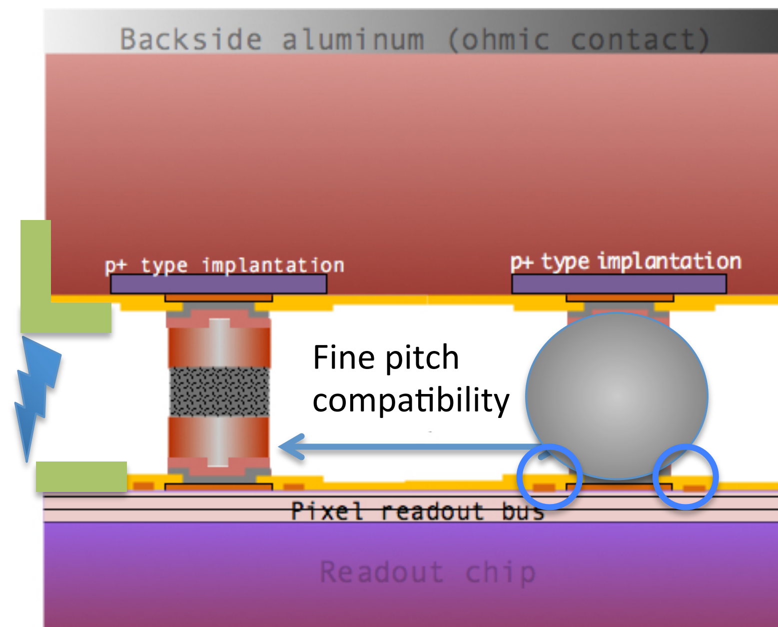
  - Ultra-fine pitch interconnects
    - Smaller pixel size
  - Small bump footprint
    - Minimize capacitive coupling to digital circuitry
  - Polymer dielectric
    - Coatings to prevent sparking at periphery
  - Thin sensor/ ASIC (high-energy physics)
  - Thick sensor (Si, GaAs, Cd(Zn)Te…) for X-ray imaging
  - Compact size
    - 4-side buttability TSV's and edgeless Si sensors



Trends and Challenges in the Flip Chip Process

- Currently, the pixel CMOS ASICs are mainly fabricated on 200 mm and Si pixel sensor chips on 150 mm Si wafers
  - Many vendors for bumping and flip chip bonding
- High-Energy Physics (HEP) community is going for 65 nm CMOS technology (RD53 ATLAS & CMS)
  - Increase or wafer size from 200 mm to 300 mm (RD53, CLICPIX & Timepix4)
  - There are only few research organizations who are able do the wafer bumping, thinning and dicing in-house
- Ultra-fine pixel pitches desired
  - Pixel electronics are getting smarter – generic benefit of having smaller pixels
  - Tracking – CLICPIX & Mönch 25 um pitch
  - Industrial application examples: Dental (intra-oral) X-ray imaging 25 um pitch, non-destructive testing, mammography etc.
- Larger chips are desired
  - Flip chip bonding is expensive in small series – larger area covered by single module
  - Larger full field of view
- Ultra-thin modules needed for HEP experiments
  - Issues with flip chip bonding – bow of the CMOS ASICS
  - Low-temperature bonding processes favorable
- Handling of Through Silicon Vias (TSV) wafers and chips
- Technological challenges will raise to next level, but the fabrication of the modules should be cheaper than ever?!!!

Solder Bump Structure

- Bumping techniques available:
  - Electroplating = EP, Solder ball placement = SBB, Evaporation = EV, Stencil Printing = SP, ENIG = Electroless Ni/Au.
    - Pay attention to the solder volume with reducing pitch

Standard FC bump

- EP
- ENIG + SP
- ENIG + SBB

FC fine-pitch bump

- EP
- ENIG + SBB
- C4NP

FC µ-bump

- EP

Cu pillar bump

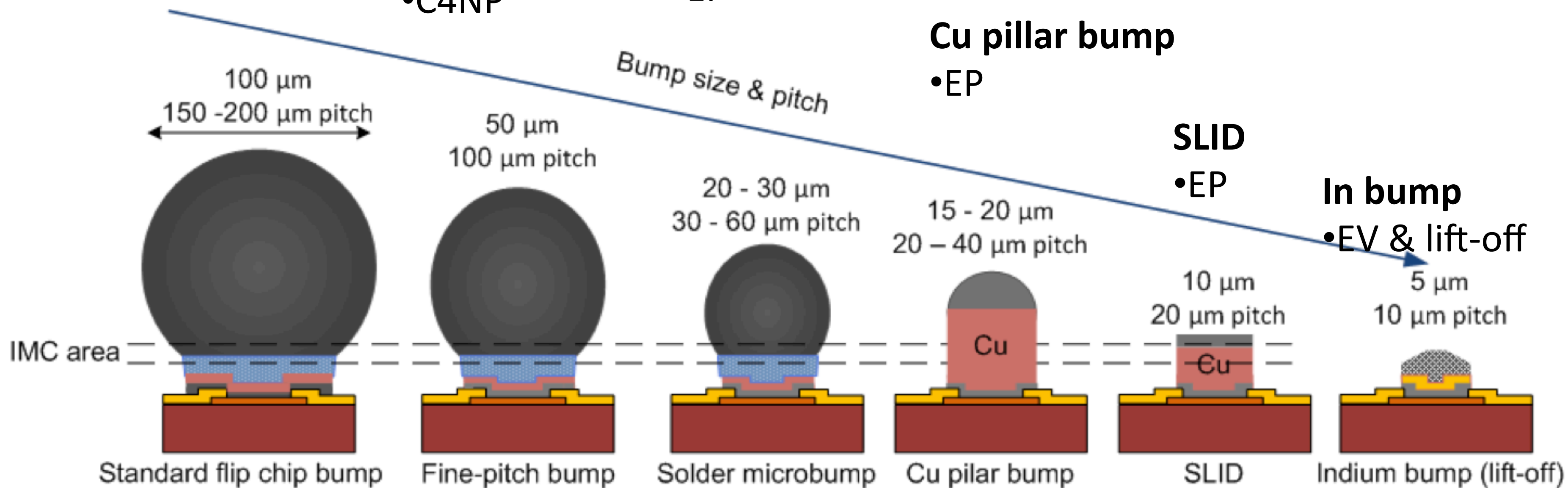
- EP

SLID

- EP

In bump

- EV & lift-off



Source: Introduction to High-density interconnection technologies on silicon wafers. 2010. S. Vahanen CERN

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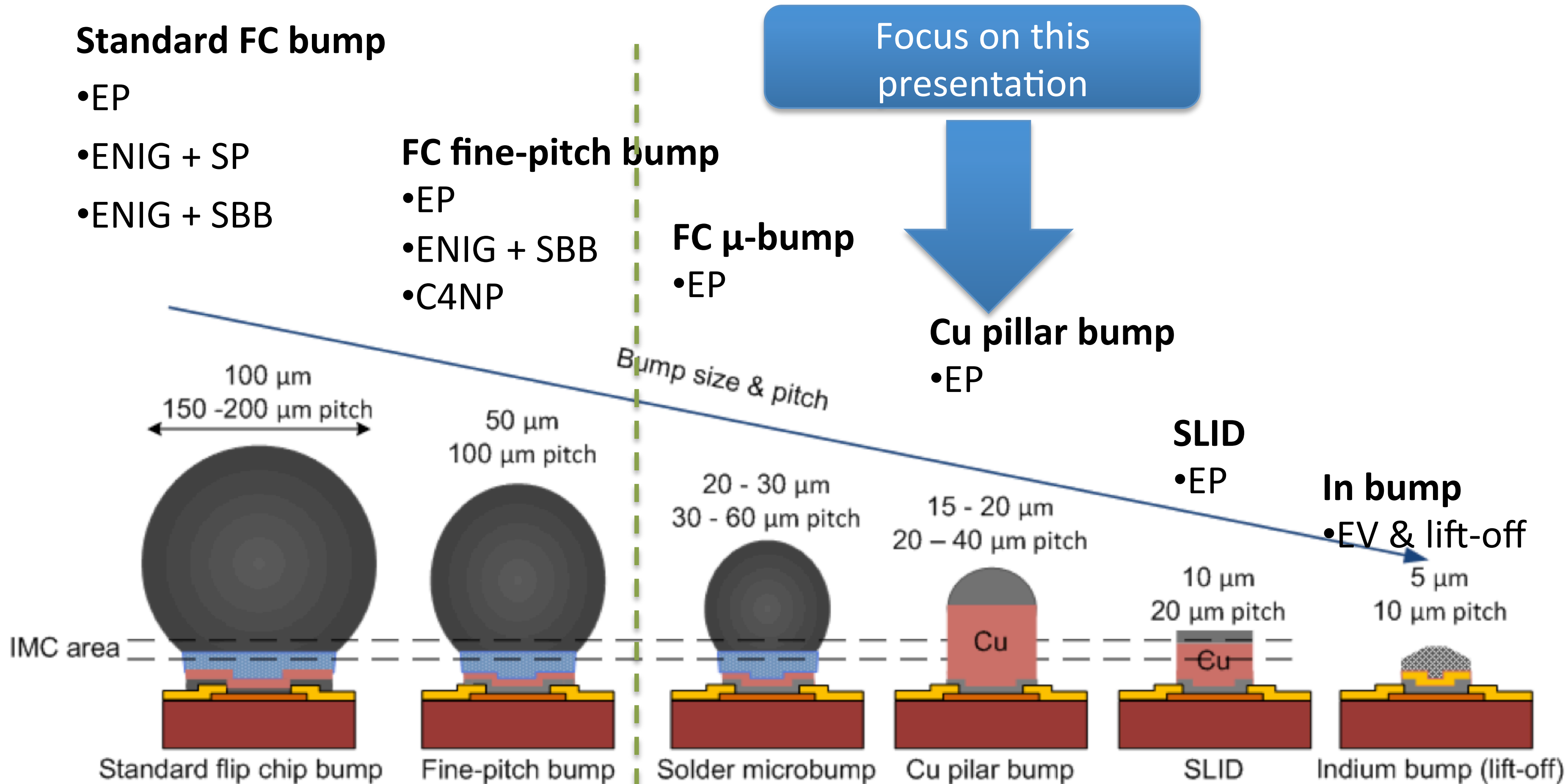

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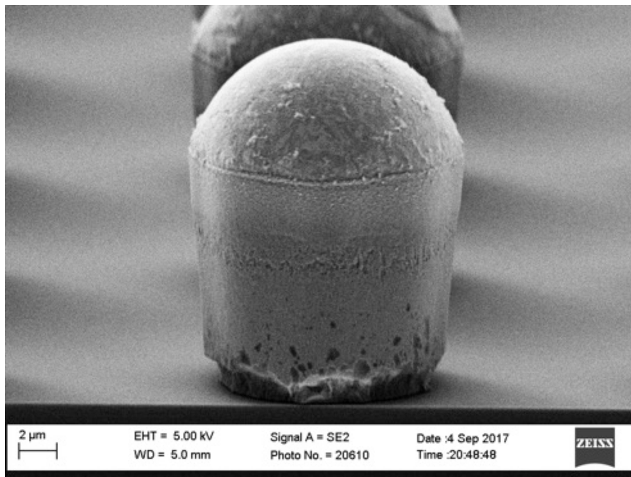
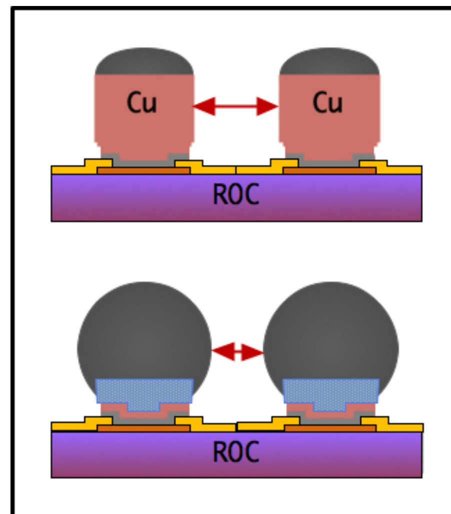
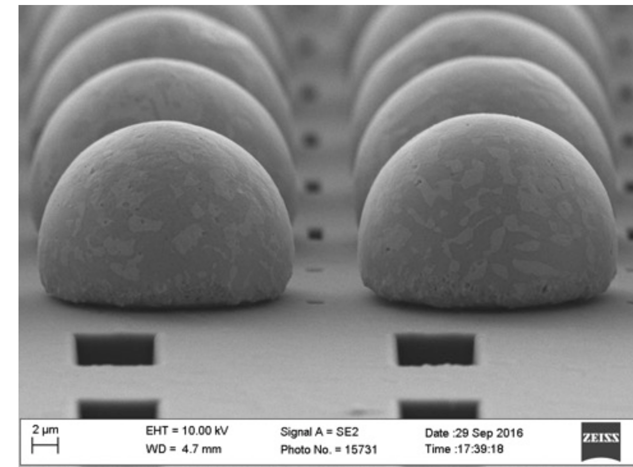
Solder bump structure – Cu Pillar with Solder Cap

- Cu pillar bump structures with solder (AgSn) cap have become mainstream
  - Widely available for bumping of 300 mm wafers – standard lead-free solution (mainstream)
  - Benefits: Compliant with fine pitches (low risk for shorting pixels), high stand-off height, relatively low radiation length and straightforward process transfer from 200 mm to 300 mm.
    - Very low risk for having shorted pixels during flip chip bonding
  - Electrical benefits: tall and fine-diameter pillars will reduce coupling to digital circuitry in pixels and thus reduce electronic noise and also reduce sparking between sensor and readout chips.





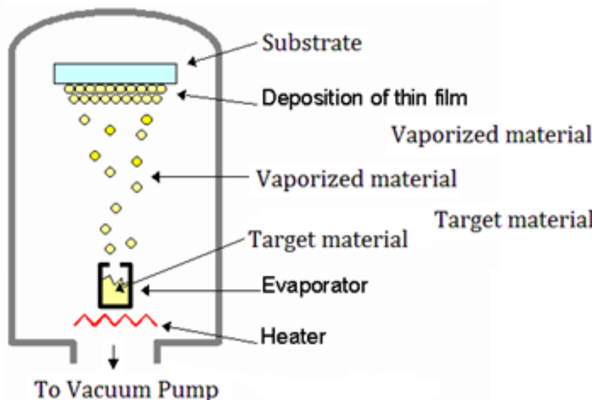


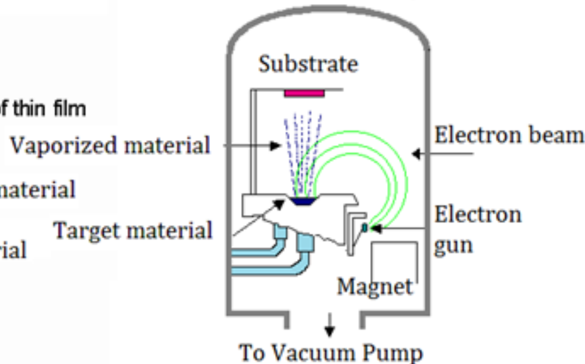
Cu pillars with solder cap @ 25 um pitch

Ni/SnPb solder bumps @ 25 um pitch

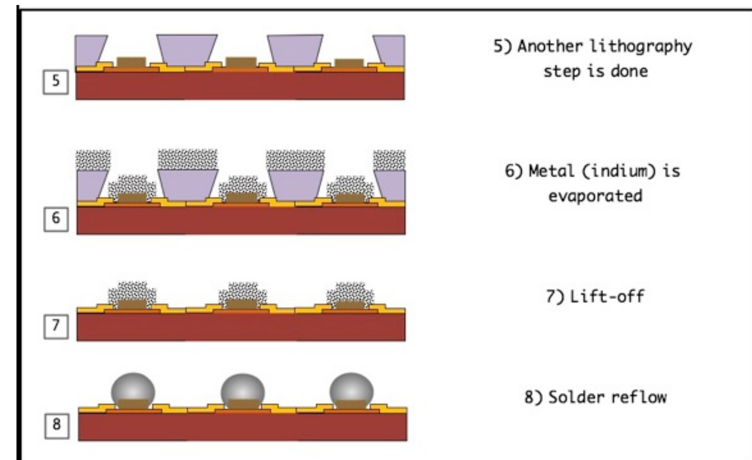
Solder bump structure – Evaporated In Bumps

- Indium bumps have been widely used in pixel detectors.
- Evaporation of indium bumps becomes difficult for 300 mm wafers
  - Waste of expensive In during evaporation – only fraction of the material ends up on the wafer
  - Very low stand-off height for the assembly (5 um – 10 um) for ultra fine pitches
  - **Electroplating of In is not yet common for 300 um wafers – but it's technically feasible**
    - Electroplating is recommended over evaporation
      - High deposition rate & taller bumps





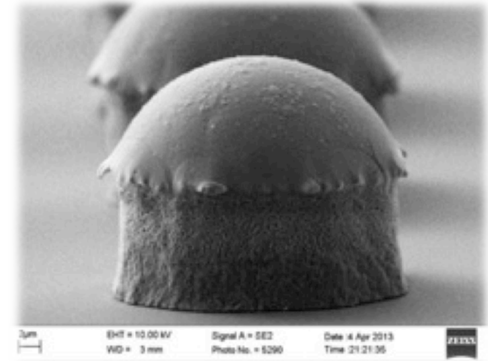
Principle of evaporation (www. http://hivatec.ca)



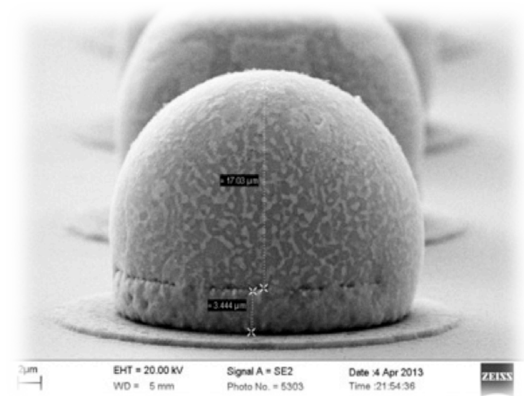
Evaporation-based bump deposition

Sensor Wafers - Solder bump structure

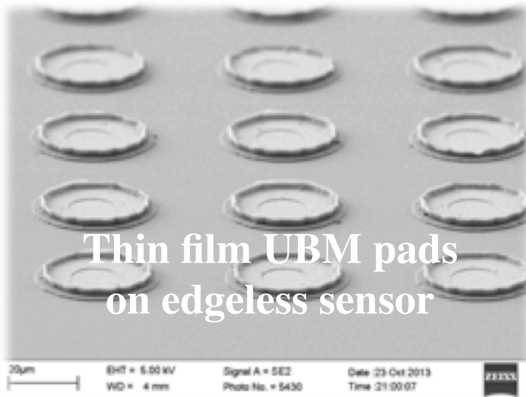
- Greater variety of bump/UBM materials available for the 6” – 8” Si sensor wafers
  - Thin film UBM pads & solder bumps with different materials
    - PVD deposition, electroless plating & electroplating
  - Thin sensor wafers require carrier wafers
    - Mechanical support & heat dissipation during processing
  - Hybrid solder bump structures − AgSn solder − low melting point metal/solder alloy
    - Facilitates flip chip bonding of thin chips
    - Risk: very complicated inter-metallic compounds − reliability?



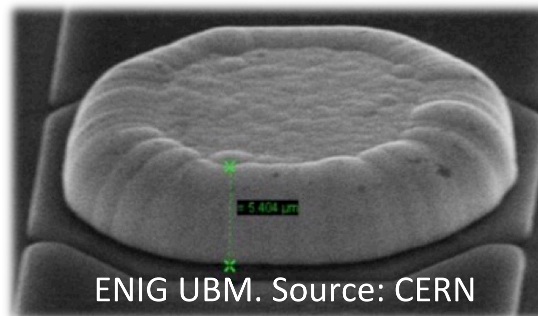
Cu pillars



Standard electroplated solder bumps



Thin film UBM pads on edgeless sensor



ENIG UBM. Source: CERN

Large ASICs

- Some applications require certain imaging sensor element size, which may be realised with stitching of reticles in CMOS process
  - + Less single modules = less flip chip placements - cost efficiency from assembly point of view
  - + Favours simple CMOS designs
  - – Reduced electric yield of ASIC
  - – Requires very good flip chip process (UBM/bumping/FC bonding) yield
  - – Potential limitations with pixel pitch using compound semiconductor sensors
  - – Thin ASICs will increase the complexity

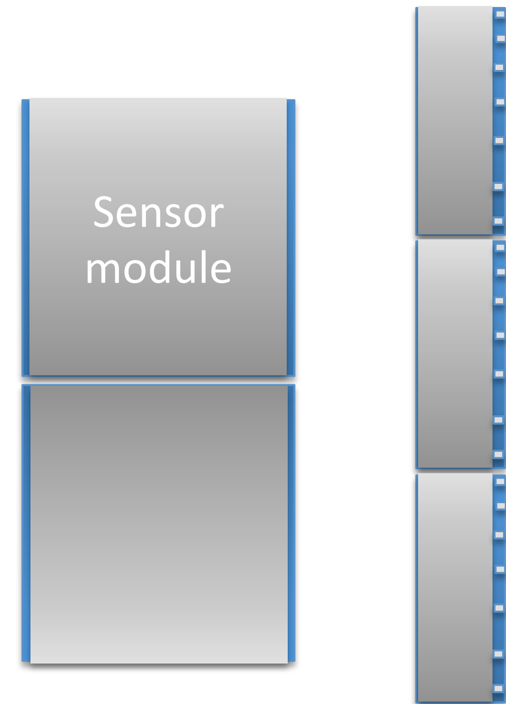
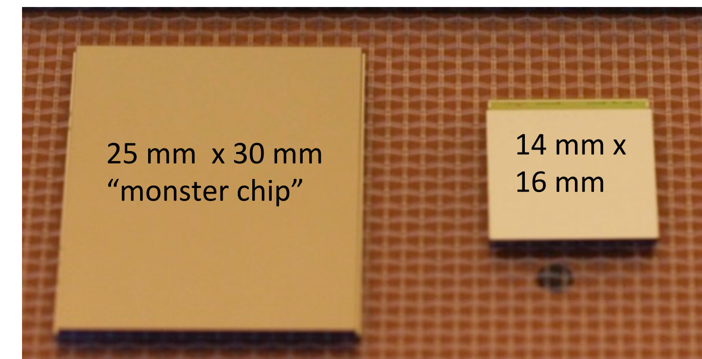


Illustration of row cameras

- 2-side-buttable modules for row cameras
  - In-line scanning application

- Thin chips: Flip chip bonding of single chips of full thickness Si chips chip-to-chip or chip-to-wafer and thinning of the ASICs afterwards
  - Cost-efficient process



ASICs - Thinning

- CMOS layers ~15 µm consist of stack of metal and dielectric layers
  - Glass dielectrics have low Coefficient of Thermal Expansion (CTE), but have high intrinsic stresses.
    - Domination of stresses at room temperature
  - Metals have high CTE
    - Domination of stresses at elevated temperatures
- Thin chips do not have much of supporting Si
  - Radical bending of chips (thickness < 300 µm) as a function of temperature
  - Corner joints open up during solder reflow of standard FC process

Illustration of wafer bow and the importance of using support wafers

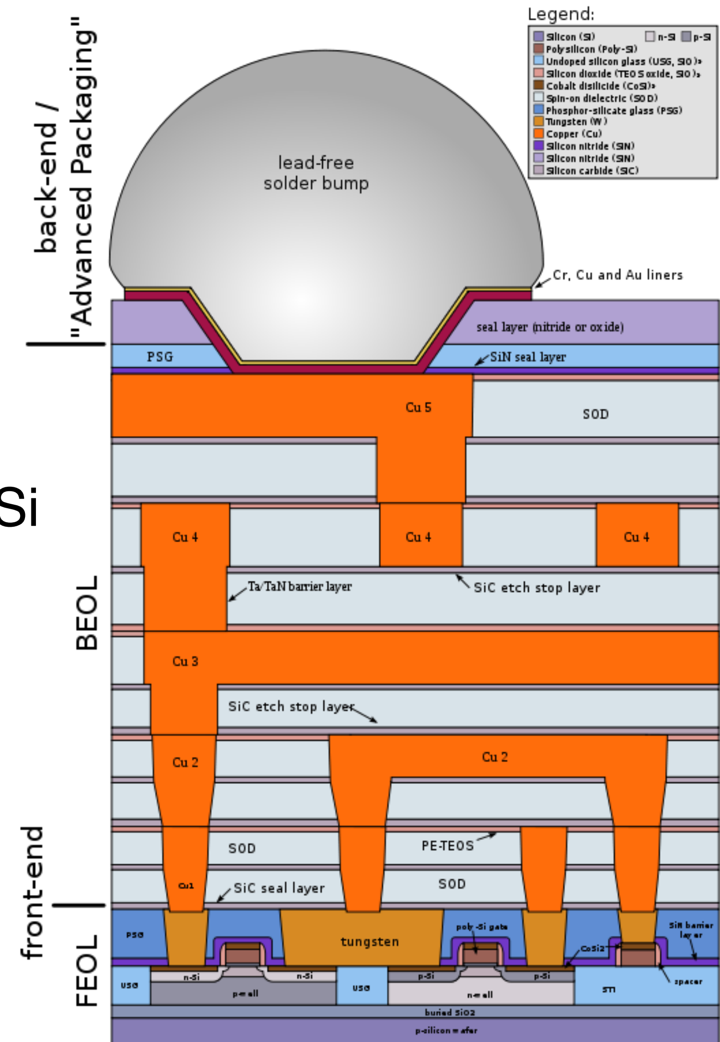
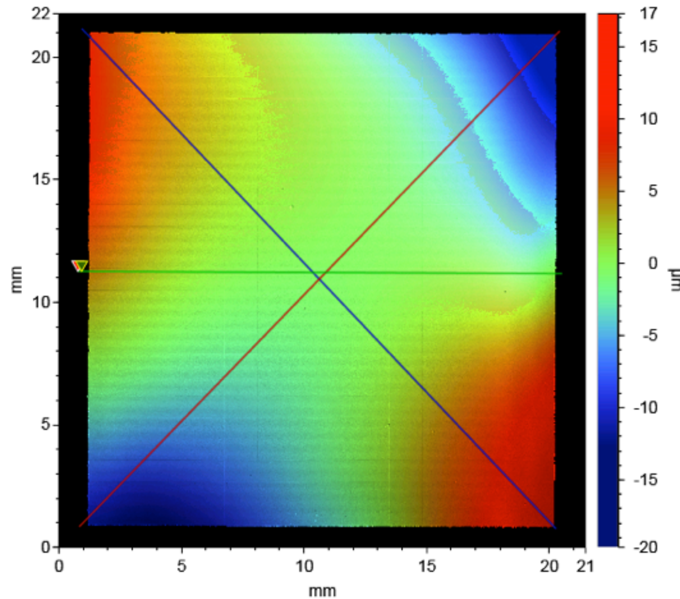


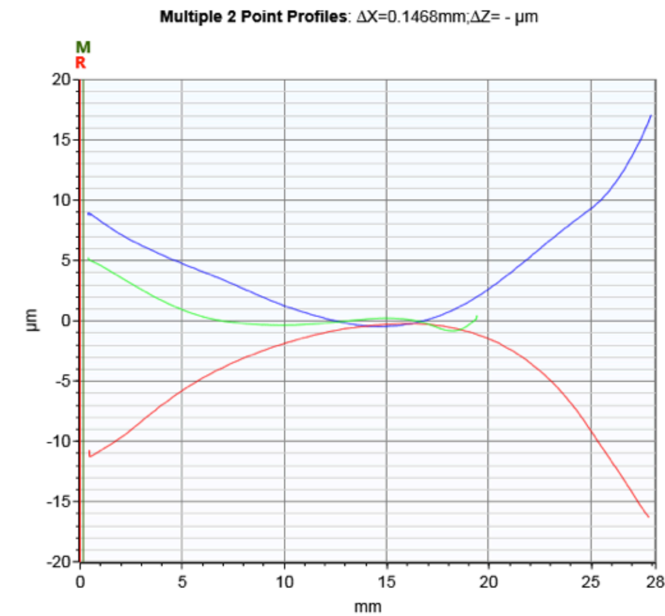
Illustration of CMOS layers

Source: Wikipedia “Back end of line”

ASICs – Thinning cntd

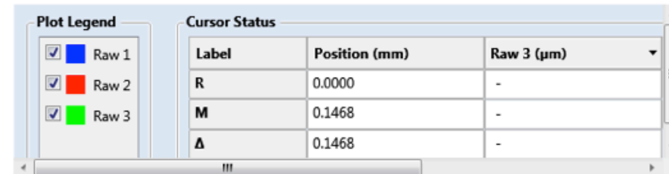
- Ultra-thin chips (< 200 um) may have different profiles on wafer-level
- Bow of the ASIC depends on:
  - Actual material, their thickness and structure in CMOS layers – CMOS process dependency
  - Stress caused by solder bumps
  - Back-grinding damage





Analytical Results

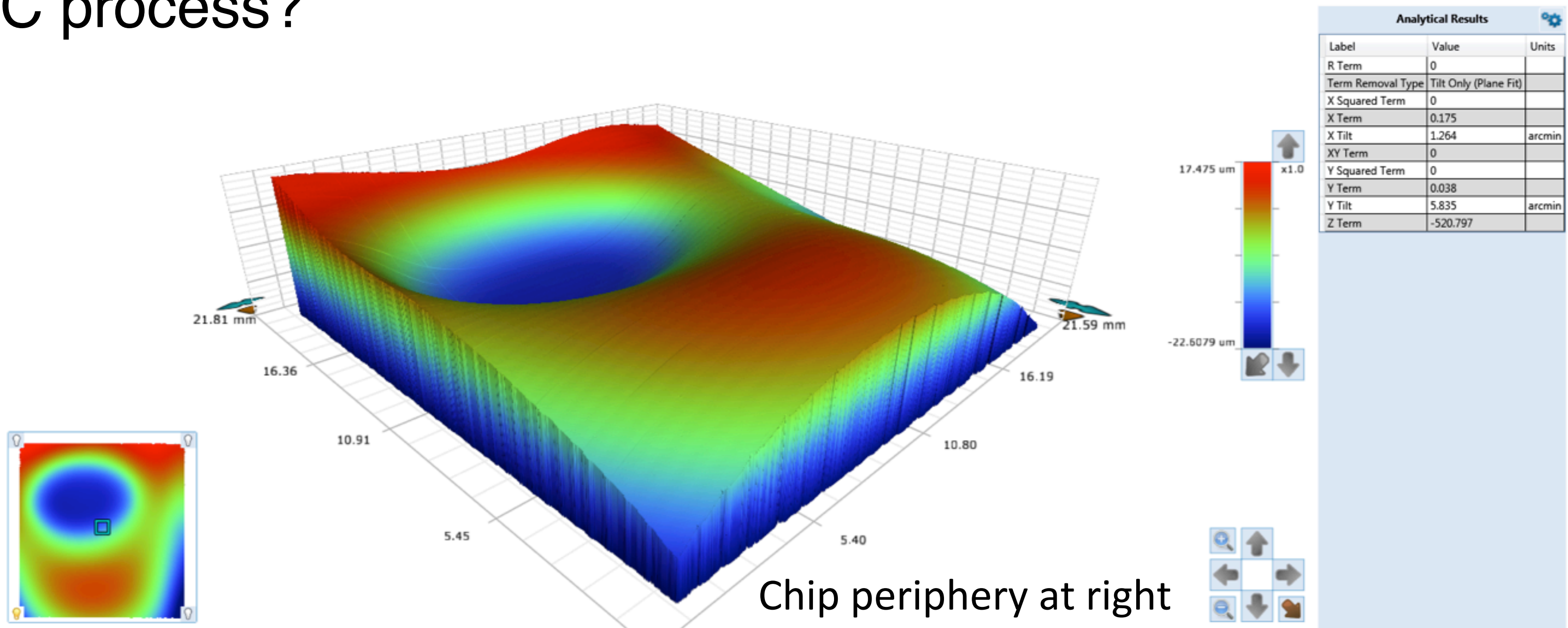
Label	Value	Units
Average	0	nm
Data Points	1779906.944	
Percent Data Points	82.04	%
Ra	3.588	µm
Rp	17.283	µm
Rq	4.819	µm
Rt	36.972	µm
Rv	-19.689	µm



Profile of 100 um thick FE-I4B ASIC with solder bumps. Bow of ~30 um can be seen. Image taken from bulk Si side.

ASICs – Thinning Chip Bonding

- What happens during flip chip/solder reflow with standard FC process?



Label	Value	Units
R Term	0	
Term Removal Type	Tilt Only (Plane Fit)	
X Squared Term	0	
X Term	0.175	
X Tilt	1.264	arcmin
XY Term	0	
Y Squared Term	0	
Y Term	0.038	
Y Tilt	5.835	arcmin
Z Term	-520.797	

Chip periphery at right

- Profile of 100 um thick FE-I4B ASIC – Si sensor module. Bow of ~30 um can be seen. Image taken from bulk Si side.
- Thermal expansion causes the chip to warp during the assembly.
- Solder joints are connected in valleys; peak regions have disconnected bump bonds.

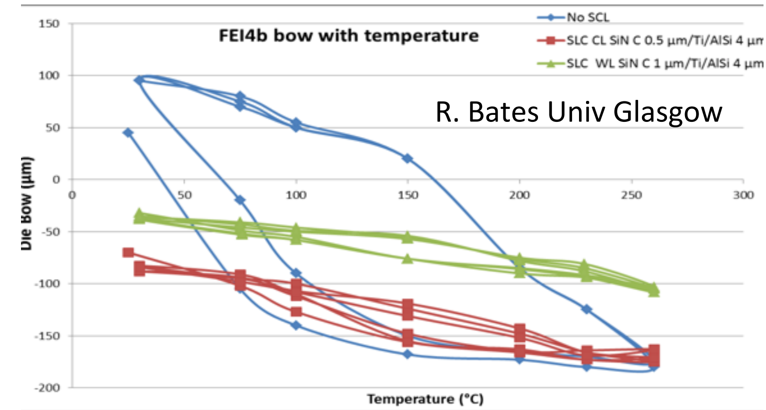
Flip Chip Bonding

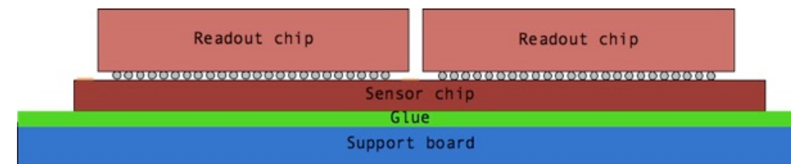
- To cope with the chip bow, the chips have to be kept flat during the flip chip bonding and reflow processes
  - When solder is in molten state and the chips are not hold in parallel, the thin ASIC will bend and open bump bonds.
  - It is very challenging to flip chip bond strongly curved chips without:
    - Support chips/wafers
    - Custom designed tools, jigs or other fixtures.
    - Special solder bump structure

- Solutions:
  - Thermo-compression bonding processes favored
    - Permanent bonding – rework won't be easy – problem with multi-chip modules (exception: In – In bump bonding)
  - Flip chip bonders with formic acid option solves the bonding problem, but slows bonding rate.
  - Low temperature flip chip bonding
  - One alternative is to keep the chips flat during the reflow using jigs & fixtures during the reflow process – fully compatible with all flip chip bonders
- Solutions must be cost efficient!

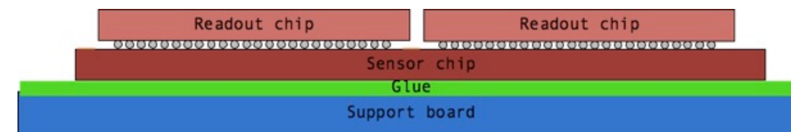
Flip Chip Bonding of Thin ASICs - Remedies

- Deposition of the Stress Compensation Layers
  - Difficult to control - no consistency from chip-to-chip and from wafer-to-wafer.
  - Technology transfer from 200 mm to 300 mm wafers might be very tricky.
  - It helps but doesn't solve the problem alone.
- Carrier chips/wafers during flip chip bonding
  - Works well, but increases the cost of the process (bonding and release steps).
  - Dicing through glass carrier – Si CMOS wafer brings some restrictions to dicing precision – wider blades have to be used.
- Support during reflow – Advacam method
- Flip chip bonding at lower temperatures
  - Alternative #1 Hybrid bump structures with low melting point alloy on one side
  - Alternative #2 In – In bonding
- Use of relatively small chips
  - Less bow
- Crazy idea: Thinning of modules after flip chip bonding
  - Feasible if the bump density is high enough
  - Solves the biggest technical and cost related problems, but moves the problem to another step.
  - Simple grinding tools – focus on developing fixtures
  - Protection of the wire bonding pads

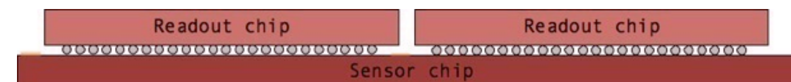




Multi-chip modules glued on support wafer. Protection of WB pads.



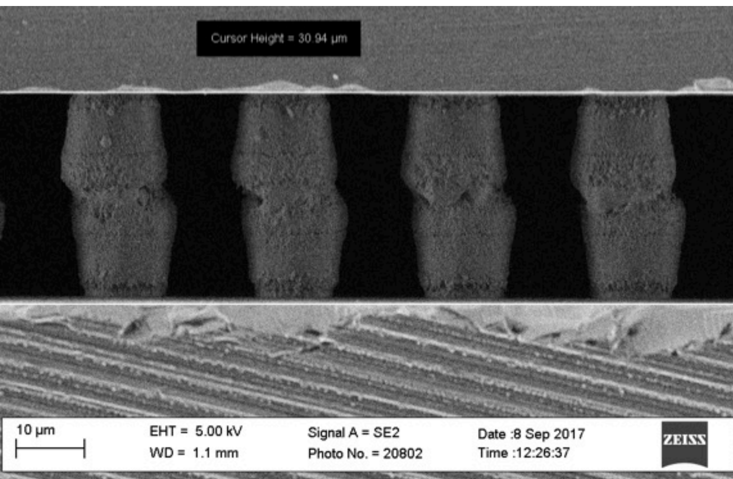
Grinding of the readout chips to desired thickness. Grinding sets requirements for the pixel density.



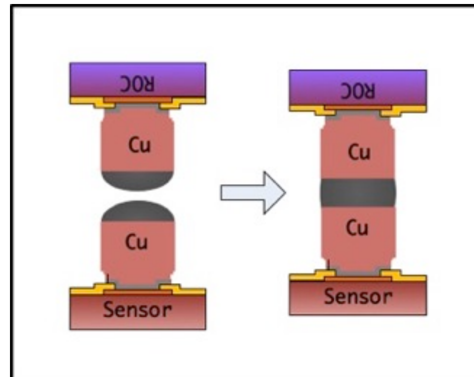
Release and washing of modules.

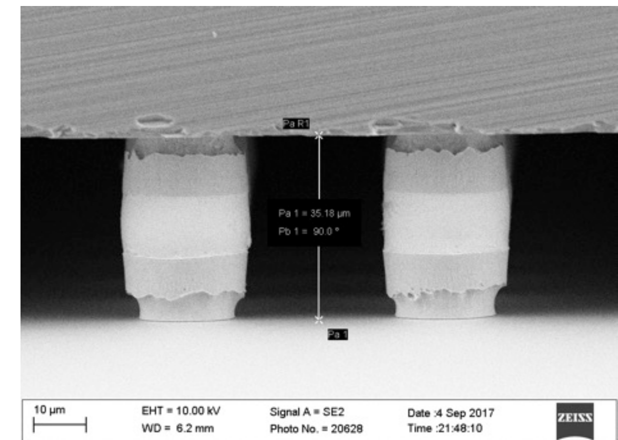
Cu pillar bumps

- Cu pillar bumps with solder cap is the solder bump structure to bet in future
  - They're on Advacam roadmap
- ASIC wafers will have electroplated Cu/AgSn or Cu/In solder bumps
- Sensor wafers could have electroplated Ni or Cu UBM with indium solder cap
- Volume of the solder cap is crucial with Cu pillars (see picture)
- Cu/In vs. Cu/In bump structure would solve many issues
  - Room/low temperature flip chip bonding – less bow on thin ASICs
  - High stand-off height – helps with underfilling
  - Compatibility with compound semiconductor sensors



FC bonded Cu pillars with SnPb cap @ 25 um pitch with 30 um stand-off height

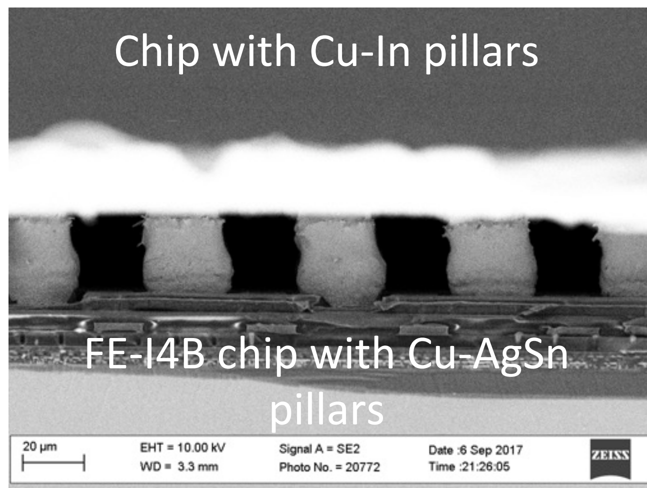


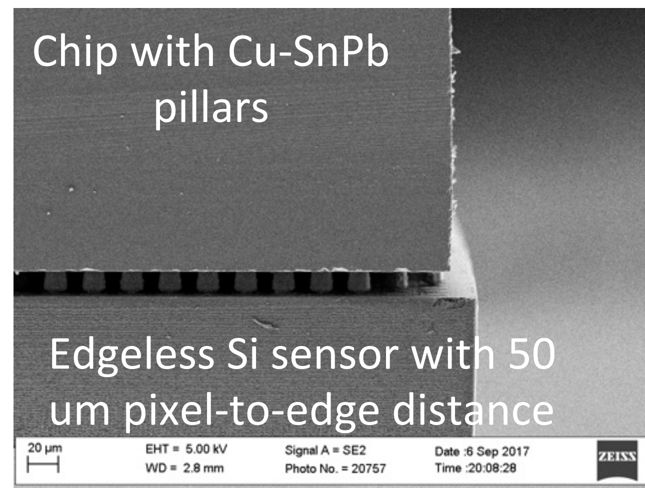


Bonded Cu pillars with In cap @ 50um pitch with 35 um stand-off height

Flip chip bonding

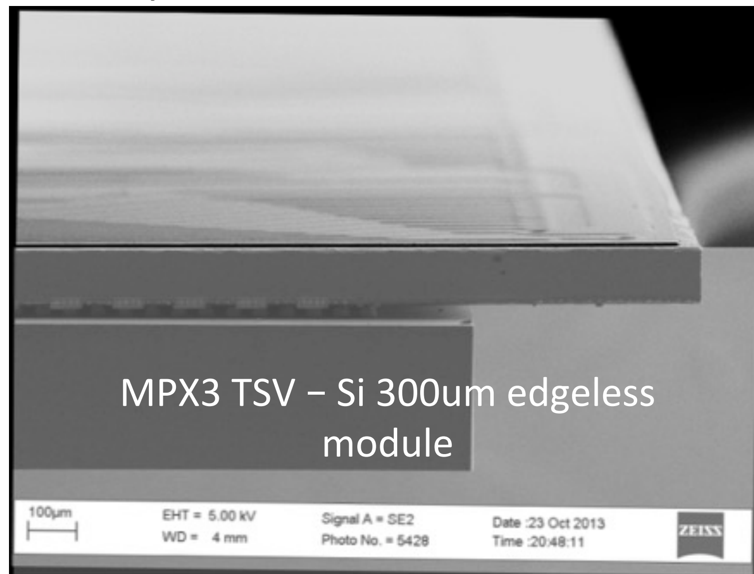
- Cu-AgSn pillar flip chip bonding works against Cu-In structure at rather low reflow temperature 185°C
  - AgSn bumps typically require reflow at 250°C
  - Demonstrated with FE-I4B ASICs (50 um pitch)
  - Further tests needed as Ag may cause reliability issues in the complex solder joint
- Cu-SnPb solder pillars at 25 um pitch were demonstrated with edgeless Si sensor with thin film Ni/Au UBM pads
  - Risk of solder bridges is eliminated during flip chip bonding step using pillar structure

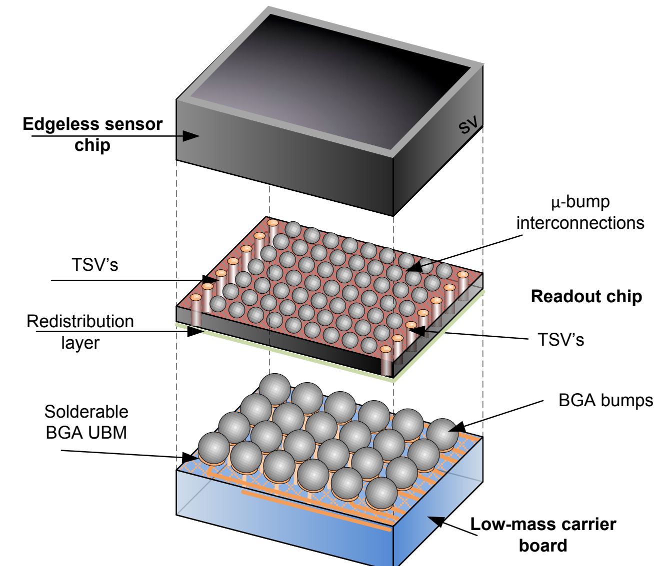




Through Silicon Vias (TSV)

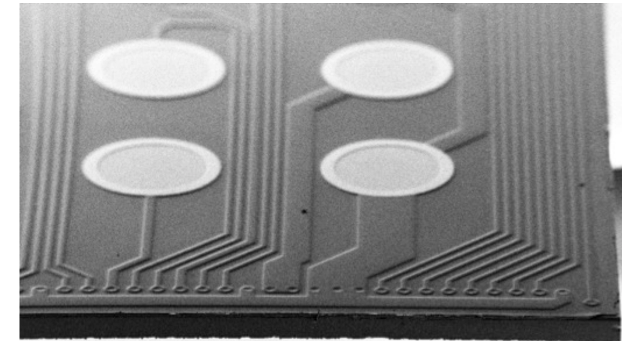
- TSV's are needed for 4-side buttable modules with minimal periphery extension
  - Construction of large panels out of single modules
- Edgeless sensors are needed to minimize the footprint of the modules
- It is challenging to deposit the solder bumps on the TSV ASIC wafers
  - TSV process becomes very complex – solder bumps suffer from high process temperatures
  - Thin (100 um) thick TSV ASICs need carrier substrates during solder reflow step



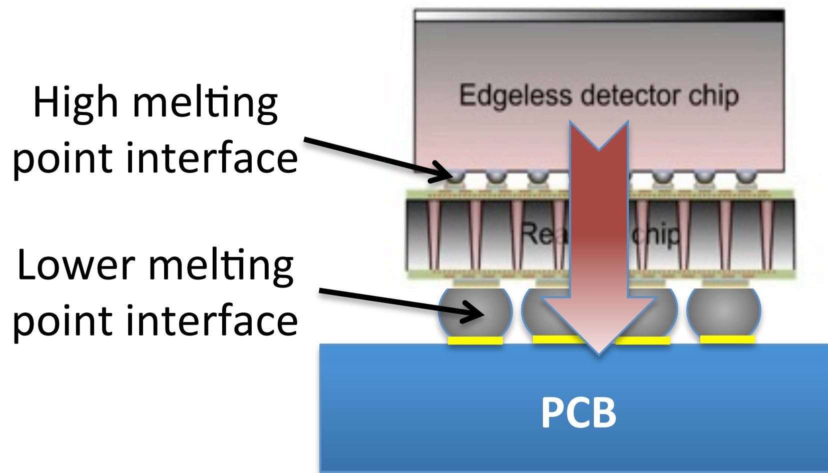


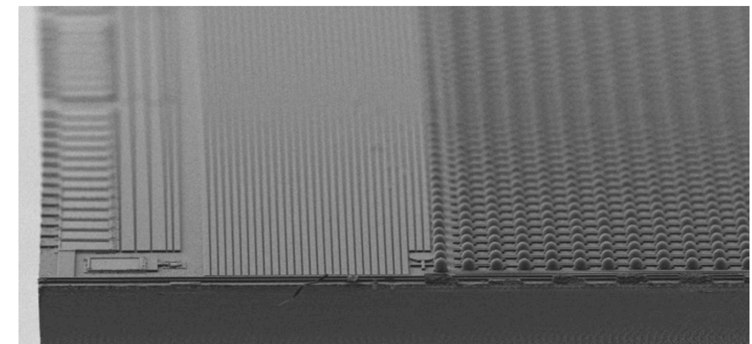
Through Silicon Vias (TSV) - cntd

- Solder bumps have to be deposited on the sensor wafers
  - Wafer-level solder plating on sensor wafers
  - Chip-level solder transfer – complex process only for small series prototyping
  - Flip chip and BGA bumps must have a melting point hierarchy
  - Flip chip bonding of thin TSV ASICs with RDL layer has shown to be easier than thin chips without RDL

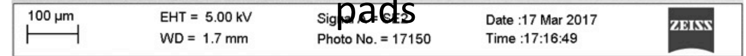


SEM image of the RDL layer of MPX3 TSV ASIC



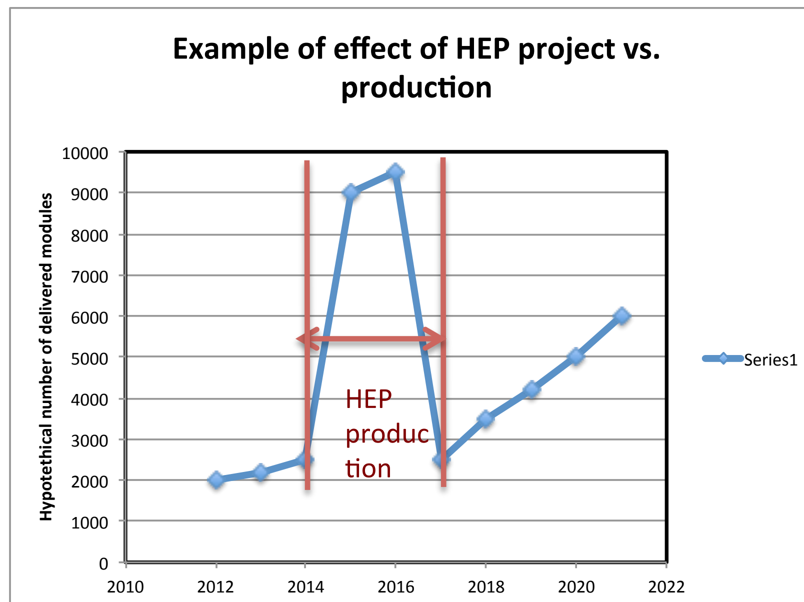


Solder bumps transferred on chip-level to MPX3 TSV ASIC with Ni/AU UBM pads



Cost

- Cost of bump bonding is high because of rather small series and lack of constant production
  - Pricing can be greatly affected when closing the annual production capacity
- HEP experiments provide lot of one-time work for short to mid-term
  - Cannot justify investment in the process equipment without consistent production
  - Hiring of personnel is problematic (fixed term contracts)
  - Cheaper bump bonding prices come along the growth of generic service sales for the industrial partners
- Common volume-based (scientific & industrial) need defines the cost of services
- Keep the technical specifications as easy as possible – simplicity rocks!
  - Lower cost of services
  - Thinning of multi-chip modules could be done outside high-end clean rooms



Solutions: 200 mm Si Sensor Wafer Fabrication

- Two sensor batches finished
- Processed 9 pcs of 200 mm wafers so far
- Wafer thicknesses: ~~300~~, 380, 500 & 675 *μm*
- Support wafers needed for ≤300 um thick sensor wafers
- Sensor polarity: P-on-N
- Wafer types used:
  - N FZ – <100>, ~5000 Ωcm
  - N MCZ – <100>, ~5000 Ωcm
- Part of the process steps subcontracted
- Wafers have electroplated Ni/SnPb solder bumps

Lot: ladder200
Wafer: mn6-1gs
X1
I@300V nA

					-41	-44	-44				
		-61	-52		-128	-51	-701	-46	-20		
	-27	-32	-36	-38	-56	-65	-61	-61	-42	-83	
	-101	-99	-93	-82	-70	-46	-44	-50	-57	-84	
-72	-23	-75	-86	-90	-94	-96	-109	-119	-126	-137	-86
-117	-180	-168	-154	-136	-120	-31	-33	-69	-84	-74	-10
-648	-83	-30	-35	-35	-35	-22	-27	-30	-31	-32	-87
	-989	-45	-43	-35	-30		-546	-798	-320		
	-62	-85	-124	-135	-149				20000		
			-113	-14	-14	-30	-112	-26			
				-3960	-190	-117					

0
-100
-200
-300
-400
-500
-600

MCZ wafer from the second batch of 200 mm

Acceptance range for 675 μm thick wafers: current <300 nA/cm^2 @ 300 V & breakdown >400 V

FZ: median leakage current 26 nA/cm^2 second batch

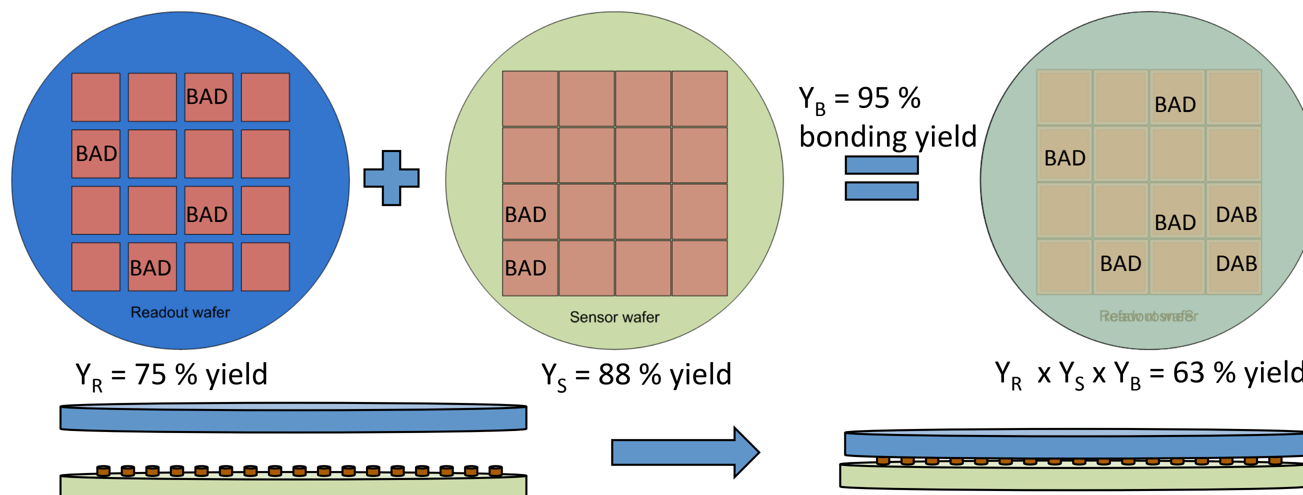
MCZ: median leakage current 30 nA/cm^2 second batch

200 mm wafer

150 mm wafer

Solutions: Wafer-to-Wafer Bonding

- Advacam has transferred its 6” Si sensor wafer process to 8” wafers
  - Wafer bonding of 200 mm wafers becomes a viable option
  - 2 choices:
    - Bond whole wafers (see backup slides)
    - Prepare built-up wafers from KGD’s by stepping the chips on the wafer with adhesive layer (see backup slides)
  - Benefits:
    - Cut down the flip chip bonding price of single modules significantly at coarse pitches (≥ 100 um)
    - Solves the thin chip problem (thinning after wafer bonding)
  - Drawbacks:
    - Potential yield killer combining the yields of two wafers. Guard rings take space on sensors and all the CMOS chips cannot be bonded without a custom design.
- Promising technology for outer low-cost pixel layers with coarse pixel pitch
- Promising for
- Simplicity of the ASIC is important to have high electrical yield
  - ~90% yields required for both the wafers to have sufficient overall yield



Summary

- Cu pillars with solder cap have prospects to be used for flip chip interconnects for generic pixel detectors.
  - Compatibility with 300 mm ASIC wafers
  - Applicable for ultra-fine pixel pitches – high stand-off height
- Cu-In-In-Cu bump bonds are promising for flip chip bonding for thin ASICs
- Multi-element solder alloys / bump structures have potential but need to be studied and tested
- Price level of bump bonding will scale down with regular production
- 200 mm Si sensor wafers enable wafer-to-wafer bonding

Thank You for Your Attention

THE END

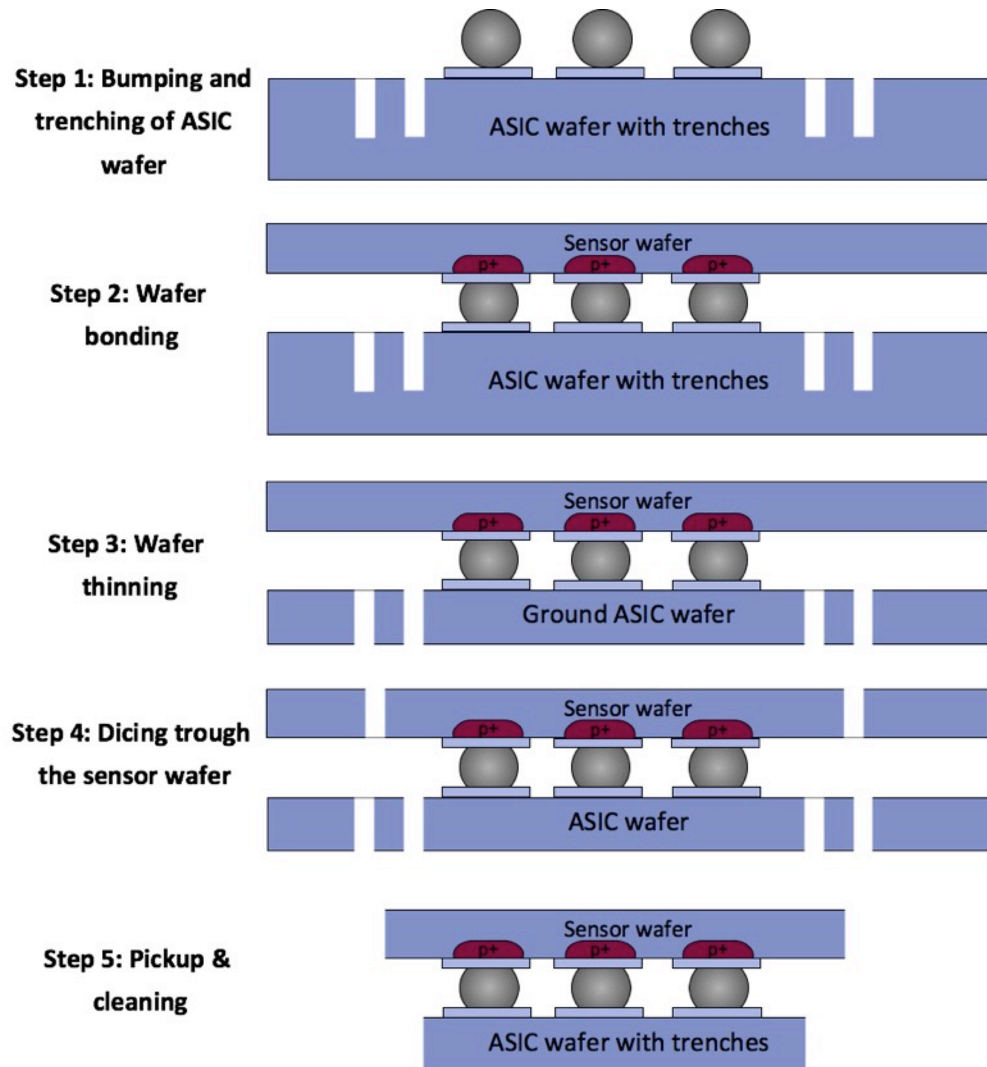
Advacam fabricates Si sensors and provides bump bonding services for pixel detectors

Backup slides

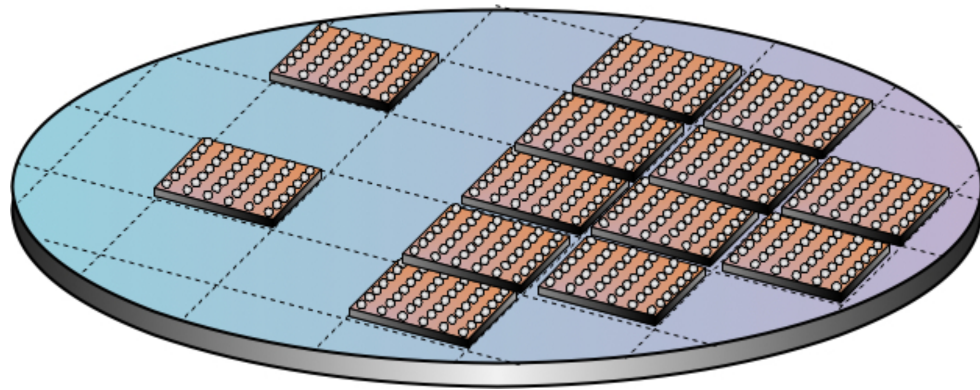
Wafer Bonding

- Illustration of the basic wafer bonding scenario with sensors having a guard ring structure

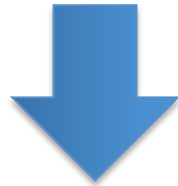
- It is benefical to have rather high interconnects to leave margin for dicing through the sensor wafer

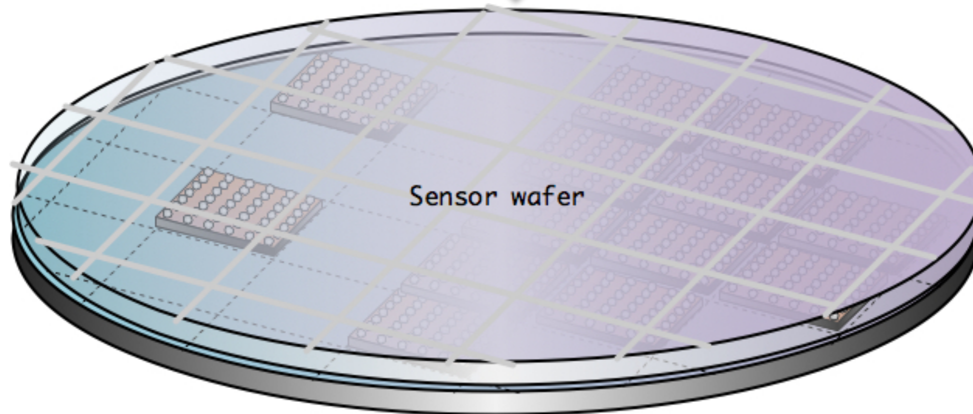


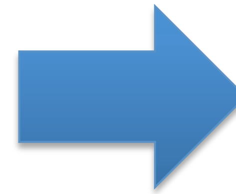
Wafer Bonding Built-up Wafer

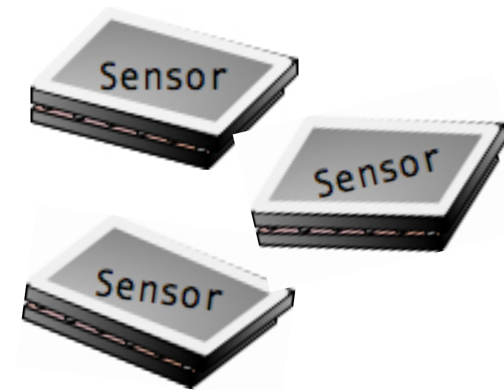


Pick & place of KGD's on glass wafer with adhesive layer in array matching the sensor wafer





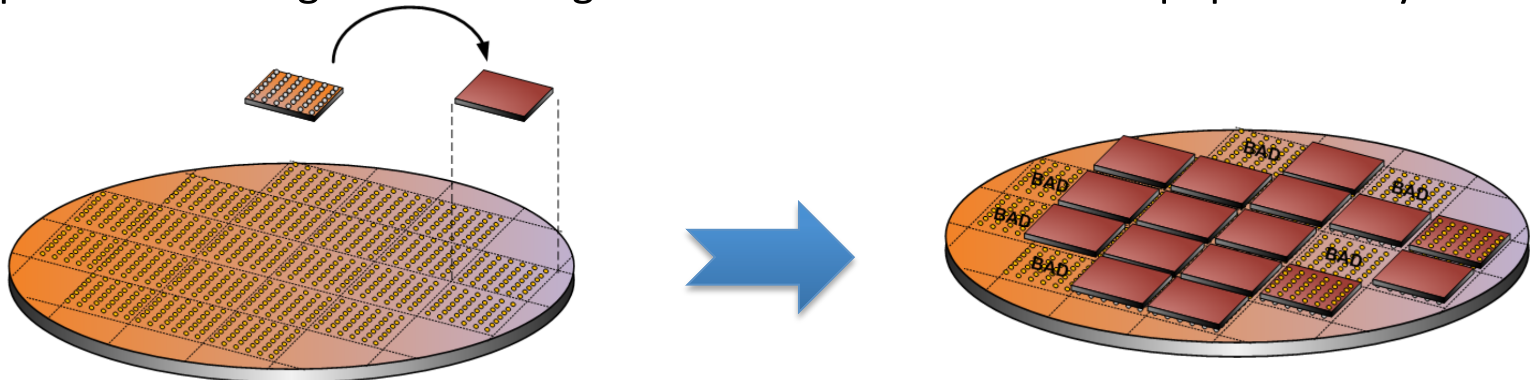




Bonding of the sensor wafer to the built-up wafer, Release of ASIC's from glue using laser beam on wafer-level and dicing through the sensor wafer

Chip-to-Wafer Bonding

- Technology benefits
  - C2W reduces manual handling of assemblies.
  - Increase in the throughput – the whole wafer has to be assembled at the time.
  - Sensors can be bonded against known good dies (KGD) – economically efficient.
  - Chips with different sizes can be bonded – flexibility!
  - Edgeless sensor chips needed - large guard ring structure consumes space on wafers.
  - C2W bonding is currently being used in industry, but it hasn't been used much in assembly of pixel detectors.
  - C2W is an intermediate step towards W2W bonding
- Common assembly cycle:
  - a)Tack-bonding (pick & place) of individual chips + mass reflow for the device wafer in reducing ambient.
  - b)Collective bonding can be done in wafer bonder after tack bonding with a cover wafer (slow processes such as hybrid-metal bonding).
- C2W bonding is favored when large and expensive dies are used.
- Optional: thinning after bonding if the whole wafer has been populated by the chips



Stand-off Height - Sparking

- High bias voltage over the sensor may cause sparking
  - ASICs will be killed
- Thick organic dielectric layers are preferred on sensor chips
  - Spin-on photo-sensitive dielectric materials patterned with lithography
    - Electroplating is the only compatible method in terms of step coverage
  - CVD deposition of organic dielectric layer – conformal coatings (parylene)
    - Wire-bonding pads have to be protected
- Increasing the stand-off height of the module reduces the sparking as well
  - Double-sided plated Cu pillars