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Solutions for flip chip bonding of future pixel detectors

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Flip chip processing of pixel detectors face many technological challenges when moving to finer CMOS technology nodes, production of 300 mm wafers and having larger chips than ever. In addition, finer pixel pitches and thinner CMOS chips are required, which will cause headache for the wafer bumping and assembly foundries. There will be fewer foundries, which are able provide all the required services, and thus the responsibilities will have to be shared within several foundries. Despite having more challenging logistic scheme and taking the technological challenges to next level, the hybrid pixel modules should be cheaper than ever in order to have large areas covered within the pixel detectors.

This presentation considers various technological aspects of flip chip process for the hybrid pixel detector and suggestions for remedies are given to overcome the problems in flip chip process of hybrid pixel detectors for vertex/tracking applications. Wafer bumping concepts and solder bump structures will be introduced for fine pixel pitches and low soldering temperatures. Thin CMOS chip flip chip bonding solutions, novel Si sensors and future large-area tiling of Si sensor modules using through silicon vias will be introduced.

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